

SYNTHESIZED WSE₂ FIELD-EFFECT TRANSISTORS
AND PROCESS FOR STEEP TRANSISTORS

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Abstract

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Voltage scaling is an important factor in device miniaturization that leads to reduction in power consumption. Tunnel field-effect transistors (TFETs) are attractive candidates to overcome this fundamental limitation of the MOSFET. Atomically-thin two-dimensional semiconductors present new opportunities for minimizing transistor channel thickness and improving gate efficiency. The epitaxy of two-dimensional materials has been advanced in the past 5 years to enable device research to move from exfoliated to grown channels, from customized electron beam patterning to stepper lithography, from back gates to deposited top gate dielectrics, and from single device processes to full batch processes. The aim of this research has been to utilize synthesized WSe₂, a transition metal dichalcogenide (TMD), as a FET channel material and to develop a TFET fabrication process. A stepper-based process has been demonstrated for fabricating WSe₂-on-sapphire FETs with 3-4 monolayer channel thicknesses. The WSe₂ was grown by collaborators from Penn State University by metal organic chemical vapor deposition (MOCVD). The development of a device process based on these materials has allowed wafer scale batch fabrication of 2D transistors for the first time and characterization of transport across centimeter scale sapphire substrates. This research has found solutions across a wide range

of technical challenges. Methods for gate stack nucleation were developed to deposit gate dielectrics on WSe₂ channels. The gate dielectric was nucleated using low temperature atomic layer deposition (ALD) of Al₂O₃ at 110° C to initiate layer formation, followed by Al₂O₃ at 200° C to complete the dielectric. The FET gate stacks were pinhole free yielding leakage current density of less than 0.1 fA/μm² at 1 V and an equivalent oxide thickness (EOT) of 4.8 nm (physical thickness of 11 nm). In contrast to conventional semiconductor processing, contact adhesion is an important consideration. Contacts must generally be anchored to the substrate and the contacts themselves must not have inherent strain as this can then delaminate the 2D material. Methods for forming junctions and doping are also required. For this, electric double layer (EDL) doping of WSe₂ channels has been utilized using polyethylene oxide: cesium perchlorate (PEO:CsClO₄) and side gates. Use of these doping schemes required development of measurement protocols to establish measurement repeatability and enable the exploration of *n*-FETs, *p*-FETs and TFETs.

This thesis is dedicated to
my beloved parents: Mohammad Asghari Heidarlou and Mahboubeh Yeganli
my brother and sisters: Reza, Masoumeh, and Mitra
my husband: Kasra Pourang
and my lovely son, Dennis.

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CHAPTER 1: INTRODUCTION

In this chapter, apart from introducing the structure of the tunnel field-effect transistor (TFET) and its operation principles, a brief quantitative discussion of band-to-band tunneling (BTBT) and performance expectations is provided. It helps to understand why TFETs defeat some of the complementary metal-oxide-semiconductor (CMOS) limitations. Subthreshold slope as a critical feature in the transistor performance will be discussed. At the end, the importance of transition metal dichalcogenide (TMD) materials and the reasons for choosing them as promising materials for TFETs will be stated.

1.1 Tunnel FETs

In CMOS technology, current is due to injection of carriers from source to channel over an electrostatic potential barrier. The barrier height is controlled by the gate voltage. The carriers in the source reservoir are in thermal equilibrium with the source contact and the distribution of carriers in the conduction band is defined by the Fermi-Dirac distribution given by

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)}, \quad (1.1)$$

where k_B is Boltzmann's constant, T is the absolute temperature, E is the energy level, and E_F is the Fermi energy level. For energies $E - E_F \gg 3kT$, the carrier density falls off

exponentially. However, the gate cannot completely suppress carriers from being injected to the channel since there are always carriers with energy higher than the source-channel potential barrier. So, there will be a voltage-dependent drain current known as the subthreshold current.

The subthreshold swing of a device is defined as the change in gate voltage that must be applied to create a decade increase in the drain current. Increasing the gate voltage of an n -FET decreases the potential barrier between the source and the channel, leading to an increase in drain current. The subthreshold slope, SS , of a MOSFET is given as [1]

$$SS = \left(\frac{d(\log I_D)}{dV_{GS}} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_D}{C_{OX}} \right), \quad (1.2)$$

where I_D is drain current, q is the fundamental charge, V_{GS} is the gate-source voltage, C_D is the depletion capacitance, and C_{OX} is the gate oxide capacitance. A lower subthreshold swing enables higher on-to-off current ratio, I_{ON}/I_{OFF} , with lower voltage swing, and as a result lower power dissipation. For CMOS, from Eq. (2) the lowest possible value for subthreshold swing is limited to $SS = 2.3(kT/q) \approx 60$ mV/decade at room temperature. As an example, to achieve current ratio of 10^5 , a gate voltage of at least 0.3 V is required. Therefore, reduction of the supply voltage faces these limits to meet the I_{ON}/I_{OFF} ratio requirements [1].

To decrease the supply voltage further in a MOSFET, a current control mechanism with capability of achieving subthreshold swing below 60 mV/decade is required. The TFET can achieve less than 60 mV/decade subthreshold swing and provide a steeper turn-off characteristic than the MOSFET. The simplest TFET is similar in structure to the MOSFET, but whereas in the MOSFET the doping type in the source and drain are the same, the TFET utilizes opposite types in the source and drain that leads to the formation

of an interband tunneling junction between source and channel. Figure 1.1 shows the difference between the basic structure of an n -channel MOSFET and a TFET. The major difference between them is that the source doping in the n -channel TFET is p -type, while it is n -type in the MOSFET. The channel region in the TFET is typically undoped and labeled intrinsic, but the channel typically has a background conductivity resulting from native impurities and defects.

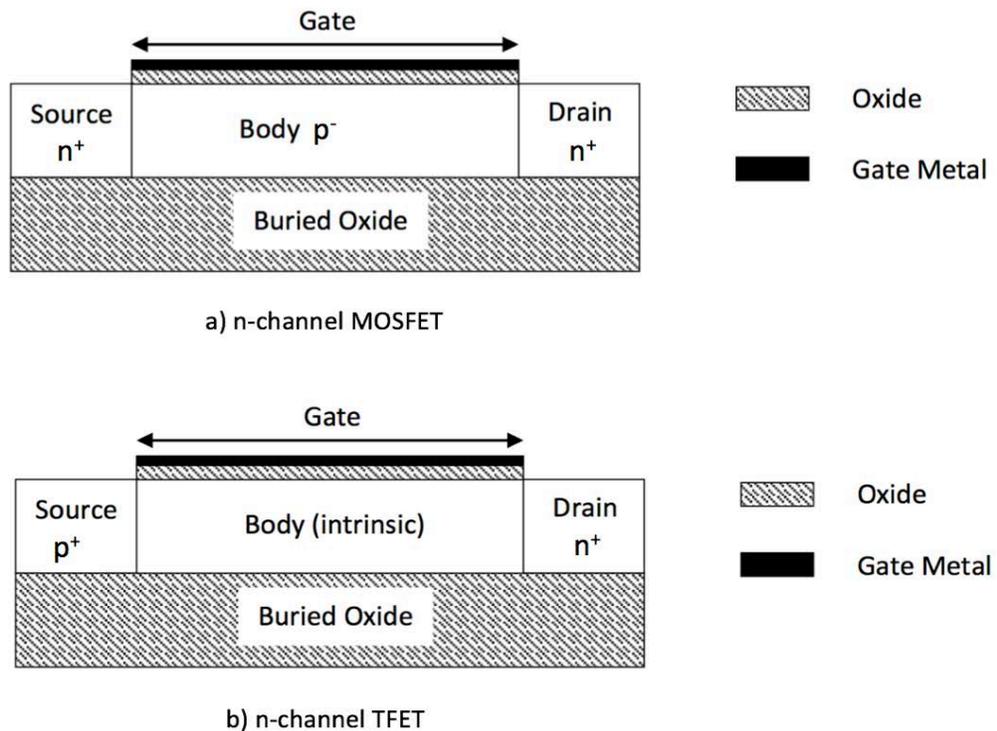


Figure 1.1. Basic structure of an n -channel MOSFET and TFET consisting of an p^+ source, n^+ drain for the TFET and an n^+ source, n^+ drain for the MOSFET, from Mamidala [1].

1.2 Operating principle

The n -TFET uses a gate-controlled tunnel junction to inject electrons from the source valence band to the channel conduction band. The operating principle of the n -TFET for off and on states is shown in Fig. 1.2. In the off state, Fig. 1.2(a), there is a potential barrier with thickness equal to the gate length and energy exceeding the band gap between the source and the channel suppressing direct tunneling and thermionic emission currents in the off state. The work function of the gate metal can be chosen to set the threshold voltage and deplete the channel at zero gate voltage. In the on state, Fig. 1.2(b), the gate voltage controls the tunneling window and sets the on-current. An analytic expression for the subthreshold swing in the TFET has been derived by Zhang [2]. The earliest reports that sub-60-mV/decade subthreshold swing was possible in the TFET were published by Wang [3], Bhuwarka [4], and Appenzeller [5].

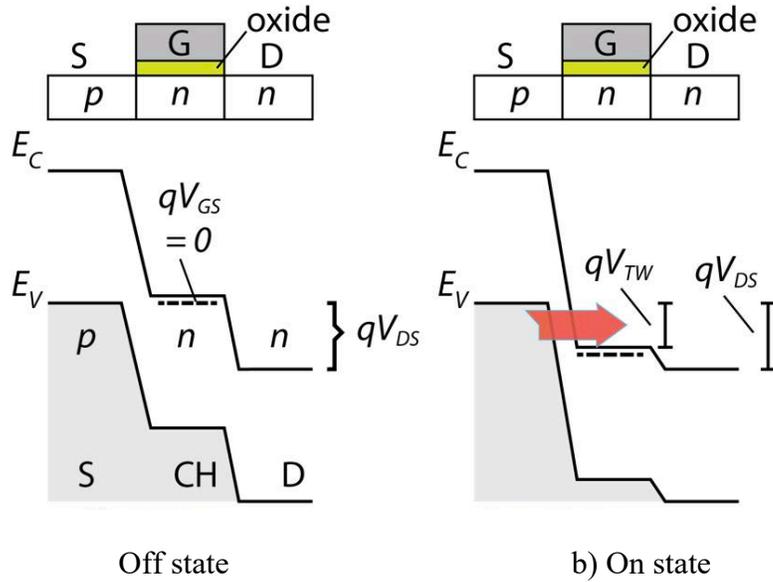


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1.3 Band-to-band tunneling

Band-to-band tunneling (BTBT) is the current control mechanism in the TFET. BTBT happens in a p^+n^+ junction when the valence band of one side of the junction overlaps energetically with the conduction band of the other side of the junction, therefore enabling carriers to tunnel through the barrier, Fig. 1.2(b). In this mechanism, the electrons travel from the valence band to the conduction band or vice versa in a p -TFET through the forbidden energy band gap.

1.4 Why TMD TFETs

Besides the limitation of subthreshold swing, MOSFETs suffer from the short channel effect, drain-induced barrier lowering [6]. TFETs demonstrate a better immunity to this short channel effect [1]. Atomically thin layered materials, due to their intrinsic scalability to different thicknesses from mono to multilayers can be an exciting alternative to traditional semiconductors. Among layered materials, TMDs with tunable band gap structure are promising candidates for demonstration of TFET behavior. Atomically thin TMD material-based TFETs result in strong electric field at the source-channel junction due to tight gate control over the channel and leads to subthreshold swing smaller than 60 mV/decade [7]. TMD materials are composed of one transition metal atom placed in between two atoms from the chalcogenide group with a molecular formula of MX_2 where M stands for the transition metal atom such as Mo, W or other transition metals and X is a chalcogenide atom like S, Se, and Te. TMD layers are weakly bound together by Van der Waals forces and each layer has strong covalent in-plane bonding. Because of the weak bonding between layers, these materials can be easily exfoliated into two-dimensional layers.

Thinning 3D materials such as Si leads to an increase in surface roughness that affects the threshold voltage and carrier transport [8]. In Si *n*MOS <100>, a 28% thickness decrease (3.5 to 2.5 nm) results in 440% increases in threshold voltage (0.05 to 0.22 V); it is due to impact of surface roughness and the fact that threshold voltage has Δ_{rms}^2 dependency [8]. TMD materials due to weak van der Waals forces between the layers can be exfoliated to thin layers without surface roughness [9] and form a surface free of dangling bonds. TMD materials have variable bandgap and decreasing the thickness of a

TMD materials result in a larger bandgap, but the increase in band gap is not as significant as in quantized III-V materials, because the effective mass of TMD materials is generally large with respect to III-V materials [10]. As an example, thinning InAs nanowires increases the bandgap more than 100% [11], but for TMD such as MoS₂, thinning from bulk to monolayer results in less than 50% increase in bandgap and for WSe₂, less than 34% and it is simply related to effective mass and can be understood from simple particle-in-a-box quantization [10]. Monolayer 2D materials usually have small dielectric constants and since the scaling length is proportional to square root of dielectric constant of TMD materials [7] that can increase the on current by decreasing the scaling length. Kumar and Ahluwalia reported the in-plane dielectric constant for bulk WSe₂ is 8.7 and thinning it to monolayer results in low 2.9 dielectric constant [12].

1.5 TMD material preparation

Most previous studies of TMD materials have used a tape transfer approach to exfoliate single or multilayer crystals onto an SiO₂ oxide on Si, similar to the original work of Novoselov and Geim on graphene [13]. Mechanical exfoliation, due to its simplicity and the high crystallinity of the final materials, has been a popular approach for preparation of atomically thin and few layer materials for device investigation. However, domain sizes are typically on the order of tens of square microns in area. The domain size is limited to under approximately 1 μm^2 , which limits the size of circuits that can be constructed. The 2D sheets or flakes are typically randomly distributed across the surface of an oxidized Si wafer, with each differing in layer thicknesses. This makes design of experiments with systematic variations difficult to examine and this approach is not suitable for batch

fabrication. Therefore, developing reliable synthesis techniques for 2D materials is desired for manufacturing. Synthesized TMD materials are now a primary focus of many researchers [14]. Advances in these materials are summarized in many reviews [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25]. Synthesis of WSe₂ has been reported via powder vaporization [26], pulsed laser deposition [27], molecular-beam epitaxy (MBE) [28], and metal organic chemical vapor deposition (MOCVD) [29].

The WSe₂ materials in this research were grown by MOCVD at Penn State in Prof. Joshua Robinson's group. The process is generally run on 1 square centimeter few-layer films grown on sapphire. Sapphire is the substrate of choice for growth in this study since it is commercially viable [30] and it has a chemically robust surface compatible with the harsh environments required for synthesis of TMDs [31, 32].

1.6 Gate oxide deposition on TMD materials

Uniform deposition of high-k dielectrics such as Al₂O₃ or HfO₂ on TMD crystals is challenging because the surfaces are fully terminated and oxides do not form readily on surfaces where there are no dangling bonds. Several studies show the problems associated with the lack of dangling bonds on TMD surfaces [33, 34, 35]. So, there should be a surface preparation and nucleation step prior to atomic layer deposition (ALD) otherwise surface without treatment leads to formation of islands on 2D materials instead of continuous film [33, 36].

There are several successful reports of gate oxide ALD on TMDs [37, 38, 39]. Recently, surface functionalization of 2D materials with oxygen plasma or ultraviolet ozone is demonstrated to promote the reactivity of the surface. Azcatl found that a UV-O₃

pretreatment in MoS₂ removes adsorbed carbon contamination from the 2D material surface and leads to formation of a weak sulfur-oxygen bond without evidence of molybdenum-sulfur bond disruption [37]. In addition, the oxygen-terminated surface can be ideal for ALD process since oxides such as Al₂O₃ can be deposited uniformly on it. Similar to this method, Yang was able to deposit 6.6 nm Al₂O₃ on MoS₂ by applying a remote oxygen plasma pretreatment prior to ALD. It is demonstrated that oxygen species in ultra-low energy plasmas are physically adsorbed on the MoS₂ surface without making the flakes oxidized [39]. Also, Lee and Cheng reported using ozone instead of water as the oxidant in ALD to provide uniform formation of Al₂O₃ deposition on 2D materials, in contrast to the incomplete coverage while using trimethyl aluminum (TMA) and H₂O as precursors [40, 38]. Zou explored utilizing an ultrathin metal oxide such as Al₂O₃, Y₂O₃ and MgO as a buffer layer between HfO₂ ALD on exfoliated MoS₂ to achieve a conformal, high quality interface with minimal interface defects, $2.3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ [41].

Recently, polymer based layers such as titanyl phthalocyanine (TiOPc) have been used as a seeding layer to form nucleation on TMDs like WSe₂ for ALD growth [42, 43]. In this method, a thick layer of TiOPc was deposited on WSe₂ in an MBE system. Subsequently, the thick multilayer was heated and a flat-lying TiOPc monolayer was formed. ALD pulses of TMA and H₂O nucleate on the TiOPc, resulting in a uniform deposition of Al₂O₃. Using this method, 3 nm EOT Al₂O₃ was deposited on WSe₂ and resulted in low leakage current, 0.046 pA/ μm^2 at 1 V gate bias [42].

Low temperature nucleation following by ALD deposition of a high quality oxide is another approach for oxide deposition on 2D materials [44]. Park reported directly deposited of Al₂O₃ on highly ordered pyrolytic graphite (HOPG) surfaces by low

temperature thermal ALD using TMA and H₂O without any seeding layer at 50 °C. Short purge times (500 ms) between the two precursor pulses and long pulse of TMA precursor (600 ms) was considered to form a CVD growth component. The CVD component provides nucleation sites on the surface and leads to formation of pinhole free Al₂O₃ film deposition on WSe₂. Liu and Azcatl reported it is necessary to reduce the temperature to 473 K to achieve a uniform 10 nm of Al₂O₃ deposition on MoS₂ [35, 37].

1.7 TFET contact resistance requirements

In order to unlock the full potential of TMDs, methods for formation of low resistance contacts to TMDs are needed. The on current in metal contacted TMD materials usually is limited by the presence of a Schottky barrier (SB) [45, 46, 47, 48]. In Si-based devices, selective ion implantation by changing the carrier density of the contact region, is one of the methods to achieve low-resistance ohmic contact.

However, due to the ultrathin body in TMD materials, traditional ion implantation doping method on 2D materials is not applicable because for typically implant energies (>500 eV) the implantation depth exceeds the thickness of the 2D material. Moreover, ion implantation does not raise the surface doping so it is not applicable for TMD contacts.

Common ways to increase the current in a SB are to lower the contact barrier by the choice of metal and to increase the surface doping to raise internal electric field and increase the tunneling probability (field emission). Selecting proper metal plays a critical role in determining the Schottky barrier height. Metals with high work function are used to form a low barrier height on *p*-type semiconductors and metals with low work function are used to create low barriers on *n*-type semiconductors. Low work function metals such as

Ti, W, and In provide low electron SBs i.e. 0.33 and 0.35 and 0.47 eV, respectively, on WSe₂, while Pd with high work function can decrease the hole SB to 0.35 eV [49].

It is important to note that work function alone is not sufficient to form good contacts. In Schottky theory, depending on semiconductor bandgap, an extremely high work function or low work function metal can form an ohmic contact [49]. Therefore, doping the TMD materials (by impurity substitutional doping, charge transfer doping, ion doping, or other method) to achieve low contact resistance is required. The contact resistance should be less than approximately $R_C = V_{DS}/20I_{ON}$ to have no more than one tenth of V_{DS} dropping across both the source and drain contacts when conducting at I_{ON} . For $V_{DS} = 0.4$ V and $I_{ON} = 100$ $\mu\text{A}/\mu\text{m}$; this corresponds to a contact resistance of 200 $\Omega \mu\text{m}$. Assuming that the tunneling through the Schottky barrier controls the current of an ohmic contact, the Fowler-Nordheim tunneling current relation can be used to estimate the contact doping requirements. The Fowler-Nordheim current density can be calculated using [50]

$$J(F) = AF^2 \exp\left(-\frac{B}{F}\right) \quad , \quad (1.3)$$

where $A = \frac{m_0 q^3}{8h\pi m^* \Phi}$, $B = \frac{8\pi \Phi^{1.5} \sqrt{2m^*}}{3hq}$, where m_0 is the electron mass, m^* the tunneling effective electron mass, h is Planck's constant, and Φ the energy barrier height. Figure 1.3(a) shows the Fowler-Nordheim current density model vs. Schottky barrier heights typical on WSe₂ and using the WSe₂ effective mass of $0.5m_0$, where m_0 is the electron mass. For a barrier height of 0.2 eV and to achieve an ON current of 100 $\mu\text{A}/\mu\text{m}$ requires an electric field of 0.75 MV/cm. The required doping to achieve this field can be calculated from the electric field in a Schottky metal-semiconductor contact using

$F = \sqrt{\frac{2qN\Phi}{\epsilon_s}}$ [51], where ϵ_s the dielectric constant, and N is the doping in the semiconductor. A doping density of $4 \times 10^{18} \text{ cm}^{-3}$ is needed to meet the contact resistance requirement for an 0.2 eV barrier on WSe₂; this corresponds to a sheet carrier density of $4 \times 10^{11} \text{ cm}^{-2}$ to obtain a current density of $100 \text{ } \mu\text{A}/\mu\text{m}$ in a 1 nm film.

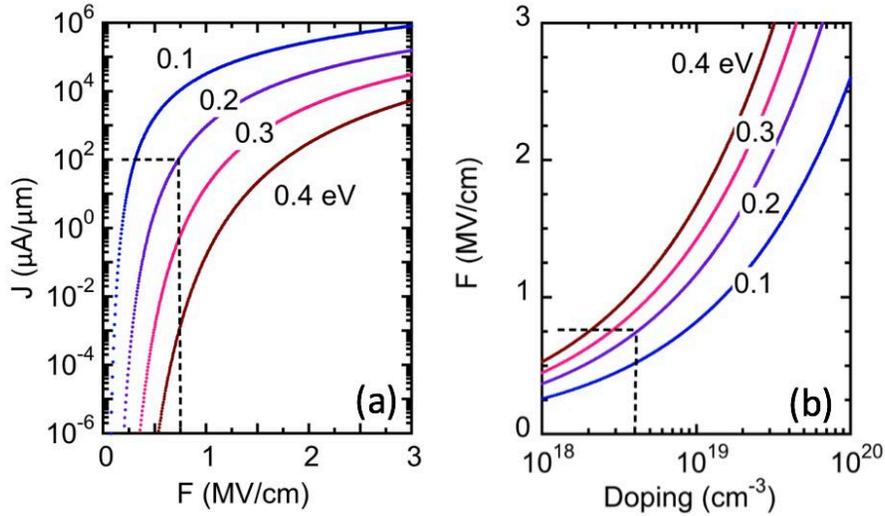


Figure 1.3. (a) Fowler-Nordheim current density vs. electric field for a metal-WSe₂ Schottky contact for four barrier heights, (b) Electric field vs. doping for four barrier heights. The dashed lines in (a) denote the electric field needed to support a current of $100 \text{ } \mu\text{A}/\mu\text{m}$ for a barrier height of 0.2 eV. In (b) the dashed lines indicate the doping needed to achieve the electric field indicated by the dashed line in (a).

There are many methods for doping TMD materials, such as charge transfer doping [45, 52, 53, 54], substitutional doping [55, 56, 57], electrostatic doping with gate electrodes [58], and electrostatic doping using electric double layers in solid polymers [59, 60, 61] and ionic liquid electrolytes [62, 63, 64, 65]. In this work, polyethylene oxide: cesium perchlorate (PEO:CsClO₄) is used as an overcoat layer to ion dope the WSe₂. This doping

approach allows sheet carrier densities as high as $3.5 \times 10^{13} \text{ cm}^{-2}$ on n -WSe₂/Ti/Pd contacts [61]. The ion doping mechanism using PEO: CsClO₄ is shown in Fig. 1.4.

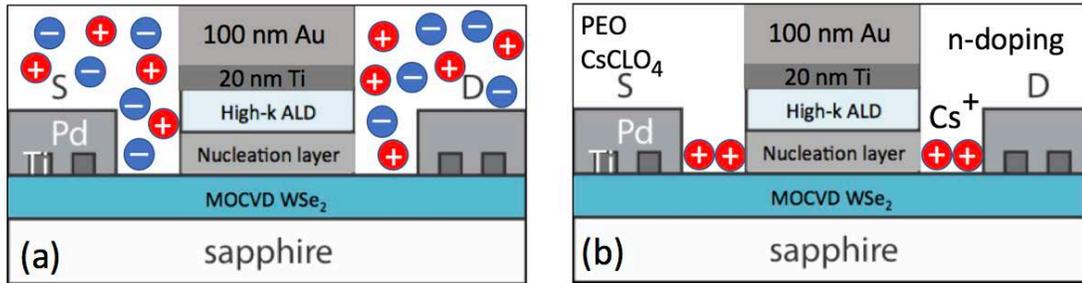


Figure 1.4. Schematic of ion doping using PEO: CsClO₄. (a) Before applying a bias, the ions are homogeneously distributed. (b) Applying positive voltage to side gate (not shown), drives Cs⁺ ions to the surface of WSe₂ and forms n -type doping in the channel.

In this method, by applying a potential on a side gate formed in the same metallization step as the source/drain (S/D) contact, a lateral electric field is established, depending on the polarity, either positive or negative ions are attracted to the surface of TMDs and stay about 1 nm away from the surface. At room temperature, the ions are homogeneously distributed in the electrolyte, Fig 1.4(a). Applying positive voltage to the side gate drives positive Cs⁺ ions onto the WSe₂ surface, which induces electrons in the channel and forms n -type doping. Rearrangement of the ions after applying voltage to field plate, forms electric double layers (EDLs) between PEO:CsClO₄ and multilayer WSe₂ FET that reduce contact resistance and provide doping for access region. Cooling the polymer electrolyte below a specific temperature (glass transition temperature (T_g)) decreases the polymer's segmental mobility to nearly zero [66]. Cooling the device below T_g locks the

ions and the fix transistor doping. The EDL approach can provide large sheet carrier densities in the range of 10^{14} cm^{-2} [67].

1.8 Analytic model for TFET

An analytic model for the TFET has been developed by Salazar [68]. This model describes the characteristics of atomically thin TMD TFETs and is applied here to a 1 monolayer WSe₂ semiconductor. Potential profile is obtained by considering 1D Poisson's equation and boundary conditions in each region, from source to channel. For predicting BTBT current, Wentzel–Kramers–Brillouin (WKB) approximation is used. Figure 1.5 shows the transfer characterization simulated for one monolayer top gated WSe₂ for different drain (source) doping at 0.5 V for drain-source voltage. Considering 0.65 nm channel thickness corresponding to 1 monolayer, 1.2 eV as band gap, and 1 nm EOT, subthreshold less than 60 mV/decade is achieved. Figure 1.5(b) shows the cross section of the simulated device. Current density more than $10 \text{ } \mu\text{A}/\mu\text{m}$ is achieved for doping higher than $5 \times 10^{19} \text{ cm}^{-3}$. Note this model does not include the Schottky metal-semiconductor contact. This analytical model is in good agreement with nonequilibrium Green's function simulations [69].

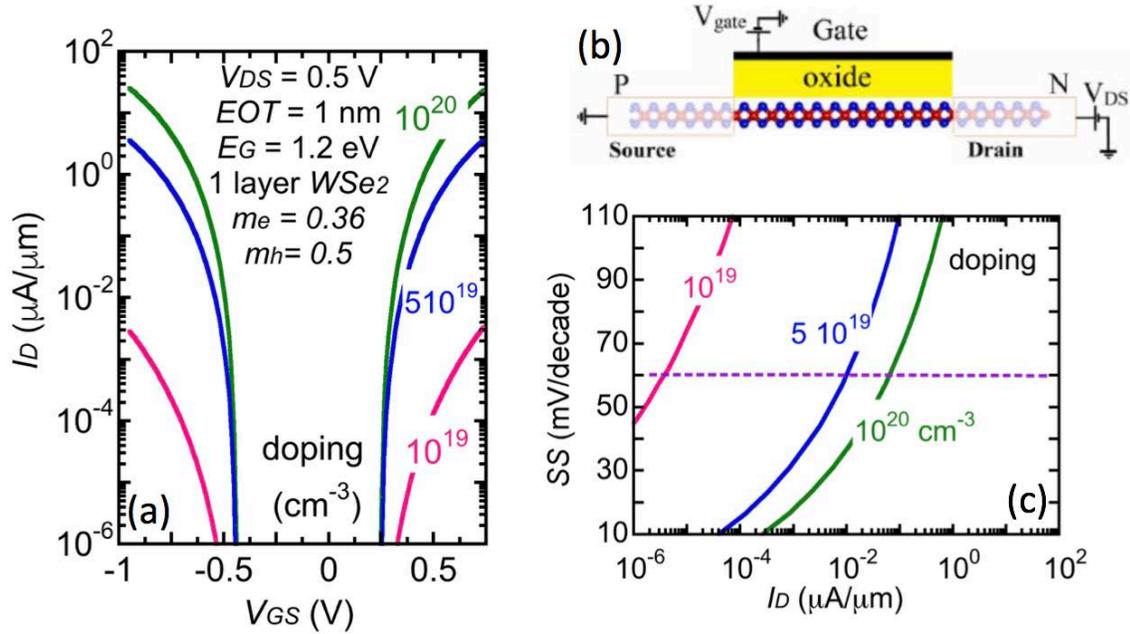


Figure 1.5. (a) Transfer characteristic for 1 monolayer top gated WSe₂ tunnel FET for different drain (source) doping, (b) Cross section of WSe₂ TFET used in simulation, (c) Subthreshold swing vs drain current density for three different doping indicating sub 60 mV/decade can be achieved in the WSe₂ TFET.

Figure 1.6(a) shows the transfer characteristics of the WSe₂ TFETs obtained from the simulator of Salazar using the same parameters as used by Ilatikhameneh in atomistic simulations of the WSe₂ TFET [70] shown in Fig. 1.6(b). The analytic and atomistic simulations are in reasonable agreement.

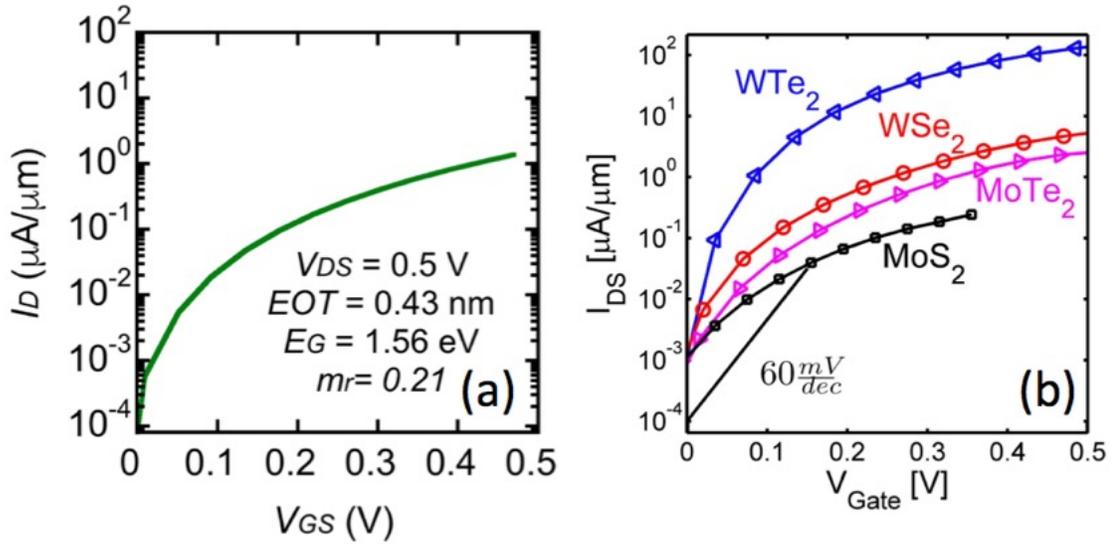


Figure 1.6. Transfer characteristics of WSe_2 FET using analytic simulator of Salazar [68], (b) atomistic simulation for different TMD materials from Ilatikhameneh [70].

In this thesis, I have developed a stepper-based process for FET and TFET fabrication on synthesized MOCVD WSe_2 . In chapter two, physical characterization of MOCVD WSe_2 is discussed to address some of the problems that were solved. I was able to carefully study the surface of MOCVD WSe_2 samples using particle analysis techniques from atomic force microscopy (AFM) measurements and provide feedback to the grower. As a result, we were able to decrease density of agglomerates to less than $0.1 \times 10^8 \text{ cm}^{-2}$. A 4-mask level process was designed to enable fabrication of 240 devices on a $1 \times 1 \text{ cm}^2$ MOCVD WSe_2 -on-sapphire wafer. The use of a stepper-based mask set is not notable for common semiconductor device fabrication but has not been reported for 2D materials where single device fabrication on exfoliated flakes is typical. This process was subsequently refined when it was discovered that a thick S/D metallization (180 nm Pd)

tended to cause the WSe₂ to detach at the metal/channel edge, apparently due to strain in the metal. In order to solve this problem, an additional mask was introduced to break the S/D contacts formation into a two-step process allowing first a thin metallization (40 nm) followed by a thick metal to support the pads for probing.

In chapter three, the development of a two-step thermal ALD process is described, which consisted of a low-temperature ALD at 110° C followed by a high-temperature ALD at 200°C at Notre Dame. In this study, the effect of key parameters (pulse and purge times for each precursor, deposition temperature, and deposition rate) were investigated to establish conditions suitable for ALD nucleation on WSe₂. A conformal oxide deposition on WSe₂ was established.

Chapter four summarizes the demonstration and characterization of top-gated field-effect transistors (FET) fabricated using a the 5-mask process on few-layer CVD WSe₂-on-sapphire. Three transistor structures were studied; transistors in which gate overlaps the S and D contacts and two transistors with open access regions to allow ion doping using PEO:CsClO₄ to induce electron and hole conductivity in access regions and allow characterization of the FETs.

Chapter five highlights accomplishments and findings. Finally, a few remarks are provided to set the stage for future investigations.

CHAPTER 2: WSe₂ FIELD-EFFECT TRANSISTOR

Two-dimensional material growth is still in an early stage of development. In this chapter, physical characterization of WSe₂ materials is discussed to illustrate some of the technical problems solved during the course of this investigation. The WSe₂ channel materials utilized here were grown at Pennsylvania State University by MOCVD. Our collaborator at Penn State, postdoc Sarah Eichfeld reported first growths of WSe₂-on-sapphire in 2015 with equilateral triangular grain size with side lengths of 8 μm [29] at 800°C growth temperature, 700 Torr and Se to W ratio of 20000. They characterized WSe₂ on sapphire by Raman spectroscopy, AFM, scanning electron microscopy (SEM) and cross-sectional transmission electron microscopy (TEM). In the first ~2 years (2014-2016) of the development at Penn State, Sarah Eichfeld led the reactor development and growth effort; in the past ~3 years (2016-2019) this responsibility transferred to postdoc Bhakti Jariwala. In 2018, Penn State reported continuous and conformal WSe₂ growth on sapphire characterized by photoluminescence and scanning tunneling spectroscopy and demonstrating high quality of mono-to-trilayer WSe₂ with low defect density of $8 \times 10^{11} \text{ cm}^{-2}$ [71]. This defect density was less than the defect densities reported on MBE-grown WSe₂, $2.8 \times 10^{12} \text{ cm}^{-2}$, and mechanically cleaved WSe₂ crystals, $1.2 \times 10^{12} \text{ cm}^{-2}$ [71].

The Penn State MOCVD system was custom built and is shown in Fig. 2.1. The system consists of a vertical, cold-wall reaction chamber that is heated by induction. The system is capable of reaching temperature between 100-950 °C and pressures between 1 and 760 Torr. The deposition substrates can be as large as 18 x 18 mm².

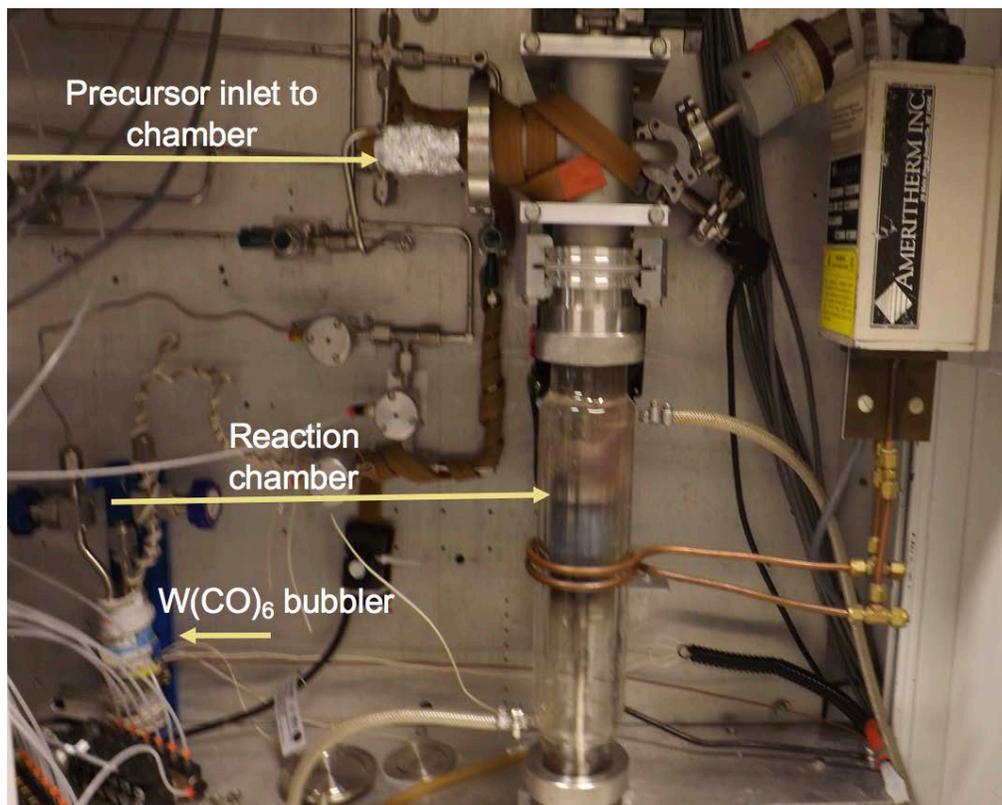


Figure 2.1. Penn State MOCVD system used for growth of WSe₂ used in this work.

The precursors used for WSe₂ growth in this system are hydrogen selenide H₂Se and tungsten hexacarbonyl W(CO)₆. Extremely high ratios of Se to W e.g. 20000, are needed to initiate nucleation and to obtain stoichiometric films. The precursors W(CO)₆ and H₂Se are introduced through two bubblers. The bubblers are kept at room temperature

with pressures of 700 and 760 Torr, respectively. Hydrogen and nitrogen are used as carrier gases. Figure 2.2(a) shows the WSe₂ growth reactor. The sapphire substrate is placed in the center of the chamber as shown in Fig. 2.2(b) and then heated to the nucleation temperature (400-550 °C) for a short time (2-3 minutes). After the nucleation step, the temperature is ramped up to the growth temperature (700-900 °C) while maintaining a Se overpressure in the chamber to avoid formation of Se vacancies. Upon reaching the growth temperature, the W precursor is reintroduced to the chamber.

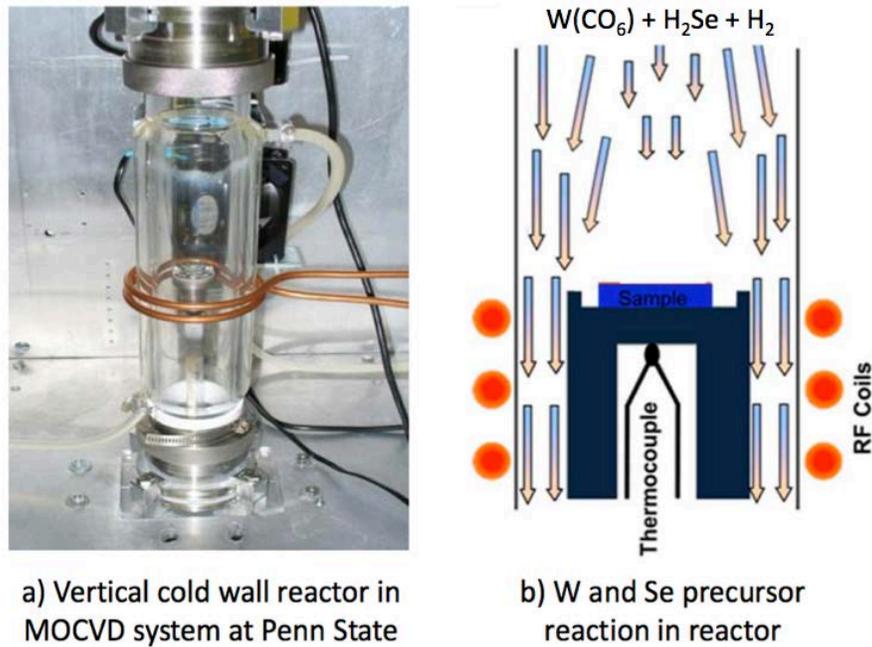


Figure 2.2. (a) Photograph of the Penn State cold-wall MOCVD reactor and (b) schematic of the growth substrate and reactor flows during WSe₂ growth, from Eichfeld [29].

The received WSe₂ wafers from Penn State were characterized using AFM as the first step before starting device fabrication. AFM was used to assess the surface flatness and continuity of the WSe₂ and to see whether packaging and transport from Penn State to Notre Dame had introduced contamination. A particle-free surface without features that could protrude through a gate oxide is crucial to achieve. Wafers were shipped from Penn State to Notre Dame in a vacuum-sealed poly bag to prevent air exposure and oxidation. These wafers were fixed in a polypropylene wafer tray with a spider spring to avoid movement and scratching.

2.1 Surface study of received MOCVD WSe₂ wafers from Penn State using AFM

Particle analysis is a powerful feature of the Bruker Dimension Icon AFM at Notre Dame. Protruding features were found in early growths from Penn State and these were automatically quantified in the AFM by counting the number of features with height taller than a specific threshold height. The counting algorithm in the AFM is able to distinguish multiple features in a given area if the area has multiple heights, Fig 2.3. The algorithm used for data extraction provides the minimum, maximum, and mean values for the height, diameter, and area of the particles. This analysis was performed in a 2.5 x 5 square micron area unless indicated which is comparable to the size of fabricated transistors.

To assess wafers sent from Penn State, at least three AFM images in different regions were made on each WSe₂ wafer to have a representative sampling. Figure 2.4 shows as-received AFM images for MOCVD WSe₂ grown on sapphire on early growth runs from Penn State. It shows measurements on 7 wafers received in 2016 from Penn State. Scan area for all of the images is 5 x 2.5 μm² except M165 that is 10 x 5 μm².

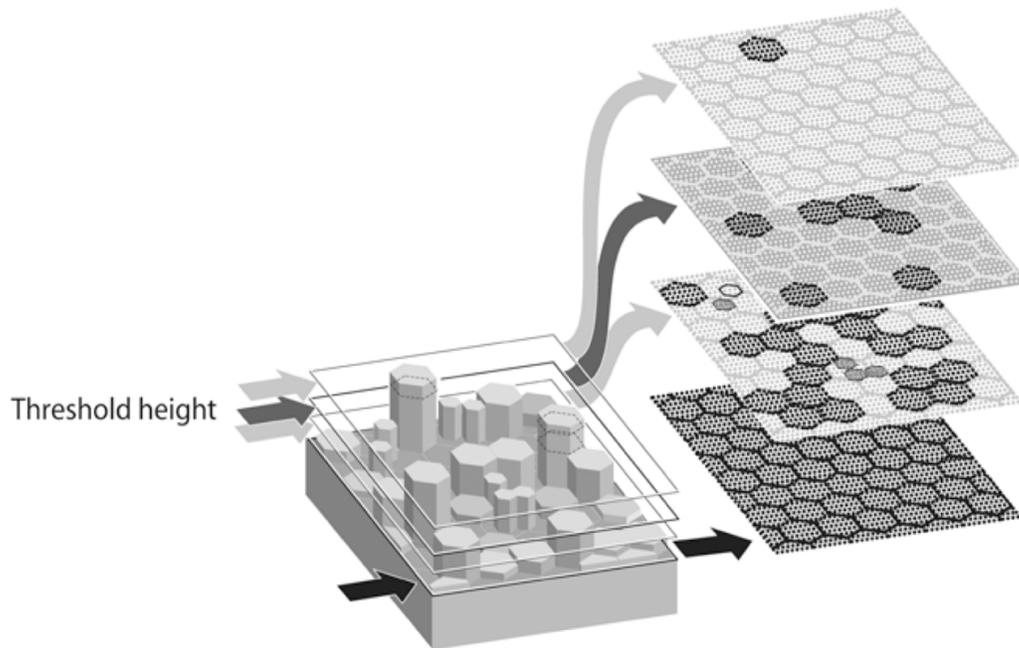


Figure 2.3. Particle analysis using the Bruker Dimension Icon AFM. The threshold height can be set to enable counting of particles with different heights and measurement of their lateral area. Image from DIMENSION iCON with ScanAsyst Instruction Manual 004-1023-000.

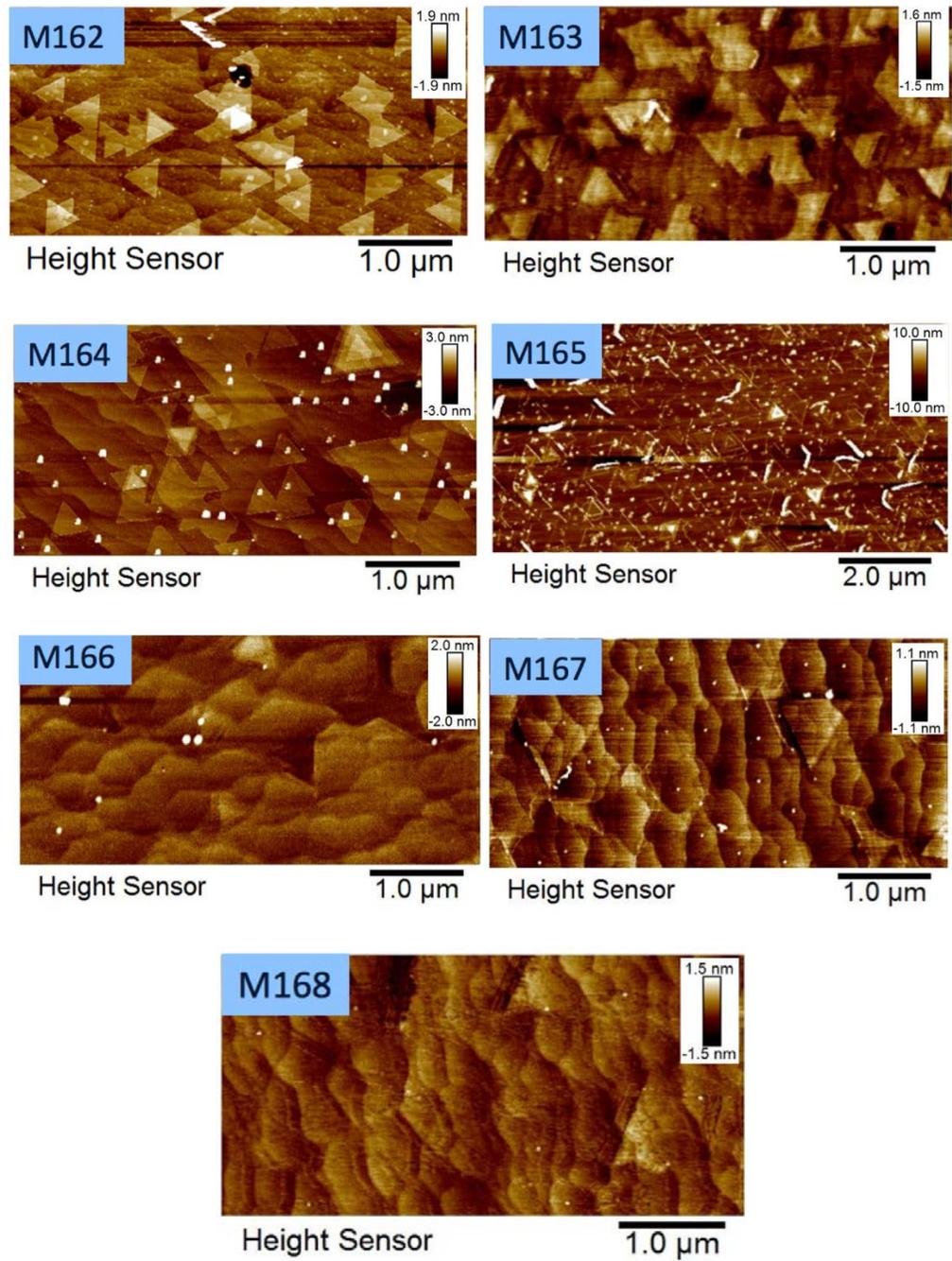


Figure 2.4. AFM images of as-received MOCVD WSe₂-on-sapphire from two growth sets of wafers. The first set is labeled M162 to M165 and second set is labeled M166 to M168.

The first set of wafers, M162 to M165, were grown at 750 °C with Se to W ratio of 28K, while there are some other differences in the details of growth such as post growth annealing condition, precursor flow rate, and growth time that are shown in Table 2.1 (in black). For the second set, M166 to M168, the Se to W ratio was 24,000 and they were grown for 30 minutes. Post growth annealing for 10 minutes was performed with 30 seconds W precursor flow prior to starting the growth as a surface preparation step. The preparation, growth, and post growth details are summarized in Table 2.1 for each wafer.

TABLE 2.1.

GROWTH DETAILS FOR THE FIRST AND SECOND SETS OF WAFERS
RECEIVED IN SEPTEMBER AND OCTOBER 2016 FROM PENN STATE.

Set #	Sample number	Se to W ratio	Growth temperature (°C)	Growth time (Minutes)	W-flow prior to growth	Pre growth annealing condition	Post growth annealing condition
Set 1	M162	28K	750	70	Yes 10 seconds	No annealing	10 minutes at 900°C
	M163	28K	750	90	Yes 10 seconds	No annealing	10 minutes at 900°C
	M164	28K	750	70	No	No annealing	10 minutes at 900°C
	M165	28K	750	70	No	No annealing	No annealing
Set 2	M166	24K	750	30	Yes 30 seconds	10 minutes at 900°C	10 minutes at 900°C
	M167	24K	800	30	Yes 30 seconds	10 minutes at 900°C	10 minutes at 800°C
	M168	24K	800	30	Yes 30 seconds	10 minutes at 900°C	10 minutes at 800°C

Particle analysis was used for surface evaluation and threshold height was set at 2 nm for feature height. These features or agglomerates are indicated as white shapes in the AFM images in Fig. 2.4. Comparing the two sets from Fig. 2.4, the first set of wafers shows many larger particulates compared to the second set. Small AFM scale bar (<2 nm) in second set shows smooth surface for WSe₂. As an example, the height scale profile for the AFM image of M168 wafer is in the range of ± 1.5 nm indicating a smooth surface with RMS roughness of 0.21 nm that it is consistent with the growth of 1 to 2 monolayers of WSe₂ on sapphire. Maximum root mean square (RMS) roughness of 0.28 nm is obtained over the scan for the second set while it is 2.8 nm for first set. The highest number of features are related to M165 wafer in the first set showing significant agglomerates distributed on the surface and the edges of triangle shape WSe₂.

One of the major differences in the growth of these two sets is the pre-growth annealing condition used in the second set. The pre-annealing step at higher temperature such as 900 °C acts as a surface treatment on the sapphire surface and promotes Se passivation of the sapphire, leading to a continuous WSe₂ growth. Annealing leads to the reconstruction of the surface resulting in terracing and regular atomic steps that improves the nucleation layer formation on sapphire substrate and decrease particulates significantly on the surface [71]. Considering M165 wafer with no pre- and post-annealing, this surface shows the formation of many particulates. Tungsten precursor flow prior to growth results in less agglomerate formation.

The number of particulates for the two growth sets is counted by the particle analysis software in the AFM and reported in Table 2.2. The table summarizes attributes of the protruding features in the AFM images shown in Fig. 2.4 including the number of

features with height exceeding 2 nm, the minimum height, the maximum height, the minimum diameter, and the maximum diameter. In the particulates' column, where there were multiple 2.5 x 5 square micron scans in different regions, a common separates this data. The data on heights and diameters are the extremes of the measured values across the measurement sets.

TABLE 2.2.

PARTICLE ANALYSIS USING BRUKER DIMENSION ICON AFM FOR MOCVD
 WSe₂-ON-SAPPHIRE GROWN AT PENN STATE IN 2016.

Set #	ND #	PSU #	Rec. Date	All Particulates 10 ⁸ /cm ²	Best Height >2 Min (nm)	Best Height >2 Max (nm)	Best Diameter Min (nm)	Best Diameter Max (nm)
Set 1	M162	B090816B	15-Sep	1, 3.2, 2.8, 6, 7, 17	2	10	11	221
	M163	B090916B	15-Sep	0.3, 0.9, 2.7	2	29	22	97
	M164	B090916C	15-Sep	12, 7, 3	2	19	11	226
	M165	B091116B	15-Sep	13, 24, 31, 31	2	66	11	306
Set 2	M166	B100116B	17-Oct	0.2, 0.6, 0.1	2	4	15	31
	M167	B100716B	17-Oct	1.7, 1.8, 10, 18	2	9.8	11	127
	M168	B100716C	17-Oct	0.1, 0.2, <0.1	2	2	11	11

By optimizing the growth condition in the second set, the density of agglomerates decreased to less than $0.1 \times 10^8 \text{ cm}^{-2}$ for M168 wafer and this was considered to be low enough density to yield devices. For a channel area of $5 \times 2 \text{ }\mu\text{m}^2$, less than 1 particle in $10 \text{ }\mu\text{m}^2$ is needed to deposit a gate dielectric without a defect. It means particulates should be less $0.1 \times 10^8 \text{ cm}^{-2}$. For the rest of the WSe_2 wafers (after M168) the number of particles was lowered to less than $0.1 \times 10^8 \text{ cm}^{-2}$ similar to AFM image in M168 wafer, shown in Fig. 2.4. Therefore, they were suitable for FET and TFET device fabrication on WSe_2 surface.

2.2 First approach for FET and TFET stepper process flow

In the 4-mask level process, alignment mark formation is the first step in fabrication. The surface is patterned with photoresist using an Autostep 200 i-line stepper for patterning prior to metal deposition. The marks act as alignment for the next lithography steps: channel mesa etch, S/D, and gate. Next, WSe_2 substrate is selectively etched using a Plasma-Therm 790 parallel-plate reactive ion etching system to isolate the devices and expose the sapphire substrate to anchor the S/D contacts. Then, thick metal, $\sim 180 \text{ nm}$, was deposited for contacts. The channel and contact masks align to the alignment layer mask. The next critical step is oxide deposition on WSe_2 followed by electron beam deposition used for gate metal deposition. The process traveler for the gate last process is given in Appendix A.

A cross section of the process flow is shown in Fig. 2.5. The alignment mark and channel formation steps are not shown, and process flow starts with contact formation. Thin Ti (0.8 nm) followed by 180 nm Pd metals for contacts were deposited using electron-

beam deposition, Fig. 2.5(a). Low temperature CVD-like Al_2O_3 oxide was deposited as a nucleation layer following by 10 nm Al_2O_3 ALD in an Oxford Flexal ALD system. Then, Ti/Au (20/80 nm) as a gate metal was deposited using FC1800-1 electron beam evaporator, Fig. 2.5(b). FET characterization were performed in this state. In order to complete the TFET, the bilayer oxides needed to be removed in the access regions, labeled L_A in Fig. 2.5(b) to allow the drop casting of PEO: CsClO_4 which is used to dope the channel and form the source/channel p - n junction.

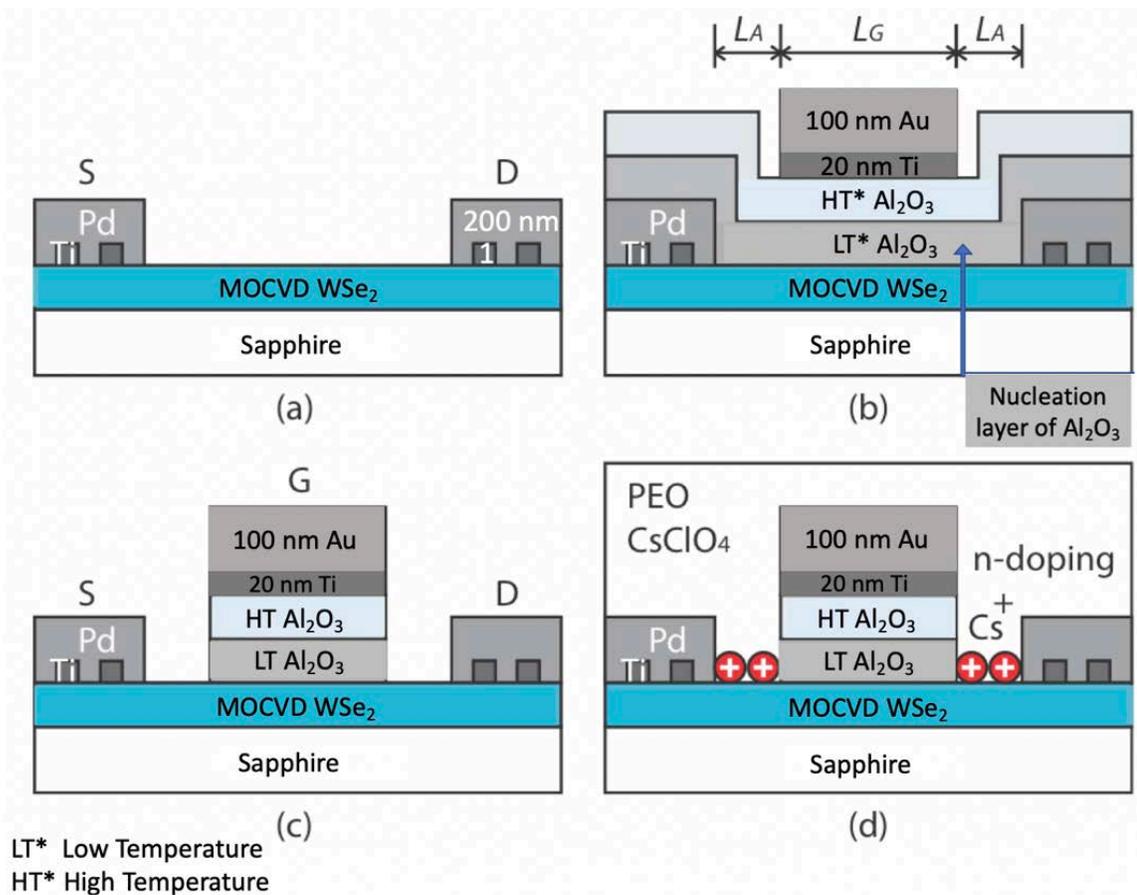


Figure 2.5. WSe_2 TFET stepper process flow cross section in first mask set. (a) Source/drain contact consisting of sub-nanometer Ti followed by 180 nm Pd, (b) Gate formation on 1.1 nm Al_2O_3 nucleation layer at low temperature followed by 10 nm Al_2O_3 ALD bilayer at 200 °C (L_A and L_G are the access regions and the gate length, respectively). (c) Oxide etching of access region using buffered HF at room temperature. (d) PEO:CsClO₄ drop cast and annealed at 90 °C for 3 minutes. The ion Cs^+ is driven to the channel surface by an adjacent field plate electrode (not shown). The doping configuration shown is that needed for testing of an n -MOSFET.

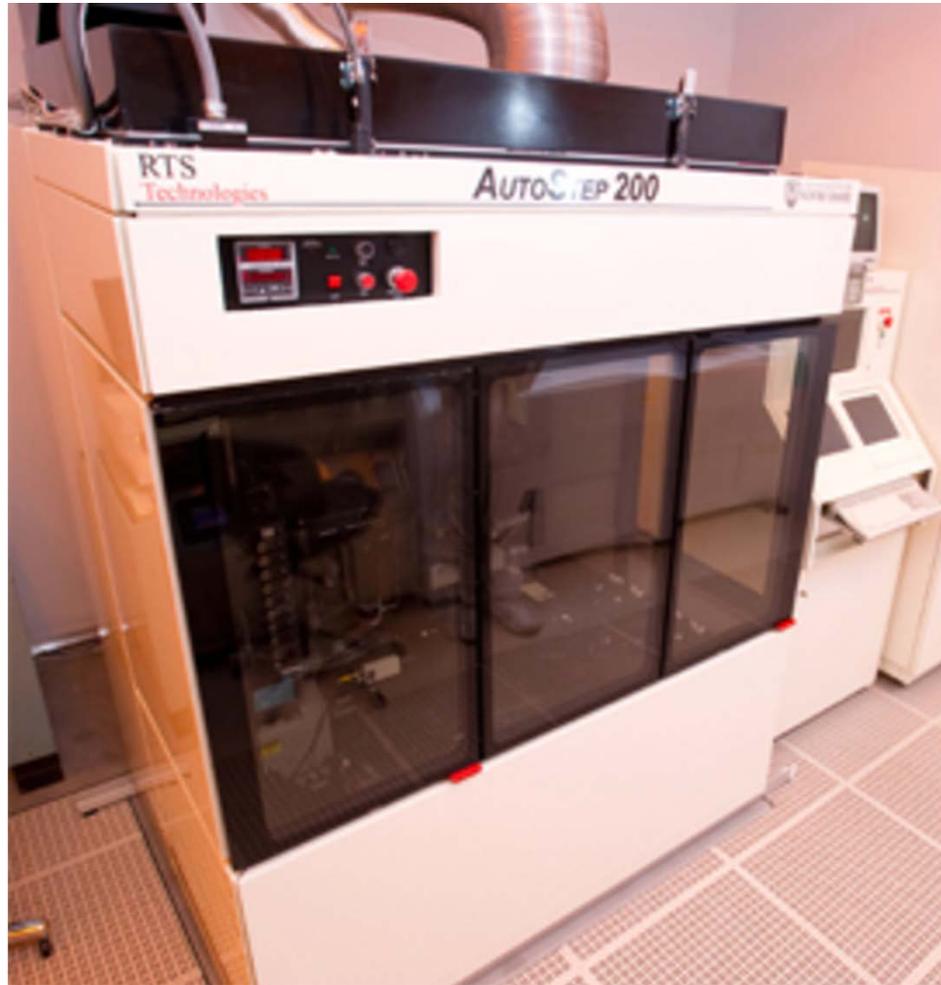


Figure 2.6. Autostep 200 i-line lithography stepper at the University of Notre Dame.

An Autostep 200 i-line lithography system with 5x reduction is used for patterning, see Fig. 2.6. It can process 4" wafers or wafers as small as 1 x 1 cm². The stepper uses a 700 W Hg arc lamp to produce 365 nm light at a typical intensity of 275 mW/cm². Optical lithography is much faster than electron beam lithography (EBL). As a comparison, a wafer could be patterned in 5 seconds using optical lithography while the same wafer takes approximately 4 hours by EBL.

2.3 First approach TFET mask set

The original TFET mask set in this research was designed by graduate student, Sushant Sabnis, but was modified extensively in the first approach design shown in Fig. 2.7. The transistors in the mask set are long channel devices with minimum 1 μm gate length and they are all top gated. There are two types of transistor designs, transistors with gate overlap and without gate overlap (with access region). There are 1 and 2 μm access regions for the transistors without overlap. In both designs, the gate width is 8 μm while gate length is changing from 1 to 5 μm with 1 μm step. In another set of transistors, variable gate widths as 2, 4, 8, 16, 20, 32 μm are provided for transistors with 2 μm access region to confirm channel width dependence. A side gate is considered for all of the transistors with 15 μm width and 6 μm distance from the of gate. There are two kinds of capacitance-voltage ($C-V$) test structures: with and without overlap. Different diameters (130 to 170 μm diameter with 10 μm step) were constructed for measuring the capacitance on WSe_2 . The Corbino disk with similar geometry as $C-V$ structures are designed for contact resistance measurement. The TLM structure is also used to determine the contact resistance and sheet resistance between the metal and WSe_2 . The separation between the contacts are 2, 4, 8, 16, 32, 64 μm with 32 μm width. Table 2.3 summarizes FETs, TFETs, $C-V$ structures, Corbino disks, and TLM structures with the geometry and dimensions for each.

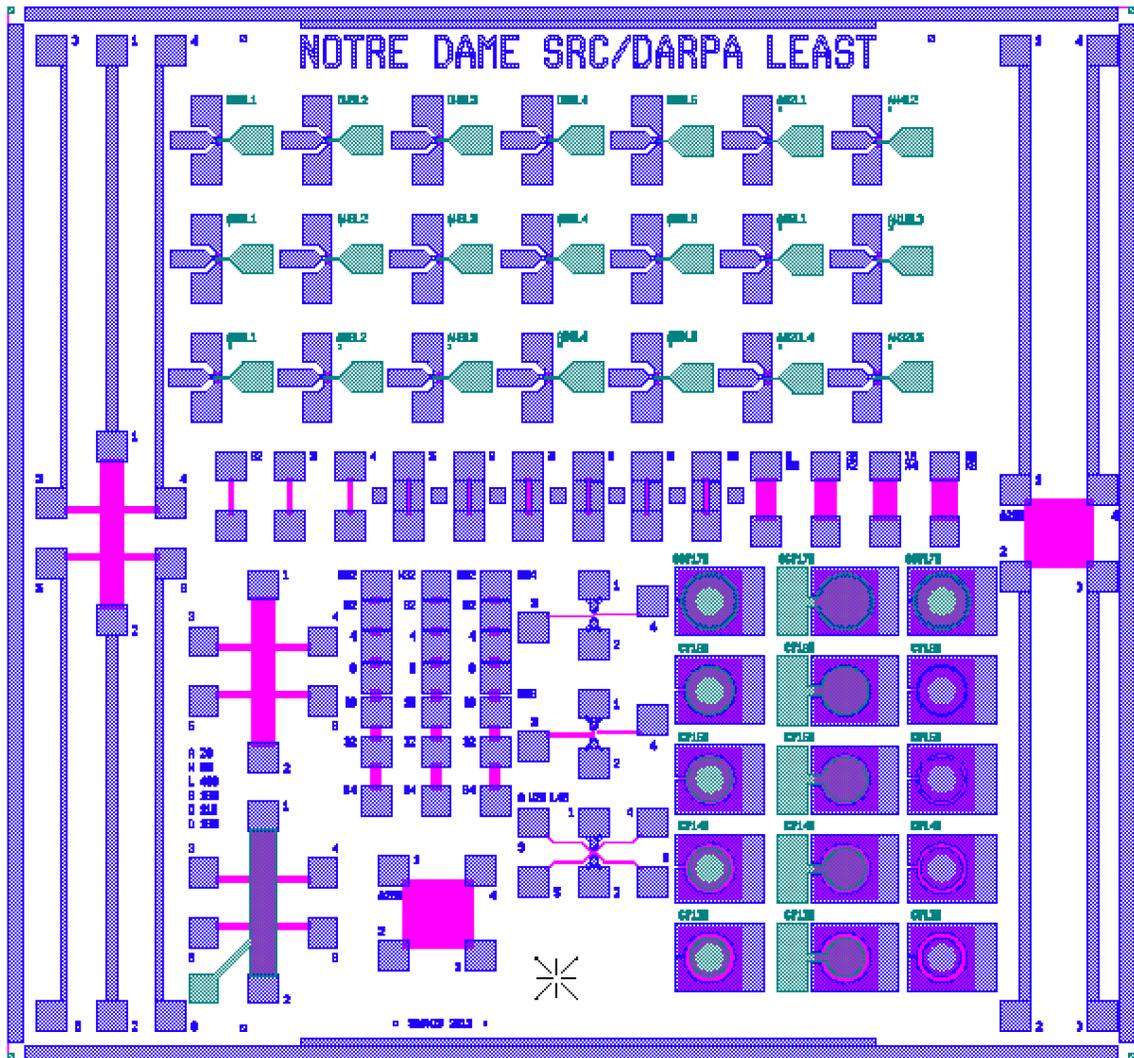


Figure 2.7. TFET stepper mask, $3.6 \times 3.8 \text{ mm}^2$, 4-mask level. Each color is corresponding to different mask level; black, pink, blue, and green colors are indication of alignment mark, channel isolation, S/D contact, and gate formation, respectively.

TABLE 2.3.

SUMMARY OF THE FET, TFETS, CV STRUCTURES, CORBINO DISKS, AND TLM STRUCTURES IN MASK SET WITH THEIR GEOMETRIES.

Device	Access region (μm)	Width (μm)	Length (μm)	Contact overlap with mesa (μm)	Diameter (μm)
FET	0	8	1, 2, 3, 4, 5	10	-
FET & TFET	1	8	1, 2, 3, 4, 5	10	-
FET & TFET	2	8	1, 2, 3, 4, 5	10	-
FET & TFET	2	2, 4, 8, 16, 20, 32	4	10	-
3 CV structures	0	-	-	20 (minimum)	170
CV structures	5, 10, 15, 20	-	-	20 (minimum)	160, 150, 140, 130
CV structures	5, 10, 15, 20	-	-	20 (minimum)	160, 150, 140, 130 (minus 100 μm diameter area)
Corbino discs	5, 10, 15, 20	-	-	20 (minimum)	160, 150, 140, 130
3 TLM structures	-	32	2, 4, 8, 16, 32, 64	10	-

2.4 Reactive ion etching of WSe_2

Channel region definition is the second step in the fabrication process. It is done by dry etching of WSe_2 on sapphire using Plasma-Therm 790 reactive ion etching (RIE) with positive photoresist (Megaposit SPR700) as the etch mask. The etch uses SF_6 and Ar as chemical and physical etchants for etching WSe_2 , respectively. Using 100 W power with 250 V DC bias, and 25 mTorr pressure, an etch rate of 7 $\text{\AA}/\text{s}$ is expected [72]. Figure 2.8 shows a WSe_2 surface, that is etched successfully using the etch recipe as above with 15/10 sccm SF_6/Ar etchants for 10 seconds and the step height between the two different regions (WSe_2 channel and sapphire) is consistent with the expected thickness of the grown WSe_2 on sapphire, about 2 nm.

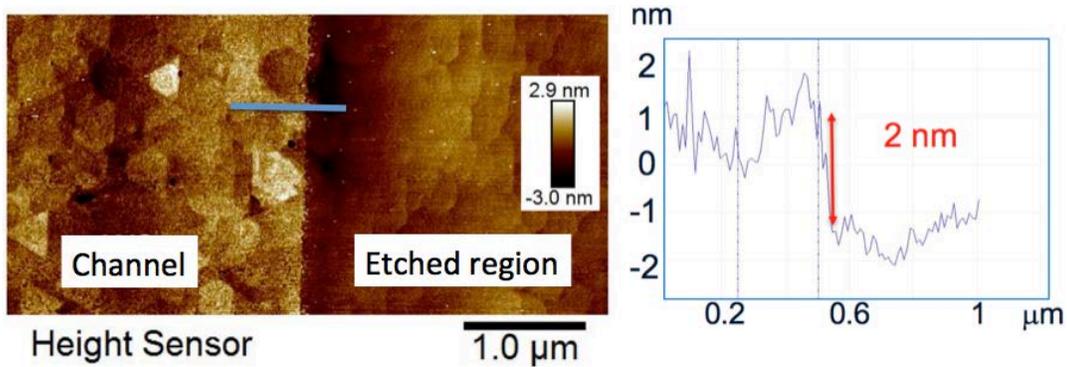


Figure 2.8. AFM image of MOCVD WSe₂ on sapphire substrate with line scan after dry etching in RIE system using 15/10 sccm of SF₆/Ar etchants for 10 seconds on wafer M179 in 5 x 2.5 μm² area.

2.5 Importance of contact anchoring

MOCVD-grown WSe₂ on sapphire is only weakly bonded to the sapphire substrate. This means that contact metallization that will be probed must be on the sapphire substrate and not on the TMD. Otherwise probing will delaminate the WSe₂. After mesa isolation to define the channel regions, the WSe₂ needs to be locked down to the sapphire by a metal to hold it in place during the subsequent processing. Figure 2.9 shows one of the insufficient mesa designs. In this design, a 20 μm width anchor region was opened to the sapphire at the perimeter of the contact pads and the central region of the metal contact was sitting on WSe₂. Although this design was effective for anchoring the contacts, probing any region except the 20 μm margins resulted in contact detachment upon probing. In retrospect, this is to be expected for a high quality multilayer 2D material. Figure 2.9 shows an optical microscopic image of a metallized contact pad on WSe₂. As shown in Fig. 2.9(a) the pads adhered properly on the sapphire in the 20 μm margin, but on probing of metal above the WSe₂ the pads ripped off. In the revised version of the mask, WSe₂ is etched

away from the wafer except in the channel region and the pads completely contact the sapphire. Figure 2.10 shows the difference between the previously design and the successful mesa design for a transistor with $8\ \mu\text{m}$ width, $1\ \mu\text{m}$ length and $1\ \mu\text{m}$ access region.

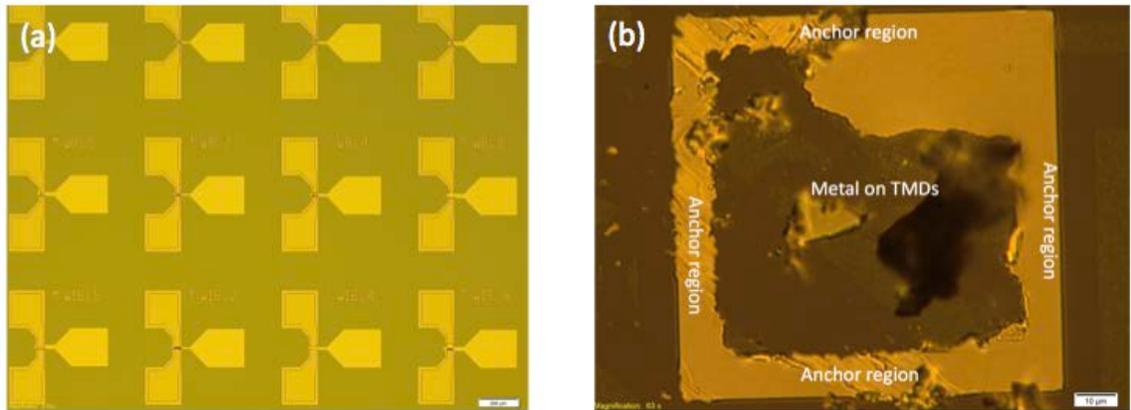


Figure 2.9. Optical microscopic images FETs and FET contact pads on WSe₂ wafer (M163) with $10\ \mu\text{m}$ anchor regions to the sapphire at the pad perimeter, first mask set. (a) After S/D and gate metal lift-off, the anchor regions are shown to hold metals in place, however in (b) the pads tear off on probing in regions where the contacts are on the WSe₂ and not directly on the sapphire.

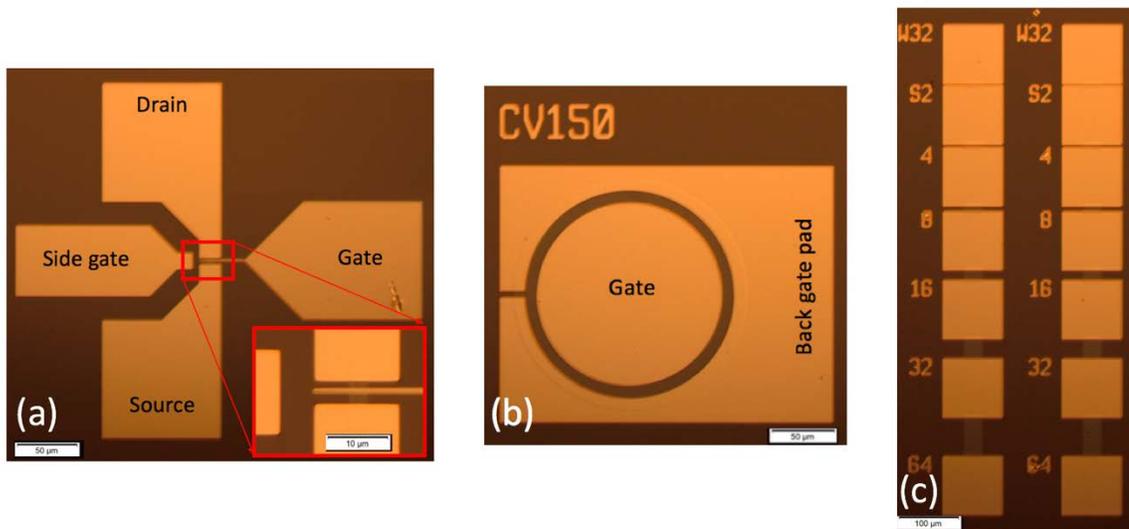


Figure 2.11. Optical microscopic images for some of the devices in the first approach mask set: (a) Transistor with 4 μm width, 1 μm gate length and 1 μm access region, (b) C-V structure with 150 μm diameter, and (c) TLM structures with separations and mesa width indicated.

Rest of this section is the development of FETs and TFETs on MOCVD WSe₂, designed by the first approach mask set. Temperature dependence of the FET characteristics and problems related to process are discussed. The MOCVD WSe₂ used in the FETs discussed was grown at 750 °C for 30 minutes using H₂Se and W(CO)₆ precursors with 10 minutes pre- and post-growth annealing. There was 90 seconds W flow prior to starting the growth and H₂ was used as the carrier gas. Figure 2.12 shows the (a) AFM and (b) SEM image of WSe₂ wafer #B021617B labeled as M179. Both images show continuous and conformal growth of WSe₂ on sapphire. The WSe₂ film contains 1 to 3 layers without surface contamination or particulates. The first layer of WSe₂ coalesces and is continuous and the upper layer appears as triangles. After receiving the wafer at Notre Dame, AFM

images were taken as a first step to confirm the cleanliness of the surface and it was found to be uncontaminated by shipping and like the AFM image from Penn State, Fig. 2.12 (a).

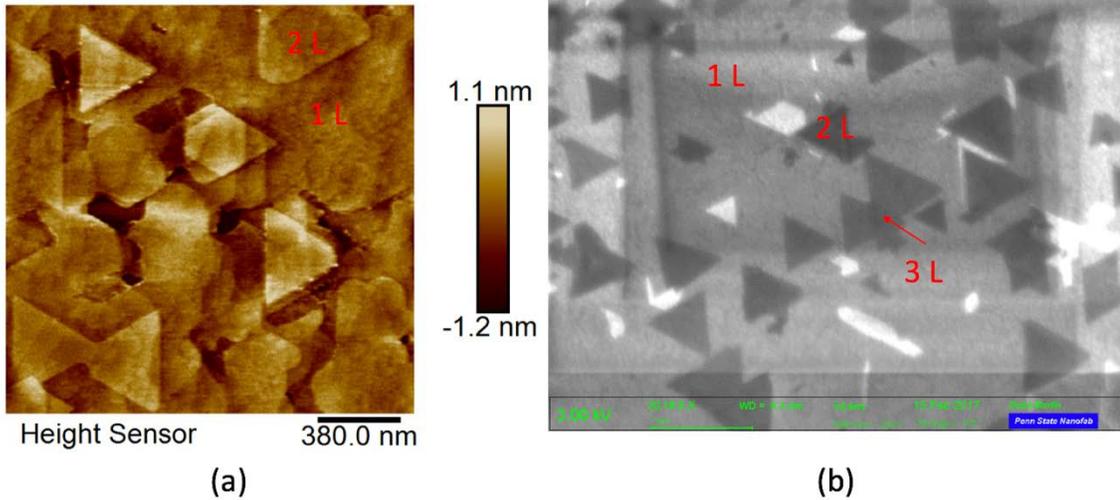


Figure 2.12. (a) AFM image of 1 to 2 monolayers WSe_2 on $1 \times 1 \text{ cm}^2$ sapphire substrate grown at 750°C for 30 minutes and (b) SEM image wafer in a $5.6 \times 4.2 \mu\text{m}^2$ area. Both images were taken at Penn State by Bhakti Jariwala.

After surface investigation by AFM and alignment mark formation, the WSe_2 channel was formed by etching the rest of the area using 15/10 sccm flow SF_6/Ar etchant by RIE for 10 seconds at 250 V bias. Step height after the etching process was 2 nm and consistent with the grown WSe_2 thickness (maximum 3 layers). Then, WSe_2 was patterned for source, drain, and side gate contacts using the Autostep-200 lithography followed by metal deposition of Ti/Pd (1/180 nm) evaporated by electron-beam and lifted off. The thin layer of Ti deposition for results in an incomplete surface coverage of Ti on WSe_2 and Pd then fills in the gaps to form a multi-work-function interface with Ti as the low work function for the n -contact and Pd as the high work function for the p -contact. The top gate oxide was deposited in two steps, first, 1.1 nm of Al_2O_3 was deposited at 110°C followed

by a 10 nm Al₂O₃ ALD layer at 200 °C. Totally, 11 nm Al₂O₃ was deposited on the WSe₂ channel followed by Ti/Au (20/80 nm) metal deposition as the gate contact.

After each step during the fabrication, AFM images were taken to evaluate the cleanness of the surface. Figure 2.13 shows representative AFM images after each step. The AFM images show low RMS roughness <1 nm of 0.65, 0.8, 0.72 (in channel region not sapphire), and 0.78 nm and clean surfaces for (a), (b), (c), and (d) images after each fabrication step.

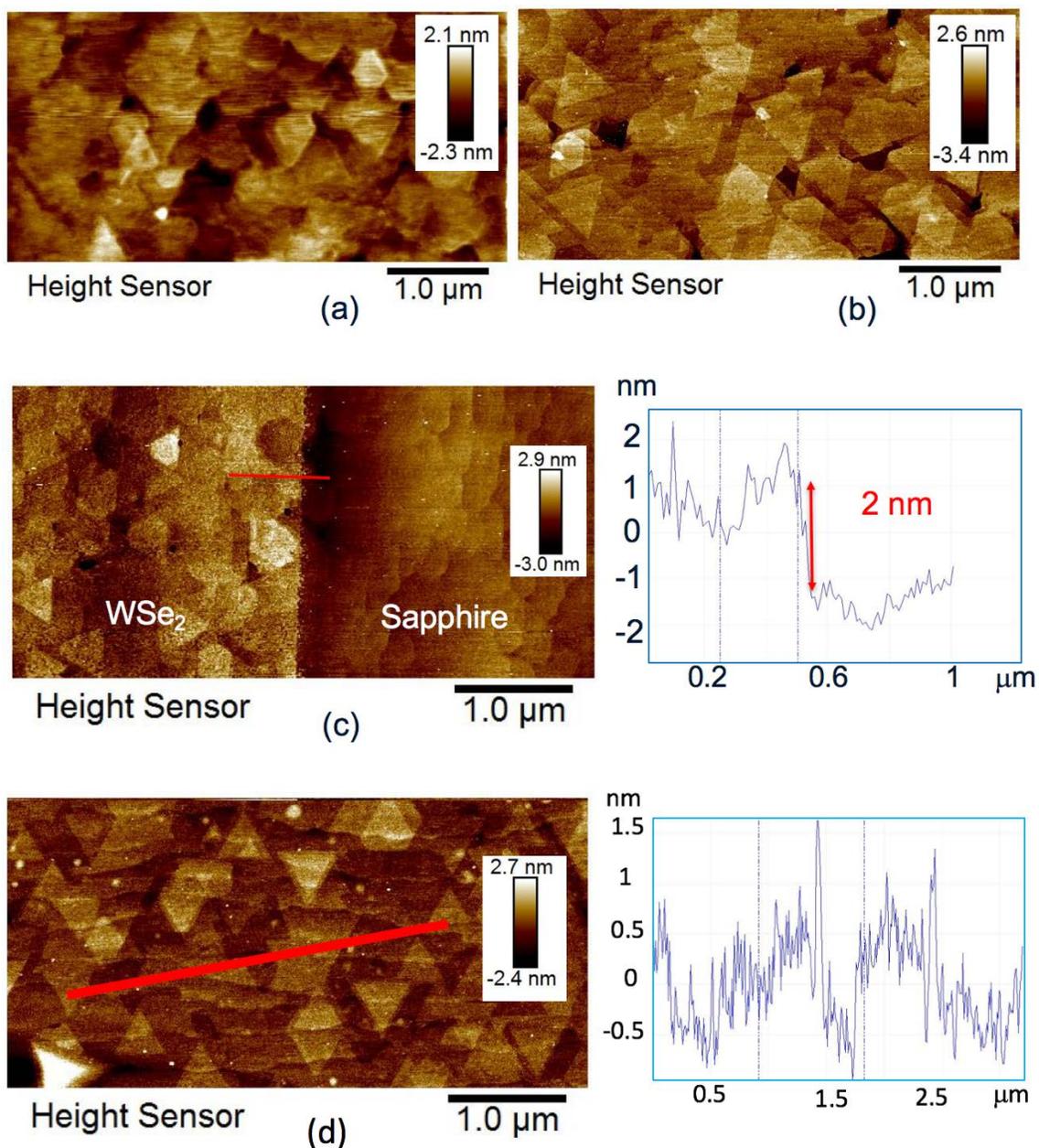


Figure 2.13. AFM images of WSe₂ on sapphire after each fabrication step: (a) as received, (b) WSe₂ surface after alignment mark evaporation, (c) channel formation along with line scan to show the step height, and (d) after ALD of 10 nm Al₂O₃ ALD on 1.1 nm Al₂O₃.

2.6 Electrical characterization of MOCVD WSe₂ FET (fabricated by first approach)

The cross section of the WSe₂ FET here is shown in Fig. 2.5(b) with $L_A = 0 \mu\text{m}$ and $L_G = 5 \mu\text{m}$ (Device M51). The measured drain current vs. top gate voltage is shown in Fig. 2.14(a). The transistor shows strong n -channel conduction, with on/off current ratio of more than 10^3 and weak p -channel conduction, with on/off current ratio of less than 10. It is interesting to note from the transfer characteristic in Fig. 2.14(a) that the electron conduction current is significantly larger than the hole conduction current for equal gate-source voltage. Since the band bending situations are similar for the hole and electron injection for equal gate-source biases, therefore, the height of the Schottky barrier for electron injection using Ti into the conduction band must be smaller than the height of the Schottky barrier for hole injection into the valence band. This implies that the Fermi level of Ti is aligned more towards the conduction band edge of WSe₂ and the transistors show n -channel conduction. In the course of the measurement, the leakage current was negligible and around the noise floor of the instrumentation. The corresponding values for the extracted on-current per unit width measured is $1.1 \text{ nA}/\mu\text{m}$ (8.6 nA) at $V_{DS} = 3.05 \text{ V}$ and $V_{GS} = 5 \text{ V}$. The lower current density can be explained by the Schottky contacts at the drain and source.

This is the first report of the characteristics of a top-gated WSe₂-on-sapphire FET. As a comparison, the only other top-gated report on CVD WSe₂ was grown on SiO₂ with a $50 \text{ nm Al}_2\text{O}_3$ dielectric by ALD [73]. In comparison with the n -FET reported, the WSe₂-on-sapphire FETs shows factor of $100\times$ improvement in the reported n -FET on SiO₂ on-current and on-currents comparable to the reported p -FET at a factor $10\times$ lower gate bias. WSe₂-on-sapphire does not permit back-gate biasing as the gate thickness is the thickness

of the substrate. This means the contact resistance cannot be improved by back gate bias, so access region doping is needed to lower the contact resistance.

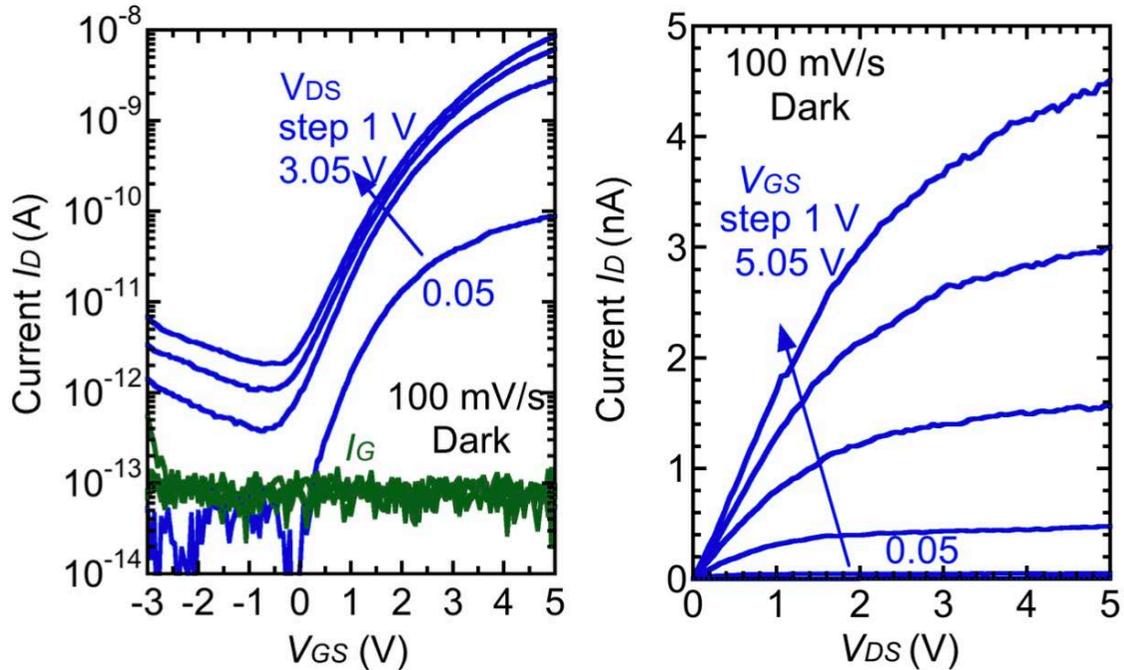


Figure 2.14. Electrical properties of top-gated few layer MOCVD WSe_2 on sapphire with channel length $L = 5 \mu\text{m}$, and width $W = 8 \mu\text{m}$. (a) Transfer characteristics, I_D - V_{GS} , vs. V_{DS} . (b) FET common-source characteristics. Both measurements are taken in the dark in a probe station with flowing N_2 ambient.

The common-source characteristics shows both the linear and saturation behavior. Gate length dependence for the WSe_2 FET with the width of $8 \mu\text{m}$ and lengths from 1 to $5 \mu\text{m}$ with the length step of $1 \mu\text{m}$ are shown in Fig 2.15(a). Increasing the channel length from 1 to $5 \mu\text{m}$ decreases the current from 10 to 0.43 nA at $V_{DS} = 5 \text{ V}$, $V_{GS} = 5.05 \text{ V}$, Fig. 2.15(b). According to the FET square-law model, it is expected the drain current to be proportional to W/L ratio. Fitting the experimental data linearly in Fig. 2.15(b) shows that

the experimental data does not fit perfectly. As the gate length and width were not measured after fabrication, there is a uncertainty in width and length. The general trend of increasing current with W/L and V_{DS} is however observed.

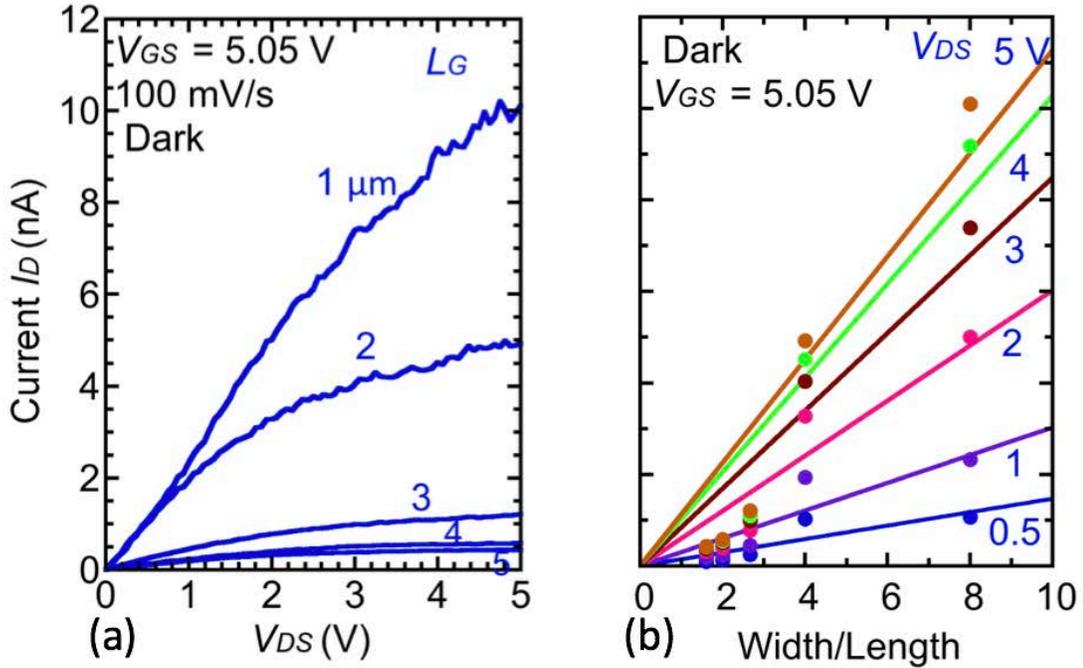


Figure 2.15. Common-source characteristics for a few-layer MOCVD WSe_2 $nFET$ on sapphire with channel width $W = 8 \mu m$, (b) Drain current vs. gate length for $W = 8 \mu m$ and 5 different gate lengths at $V_{GS} = 5.05$ V on wafer M179.

2.7 Temperature dependence of MOCVD WSe_2 FET (fabricated by first approach)

Temperature dependence of the transfer characteristic of this same FET wafer with 1-3 layers of WSe_2 were made. Measurement of the drain current vs. V_{GS} from 223 to 373 K, with the gate biased from -3 V to 5 V was performed. From the temperature-dependence study a barrier height was extracted and used to determine the Schottky barrier height. Current transport through a Schottky barrier occurs by three mechanisms:

thermionic emission I_T , thermionic field emission I_{TF} , and field emission I_F , corresponding to emission over the Schottky barrier, tunneling of hot carriers through the barrier, and direct tunneling through the barrier, respectively, as discussed by Padovani and Stratton [74]. Electron injection originates from the source side from Ti. The band diagrams, insets in Fig. 2.16, indicate bias conditions, from left to right, showing transport governed by thermionic emission, thermionic-field emission, and direct tunneling. In WSe₂, the current density is controlled by thermionic emission and in the reverse direction is given by $J = AT^{1.5} \exp(q\Phi_B/kT)$ [75], where the parameters are the Richardson constant $A = 4\pi qm^*k^2/h^3$. This reverse current can reveal the barrier height. Therefore, Schottky barrier height and flat band voltage can be determined from barrier height vs. gate-source voltage.

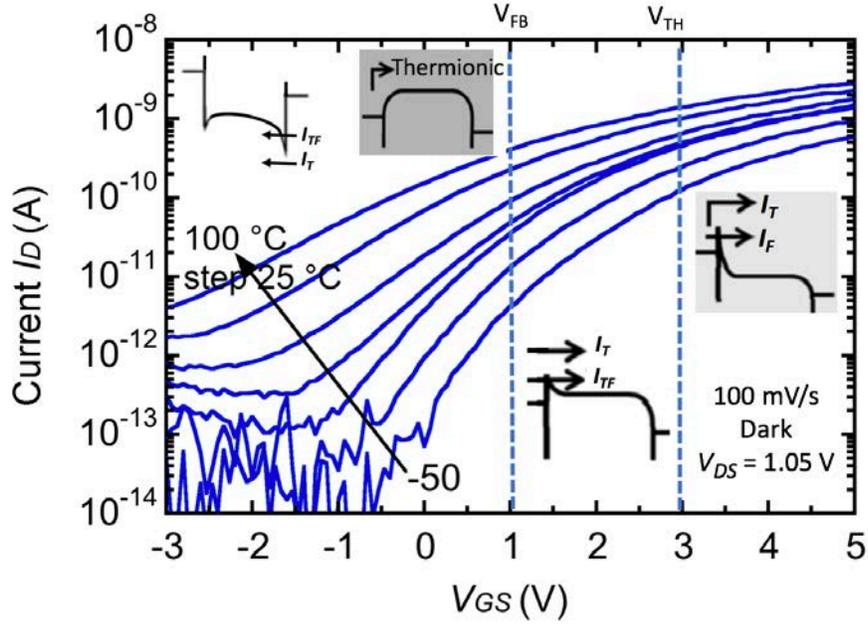


Figure 2.16. Experimental transfer characteristics of a 1-3 layers WSe₂ transistor with $W = 8 \mu\text{m}$, $L = 5 \mu\text{m}$ using Ti contacts. The insets represent the energy band diagrams corresponding to the applied gate biases in three distinct regions: below flat band, below threshold, and above threshold on wafer M179.

Drain current vs. inverse temperature is extracted from Fig 2.16 for gate voltages from -1 to 5 V. The slope of the curves in Fig. 2.17(a) in the high-temperature region (from 2 to 5 K^{-1}) is calculated for each voltage. The effective barrier height extracted from Fig. 2.17 linearly responds to the gate voltage V_{GS} that is result of the fact that the current flows by thermionic emission. The Schottky barrier height corresponds to the voltage at which Φ_B deviation from a linear dependence on gate voltage and this also corresponds to the voltage at which the gate source voltage corresponds to the flatband condition V_{FB} . From Fig. 2.17(b), a Schottky barrier height of 0.18 eV with flat band voltage of 1 V is extracted.

Also, 3 V threshold voltage in Fig. 2.167 is extracted from the gate-voltage axis intercept of the linear extrapolation of the I_D - V_{GS} curve.

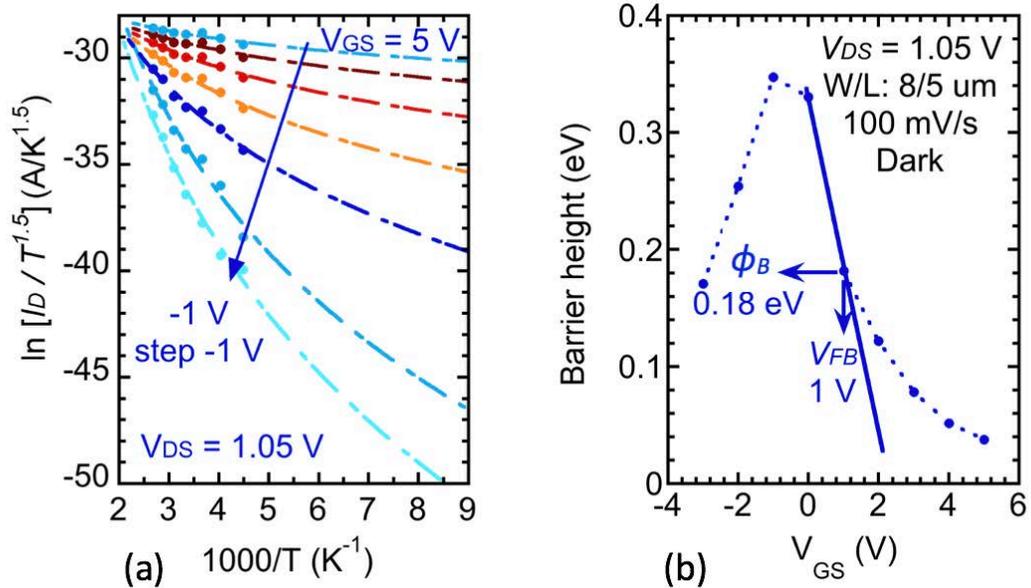


Figure 2.17. (a) Arrhenius-type plot constructed from Fig 2.16 at different gate voltages and (c) Barrier height vs. gate-source voltage indicating the flat band voltage where the n -Schottky barrier height is extracted, wafer M179.

2.8 WSe₂ FET measurements after application of PEO:CsClO₄ (fabricated by first approach)

Typically once the gate oxide is removed and PEO:CsClO₄ is applied the WSe₂ conductivity increases of order 100x [61]. However, on wafer M179, measurement for the FETs with access regions at room temperatures did not increase the drain current. A maximum current of 2 pA was achieved at $V_{GS} = 5$ V and $V_{DS} = 3.05$ V using the ions. Cooling down the ions in order to lock the ions to dope the channel did not increase the

drain current. To discover the reason why ion doping did not increase the current as expected, TEM images were taken to investigate more about the device. The TEM image in Fig. 2.18 shows the cross section of transistor including gate, drain-source with 1 μm gate length, 8 μm gate width, and 1 μm access region (Device M11). The different regions are labeled as A, B, C, D, E, F, G, and E and scanning transmission electron microscope (STEM) images with high resolution were taken at these regions. To have better understanding from each region, STM images are shown in the following images. Since FET M11 is symmetric with respect to gate, for better comparison between the regions, STEM images for symmetric regions are considered together.

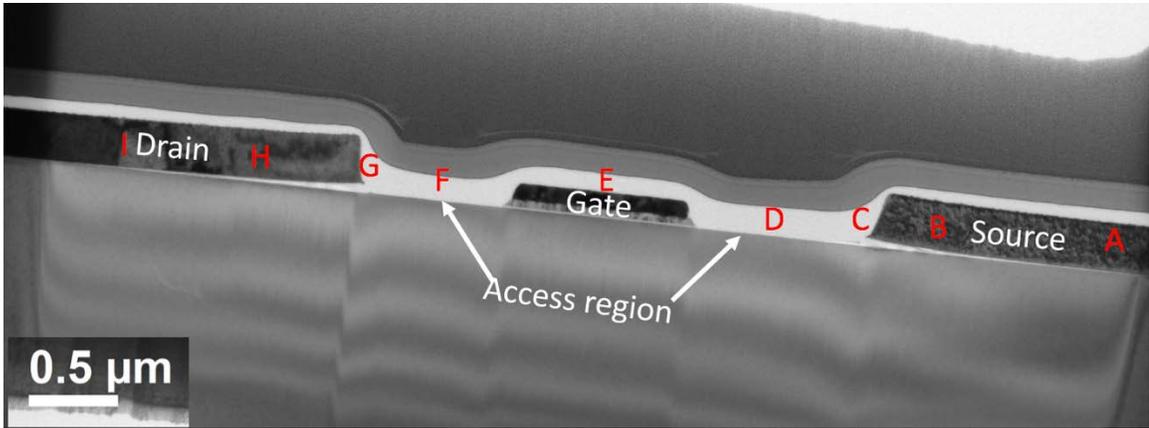


Figure 2.18. TEM image of FET M11, including gate, drain, source, and access region.

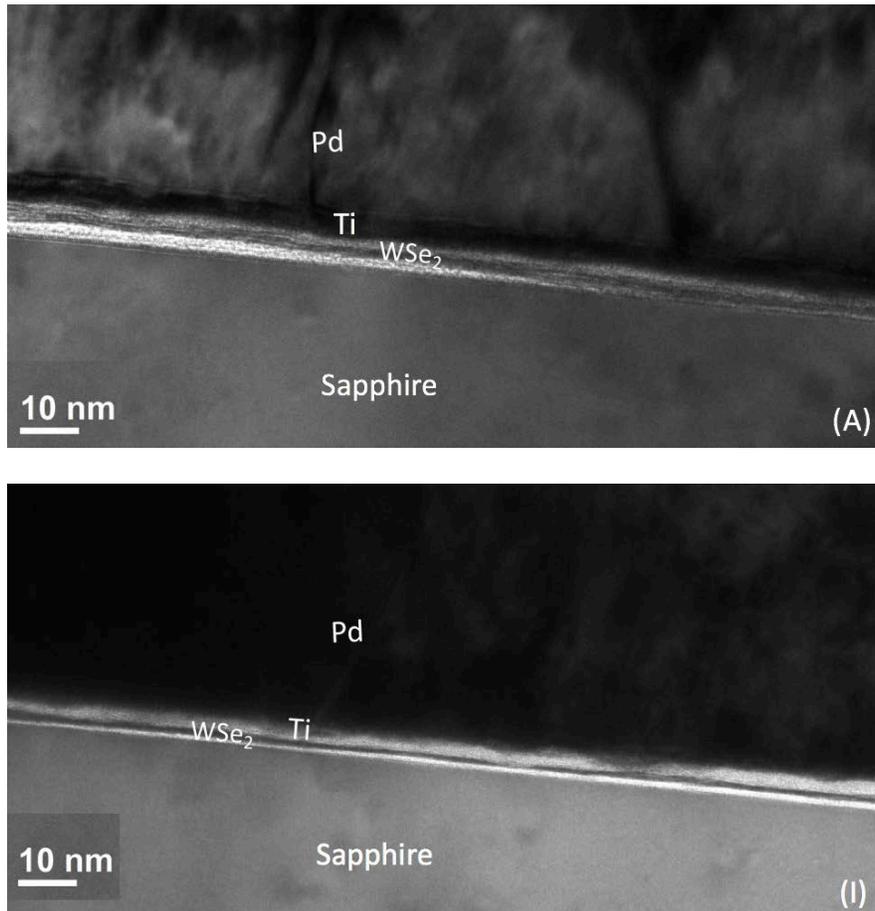


Figure 2.19. STEM image of FET M11 in region (A) and (I).

Regions (A) and (I) are source and drain regions far from the channel. At the right side of the region (A) there are 2 monolayers (1.5 nm) WSe₂ with Ti and Pd contact on top. Going from right side to left, a gap between WSe₂ and sapphire starts to increase. For (I) the STEM image is a bit closer to channel and going from left to right, the gap is increasing. Ti is shown as black color on WSe₂ in both images following by Pd contact.

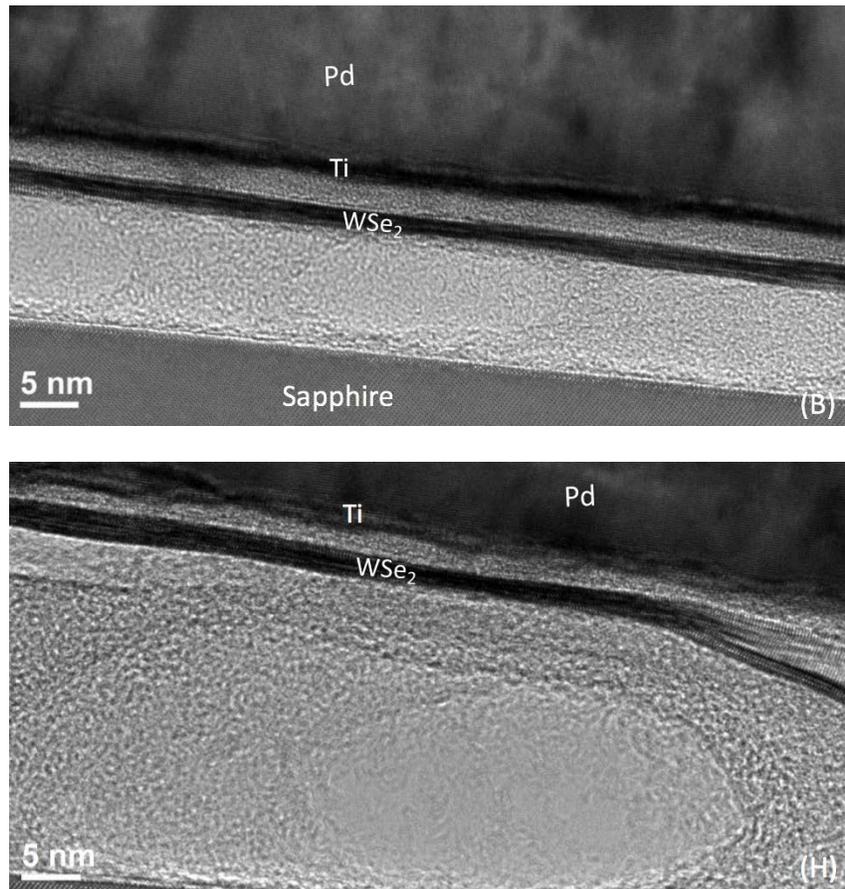


Figure 2.20. STEM image of FET M11 in region (B) and (H).

Regions (B) and (H) are source and drain regions closer the channel. Closer to channel, the gap is increasing to more than 20 nm. Two monolayers of WSe₂ layer are seen to be continuous under both drain and source contact.

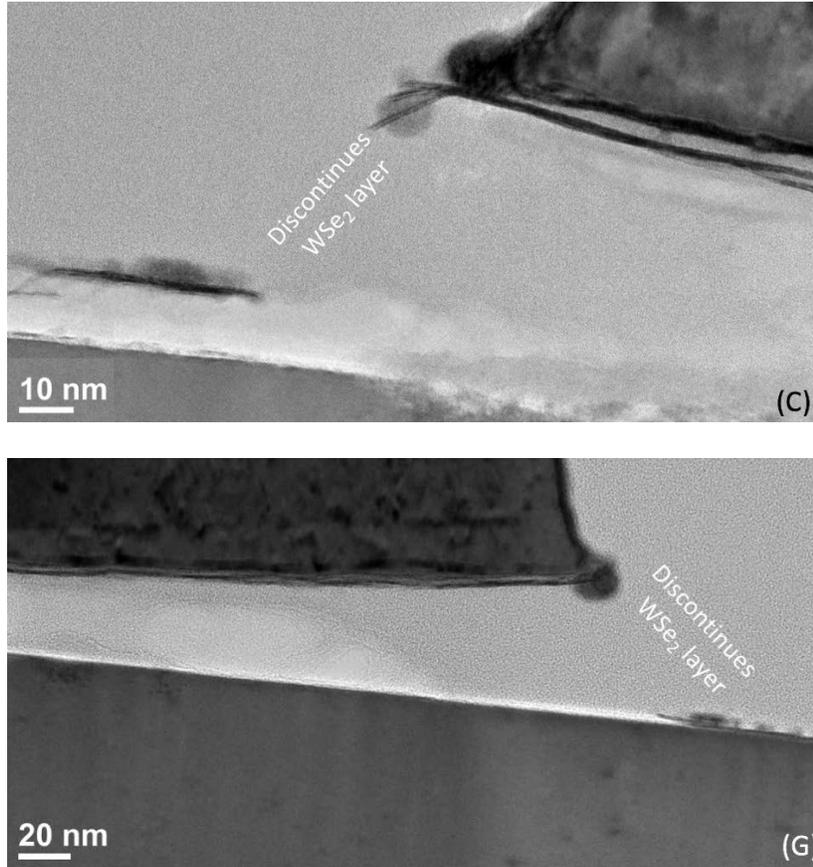


Figure 2.21. STEM image of FET M11 in region (C) and (G).

Regions (C) and (G) are the edge of source and drain regions. The gap is still getting larger for both regions, ~ 80 nm. Also, on both of the drain and source contact the channel has been damaged and is not continuous anymore. This is attributed to residual strain in the thick layer of metal deposition.

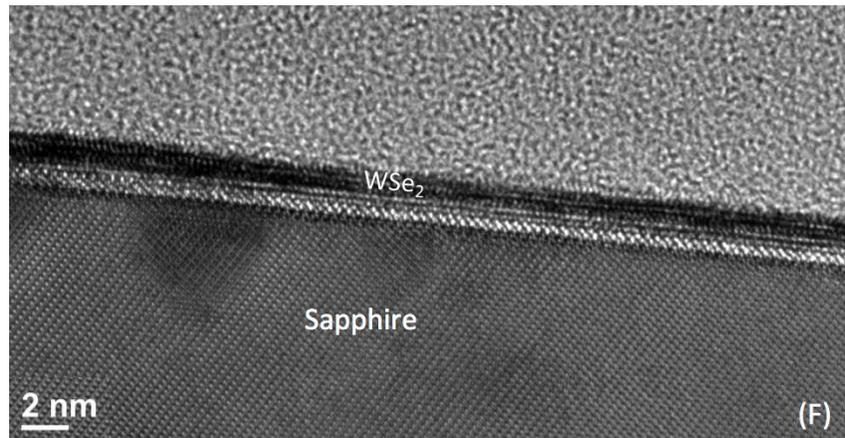
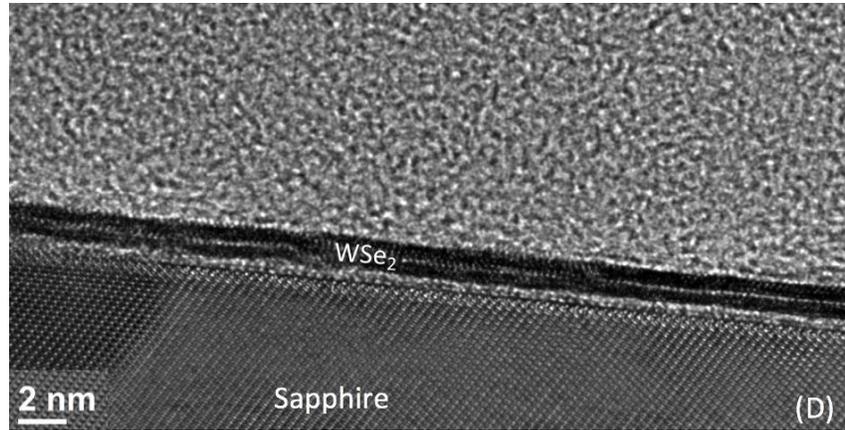


Figure 2.22. STEM image of FET M11 in region (D) and (F).

Regions (D) and (F) are access regions that Al_2O_3 has been removed by buffered HF. These images are representative STEM images and for all of the images, the WSe_2 layer is continuous and around 2-3 monolayer.

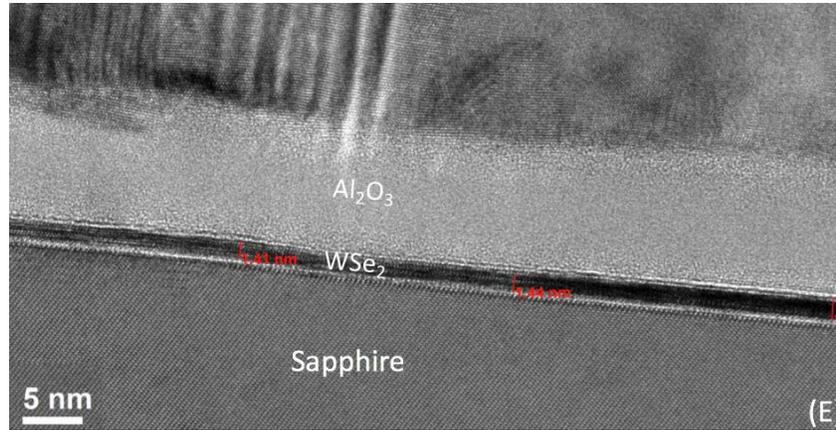


Figure 2.23. STEM image of FET M11 in region (E).

Regions (E) is the gate region where 11 nm Al₂O₃ is deposited on WSe₂. In this region, WSe₂ is continuous and is not detached from sapphire substrate. Ti and Au are deposited as a gate metal. The Ti metal was deposited on Al₂O₃ on WSe₂ without any detachment of the metal from substrate. Since the gate metal is deposited on Al₂O₃ not WSe₂ and Al₂O₃ is holding WSe₂ layer, so the metal is not detached.

From STEM images, both drain and source contacts in the region close to channel start to detach from the substrate. Near the edge of the contacts, WSe₂ layer on both sides is not continuous anymore. The STEM images can explain why low drain current was achieved after ion doping and it can be explained by the discontinuity of the channel. Curling off the metal from substrate was due to thick metal deposition; depositing thick layer of metal on WSe₂ layer can build up thermal stress and since WSe₂ layer is weakly bounded to sapphire, it can be easily detached from the surface. There is also evidence that the Ti/Pd contact is under tensile stress on the WSe₂. This problem is solved by decreasing

the metal contact thickness and required another mask level to make the contact pad thickness thick enough for repeated probing.

2.9 Second approach in TFET stepper process flow

In order to solve the first process flow problem, metal deposition needed revision and a thin S/D metal was deposited on the WSe₂ channel. In this process flow, 5 mask levels were designed. The S/D contact mask was edited and split into two different masks, one for contact to the device and a second for the S/D pads for probing. In the second fabrication approach, Ti/Pd (1/40 nm) was evaporated where S/D contacted WSe₂ and Ti/Au (20/200 nm) was evaporated for pads and side gate electrodes. The gate oxide deposition and gate metal deposition remained the same.

Figure 2.24(a) shows an AFM image of the WSe₂ on sapphire for the measurements described in chapter 4. As seen previously, there are triangular WSe₂ submicron grains that coalesced into a polycrystalline WSe₂ film. The three different transistor structures in the mask set are labeled T1, T2 and T3 in Fig. 2.24 and shown in (b,c) cross section and in (d-e-f) as accurate top-view layouts. Transistor T1 has the gate overlapping the source and drain; transistors T2 and T3 have the gate positioned between the source and drain with access regions on either side of the gate. Transistors T2 and T3 have one or two side gates which are used as field plates to control the access region carrier type and density as will be explained with the measurements in chapter four. In Fig. 2.24(d) the label SG means side gate; in (e) SGS refers to the side gate on the source side, and SGD is the side gate on the drain side. The labels S, D, and TG refer to source, drain, and top gate. The gate width is 8 μm with gate lengths of 1, 2, 4, 8, and 16 μm , and access region lengths of 1, 2, 3 and

6 μm . The side gate for all of the T2 and T3 transistors had 7 μm width and 5 μm distance from the of gate.

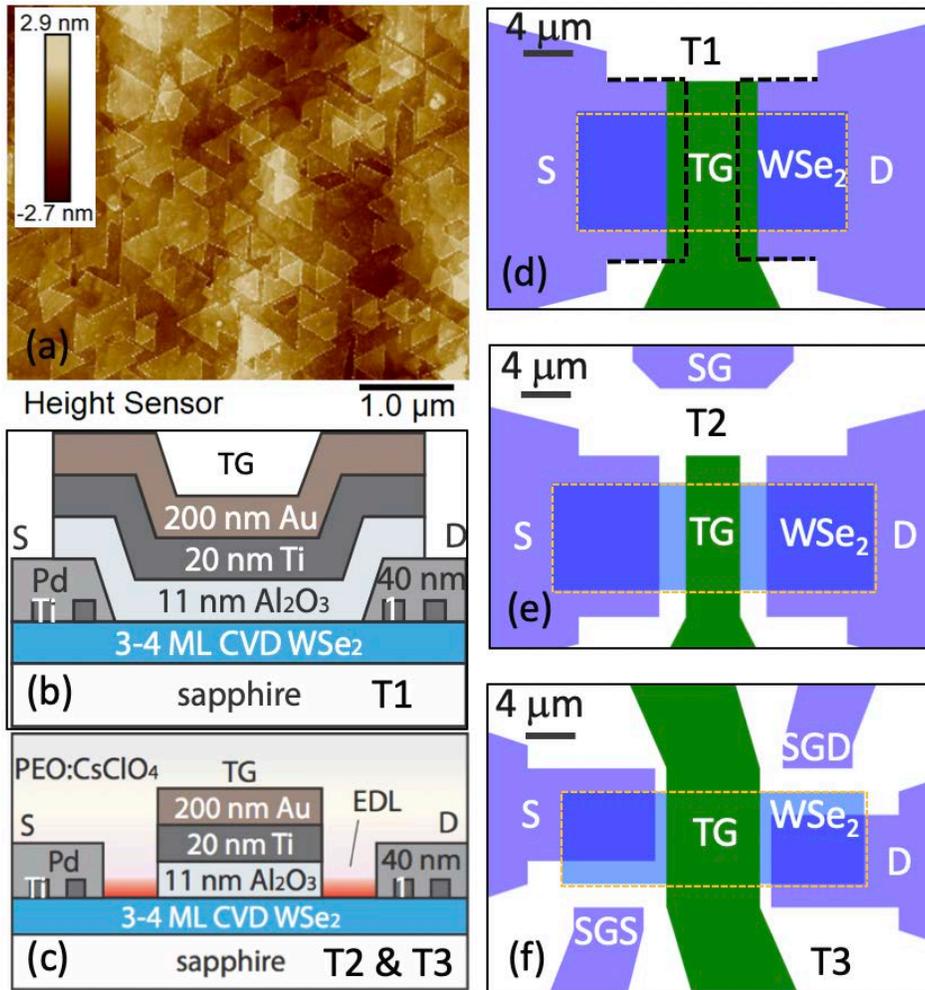


Figure 2.24: (a) AFM image of WSe₂ on sapphire, (b) cross section of transistor T1 with 2 μm gate overlap, (c) cross section of transistors T2 and T3 with access regions. The red layer in (c) indicates the accumulation of ions at the WSe₂ surface and forms half of the electric double layer (EDL). These ions are contained in the polymer PEO:CsClO₄ and positioned by an electric field controlled by a side gate (not shown). (d-e-f) Dimensionally accurate top-view layouts of the three transistors T1, T2, and T3, respectively.

All layers in the mask were redesigned to focus the characterization on structures of interest. The C - V test structures without overlap were laid out for capacitance measurements with diameters of 60, 84, 120, and 170 μm with 4 μm access regions. Corbino disks were designed for contact resistance measurements. The transmission line measurement (TLM) structures were provided to determine the contact resistance and sheet resistance between the metal and WSe_2 . The separation between the contacts are 2, 4, 8, 16, 32, 64 μm with 32 μm width. Table 2.4 summarizes FETs, TFETs, C - V structures, Corbino disks, and TLM structures with the geometry and dimensions for each in the new mask set. Totally 64 devices were designed in this mask set that is shown in Fig. 2.25. In chapter four, the electrical measurements for fabricated devices using this mask are discussed in detail.

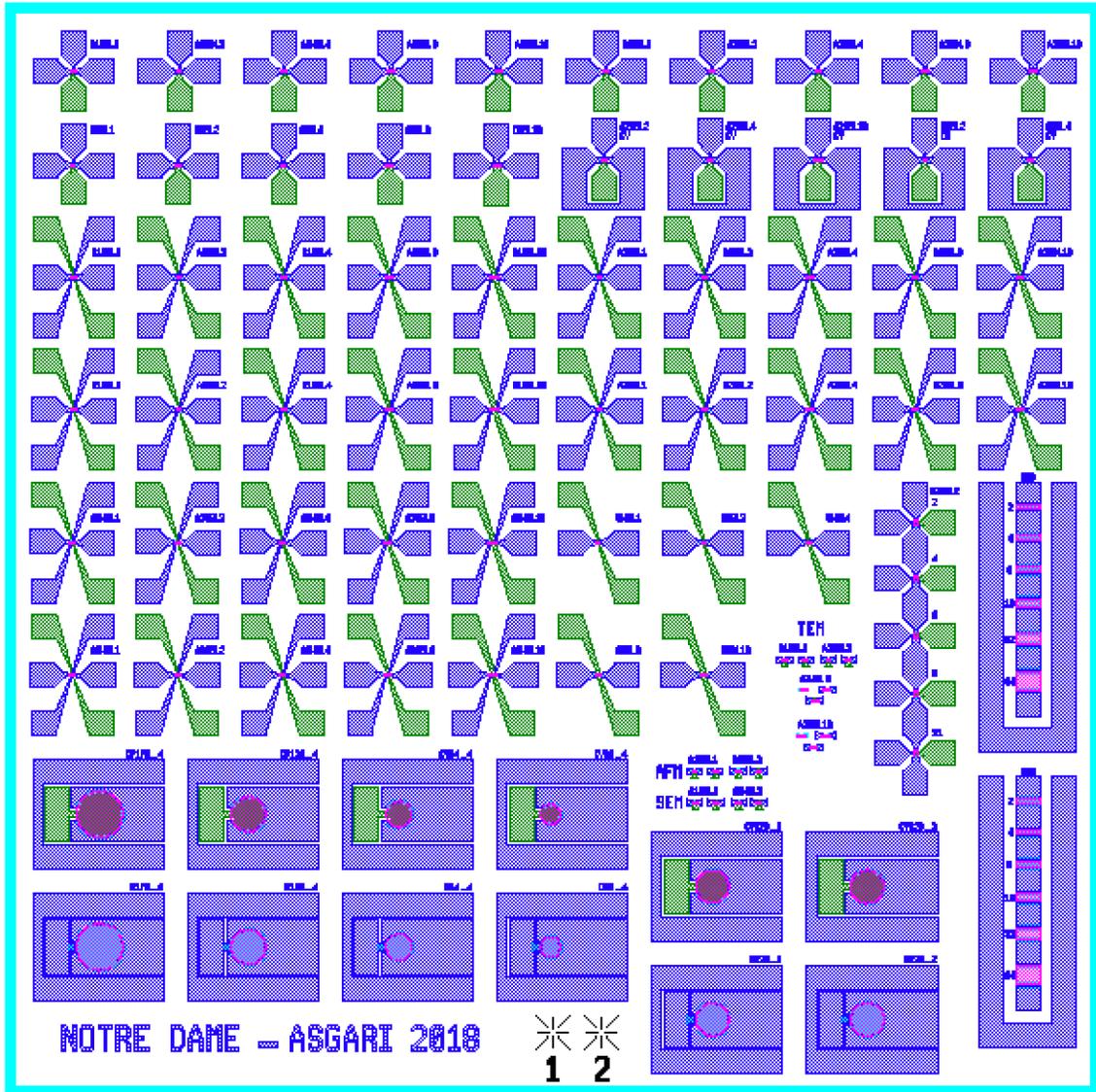


Figure 2.25. TFET stepper mask, 3.6 x 3.8 mm², 5-mask level. Each color is corresponding to different mask level; black, pink, (light and dark) blue, and green colors are indication of alignment mark, channel isolation, (thin and thick) S/D contact, and gate formation, respectively.

TABLE 2.4.

SUMMARY OF THE FET, TFETS, CV STRUCTURES, CORBINO DISKS AND TLM STRUCTURES IN MASK SET VERSION 2 WITH THEIR GEOMETRIES.

Device	Access region (μm)	Width (μm)	Length (μm)	Contact overlap with mesa(μm)	Diameter(μm)
10 Overlapped FETs	0	8	1,2,4,8,16	8	-
5 FETs & TFETs with one SG	1	8	1,2,4,8,16	8	-
5 FETs & TFETs with one SG	2	8	1,2,4,8,16	8	-
10 FETs & TFETs with two SGs	1	8	1,2,4,8,16	8	-
10 FETs & TFETs with two SGs	2	8	1,2,4,8,16	8	-
5 FETs & TFETs with two SGs	3	8	1,2,4,8,16	8	-
5 FETs & TFETs with two SGs	6	8	1,2,4,8,16	8	-
4 CV Structures	4	-	-	8	60,84,120,170
2 CV Structures	1,2	-	-	8	120
4 Corbino disks	4	-	-	8	60,84,120,170
2 Corbino disks	1,2	-	-	8	120
2 TLM structures	-	96	2,4,8,16,32,64	8	-

CHAPTER 3: ATOMIC LAYER DEPOSITION OF GATE STACKS ON 2D SEMICONDUCTORS

Because of the lack of dangling bonds on WSe₂ surfaces, nucleation of ALD oxides is challenging. The approach taken here is to deposit a first nucleation layer in the ALD at low temperature in a physical vapor deposition (PVD) mode. The temperature is then increased and the remainder of the film is deposited by ALD. This follows an approach developed by Prof. Andy Kummel [44] at Univ. California at San Diego.

Highly ordered pyrolytic graphite (HOPG, grade 2 from SPI Supplies) is used as a 2D material substrate for the ALD process development. Processes developed on HOPG are more likely to transfer to other 2D materials like WSe₂ than processes developed on 3D surfaces like Si. Fresh and clean surfaces of HOPG wafers are readily achieved by mechanical exfoliation using an adhesive tape just prior to loading for ALD. Both Al₂O₃ and HfO₂ oxides have been explored on HOPG using the precursors trimethylaluminum (TMA) or tetrakis(dimethylamido)hafnium (TEMAH) and H₂O separated by Ar and N₂ purges. The CVD component of the deposition is enhanced at low temperature and by increasing the intermixing of the precursor and the water pulses.

Two ALD systems have been used in the development of oxides on WSe₂, a Savannah Cambridge 100 system with a deposition temperature range from 50 to 300 °C with a base pressure of 200 mTorr. Also utilized has been an Oxford Flexal ALD with

temperature control between 110 and 300 °C, and base pressure of 15 mTorr. For the processes under consideration here consisting of a low temperature nucleation step followed by a higher temperature ALD step, the time to change the temperature is a consideration. In both systems, it takes about 120 minutes to change and stabilize the temperatures before deposition. These long delays are not desirable but are necessary in these tools.

In this chapter selected process-development experiments in the Savannah and Oxford ALD systems are discussed to illustrate the state of the gate oxide development in this research. The films are characterized by AFM to measure the surface coverage and roughness, ellipsometry is used to get the thickness (on a companion Si pilot wafer), and electrical measurements, current-voltage and capacitance-voltage measurements to measure leakage, electrical thickness, and as an indicator of traps.

3.1 Deposition of HfO₂ on HOPG in the Oxford Flexal ALD system

In the first report of top-gated FETs on MoS₂ by Radisavljevic [76], 30 nm of HfO₂ was deposited by ALD at 200 °C using tetrakisdi(methylamido)hafnium, Hf(N(CH₃)₂)₄ and H₂O vapor as the precursors and oxidant, respectively. The process used 1 and 2 s pulse times for the Hf and water precursors, respectively, followed by 5 s purge for Hf and 10 s for H₂O resulting in a growth rate of 1.9 Å/cycle. This recipe was used as a reference deposition and check against prior art, as the same precursor is available in our Oxford Flexal ALD system.

The Radisavljevic reference recipe was performed on a fresh and exfoliated HOPG surface and on an RCA-cleaned Si substrate. Totally, 150 cycles were performed. The

thickness measured by ellipsometry on the Si pilot was 36 ± 1.5 nm, indicating a deposition rate of 2.4 ± 0.1 Å/cycle. This compares with 1.9 Å/cycle reported by Radisavljevic [76]. A typical growth rate for HfO₂ on Si grown in an ALD mode at about a monolayer per cycle or 1 Å/cycle in our Oxford tool at 200 °C. The high deposition rate observed here indicates that the grown oxide is more CVD-like than ALD. There are some minor differences in the growth systems and they are not identical systems. For example, in their system, the pressure was kept at 90 mTorr while it is 15 mTorr in the Oxford Flexal ALD.

A representative AFM image of 150 cycles of HfO₂ at 200 °C on HOPG is shown in Fig. 3.1. There are some white features on HOPG with 3 to 10 nm height likely resulting from the CVD-like process. The surface RMS roughness is 2.5 nm, which is not sufficiently uniform for the TFET gate oxide, which should have roughness <1 nm. Although the surface does not look smooth, there is no evidence of pinhole formation on the surface. Pinhole formation can be detected by the depth of the line scan in the AFM image. Here the thickness of the oxide is 36 ± 1.5 nm and no features are observed approaching this depth.

After HfO₂ deposition, 20/200 nm Ti/Au was electron-beam evaporated using a shadow mask in an AIRCO Temescal FC1800-1 evaporator. Metal-Insulator-HOPG capacitors (40 μm diameter) were characterized by current-voltage (*I-V*) measurements. A roughly symmetric *I-V* characteristic was obtained with a leakage current of approximately 0.75 pA (0.6 fA/μm²). While this is a low current on an absolute scale, the measured current should have been limited by the noise floor of our instrumentation, 100 fA for this oxide thickness. This is an indication of some imperfections in the film leading to this leakage.

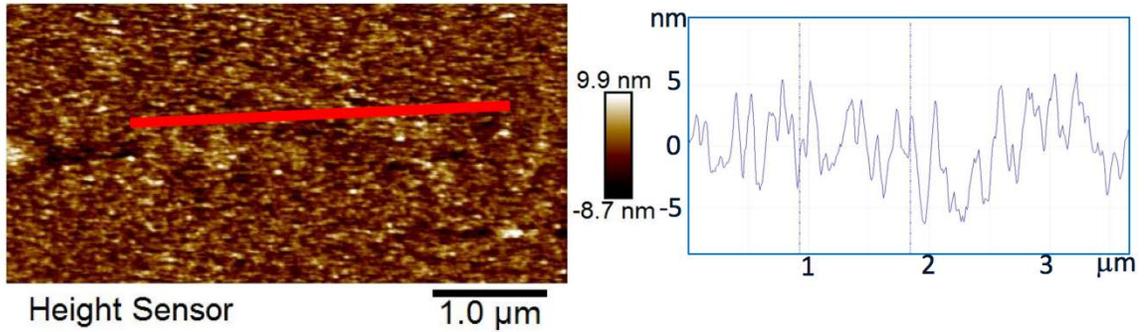


Figure 3.1 AFM image of 150 cycles HfO₂ grown on HOPG at 200 °C using TEMAH and H₂O precursors in the Oxford ALD system using the conditions of Radisavljevic [76], the pulse sequence 1 s TEMAH pulse/5 s Ar purge/2 s H₂O pulse/ 10 s Ar purge. No pinholes are detected after growth and the RMS surface roughness is 2.5 nm.

To observe the deposition in the early stages of nucleation, the number of cycles was reduced from 150 to 10 to make a thinner film. Due to the high rate of deposition (2.4 Å/cycle) nonuniform deposition can be expected for the first layers. Figure 3.2 shows a 10-cycle deposition of HfO₂ on HOPG again using the Radisavljevic ALD conditions, with partial nucleation observed mostly along the step edges of HOPG. The surface roughness is 3.1 nm and the line scan show that the roughness extends all the way to the HOPG surface. The initial stages of growth show a similar roughness to what was measured after 150 cycles showing that the film does not get smoother as it becomes thicker. The nonuniform open structure seen in nucleation is consistent with the observed high rate of deposition and low dielectric constant.

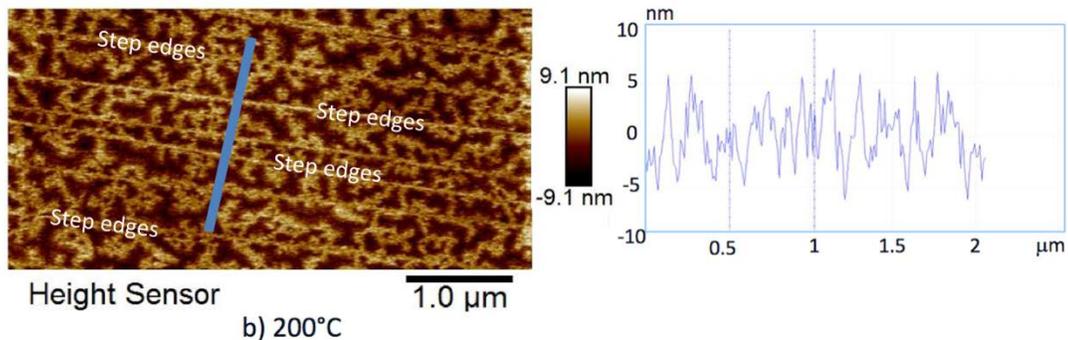


Figure 3.2. AFM images of 10-cycle deposition of HfO₂ film on HOPG at 200 °C with the pulse sequence 1 s TEMAH pulse/5 s Ar purge/2 s H₂O pulse/ 10 s Ar purge Partial coverage on HOPG is observed with the greatest nucleation at the step edges.

3.1.1 Deposition temperature dependence of HfO₂ on HOPG in the Oxford Flexal ALD

To further understand the early stages of growth, the deposition temperature dependence of the first 10-cycles of HfO₂ on HOPG was investigated. Deposition temperature can change the kinetic energy of precursors and affect the nucleation formation. Again, using the ALD conditions of Radisavljevic, HfO₂ was deposited at different temperatures of 300, 200, 170 and 150 °C to see how temperature affects HfO₂ nucleation on HOPG. AFM images and line scans are shown in a 2.5 x 5 μm² area for all 5 temperatures in Fig. 3.3. At 300 and 400 °C, nucleation is inhomogeneous and only partial coverage is observed. At these temperatures, the nucleation of HfO₂ is observed mostly along the step edges. By decreasing the temperature to 170 and 150 °C, nucleation at the step edges is not observed and the film appears to nucleate on the HOPG surface, but it is not clear that it is continuous. At 150 and 170 °C, hemispherical formations are visible with diameter of ~ 0.5 μm and height of maximum 10 nm.

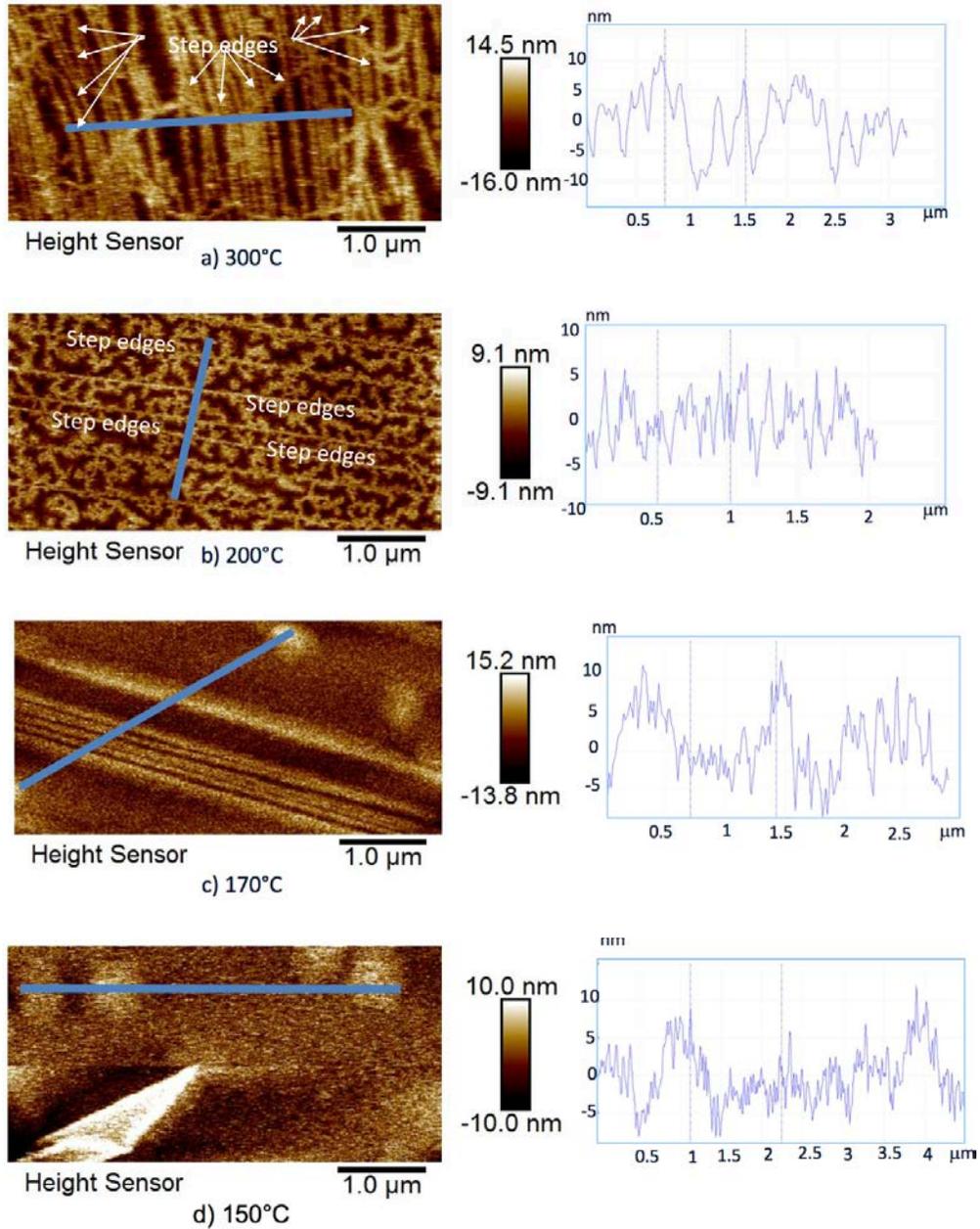


Figure 3.3. AFM images of 10-cycle depositions of HfO₂ film on HOPG with different growth temperatures: (a) 300 °C, (b) 200 °C, (c) 170 °C, and (d) 150 °C. Each ALD cycle consists of the pulse sequence 1 s TEMAH pulse/5 s Ar purge/2 s H₂O pulse/ 10 s Ar purge. At higher temperatures, partial coverage and more open areas are visible on HOPG.

This experiment shows that at higher temperatures nucleation of HfO₂ occurs preferentially at the step edges. As temperature is lowered the oxide is found to condense everywhere but the film is not uniform and continuous. The thickness of the deposited film is about 10 nm but with peak-to-peak roughness also of about 10 nm. The 10 nm thickness gives a deposition rate of about 1 nm/cycle which is about 5x higher rate than was measured on the 150 cycle film on the Si substrate. While more than 100 other ALD HfO₂ thin film depositions have been made, this study gives a representative view of the resistance of 2D materials to nucleation of oxides. Growing HfO₂ film directly on substrate such as Si creates an interfacial layer at the Si-oxide interface due to existence of excess oxidizing elements at the interface [77-78]. This statement can be true on layered materials as well.

3.2 Deposition of Al₂O₃ on HOPG in the Savannah Cambridge 100 ALD

Al₂O₃ is also well suited as a gate dielectric on 2D materials with low dielectric constant of 9 compared to Hf but larger band gap of 8.8 eV [79]. The Savannah Cambridge ALD system has capability for deposition at 50 °C, below what can be achieved in the Oxford system, 110 °C. ALD of Al₂O₃ was explored using a low temperature nucleation step as was done for HfO₂. Al₂O₃ was deposited at 50 °C on fresh HOPG using TMA and H₂O as ALD precursor and oxidant, respectively. The pressure was kept at 200 mTorr and 20 sccm N₂ flow was used as purge gas. The ALD sequence used was 600 ms TMA pulse/ 500 ms N₂ purge/ 50 ms H₂O pulse/ 500 ms N₂ purge, following a method proposed by Prof. A. Kummel [44]. This recipe was used as a reference as the same precursor and temperature is available in the Savannah ALD. AFM image of 50-cycle deposition of Al₂O₃ on HOPG at 50 °C is shown in Fig. 3.4.

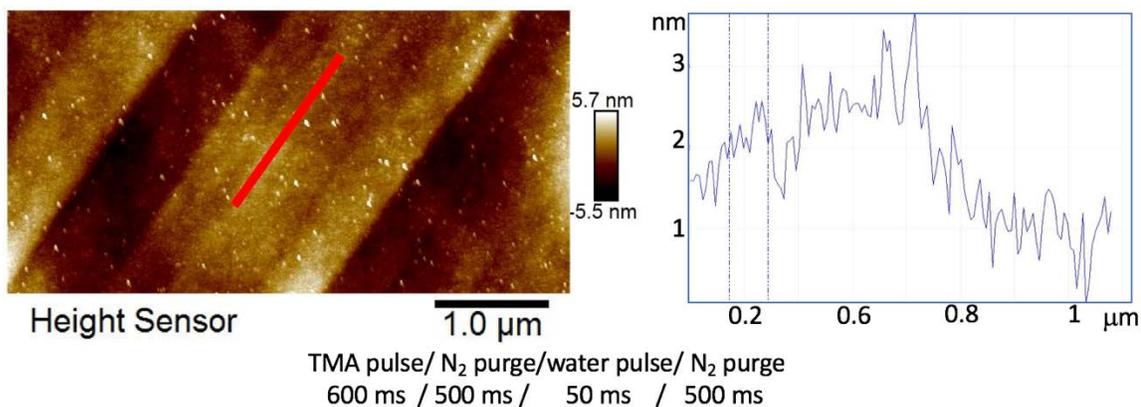


Figure 3.4 AFM image of 50-cycle deposition of Al₂O₃ on HOPG at 50 °C using 600 ms TMA pulse/ 500 ms N₂ purge/ 50 ms H₂O pulse/ 500 ms N₂ purge. The nuclei centers of Al₂O₃ were observed.

As observed on HfO₂, low temperature deposition at 50 °C leads to continuous nucleation on both step edges and terraces of HOPG with peak-to-peak roughness of about 1 nm, Fig. 3.4. The nuclei centers of Al₂O₃ (bright spots) were observed across the 1 x 1 cm² surface with small diameter (20 nm); these features were not observed in the low temperature nucleation experiments on HfO₂. The measured deposition rate was 20 Å/cycle (while 1.2 Å /cycle was obtained by Prof. Kummel's recipe in their custom ALD system at UCSD). This rate is much higher than desired for a nucleation layer; the rate obtained by UCSD is preferred to allow more precise control. The difference in deposition rates in the two systems shows the process must be tuned for use in the Savannah ALD system.

3.2.1 Dependence of N₂ purge time after the TMA pulse on Al₂O₃ nucleation on HOPG in the Savannah Cambridge 100 ALD system

To explore the nucleation phase in the Savannah system, the effect of N₂ purge time after the TMA pulse was studied. Since a thin layer of nucleation oxide is desired, a 10 cycles deposition, to induce 1-2 nanometer oxide, was considered. Generally, longer N₂ purge time means less remaining TMA from the previous reaction and thus thinner oxide is expected. It makes the process more ALD-like. For this purpose, N₂ purge time increased from 500 ms to four different values as 1, 3, 5, and 8 s while keeping the other process parameters fixed. Specifically, the sequence was 10-cycle Al₂O₃ deposition at 50 °C using 600 ms TMA pulse/ 500 ms N₂ purge/ 50 ms water pulse/ 500 ms N₂ purge and the variable was the N₂ purge time after the TMA pulse. As anticipated, increasing the N₂ purge time decreased the deposition rate by ~10x to 2.5 ± 0.2 Å/cycle and the nucleation layer became increasingly nonuniform. Ellipsometry is used to get the thickness on a companion Si pilot wafer. Longer N₂ purge times resulted in partial coverage on HOPG. Figure 3.5 shows nonuniform nucleation for four different TMA purge times. AFM images show that increasing the purge time for TMA makes the process more ALD-like rather than CVD-like.

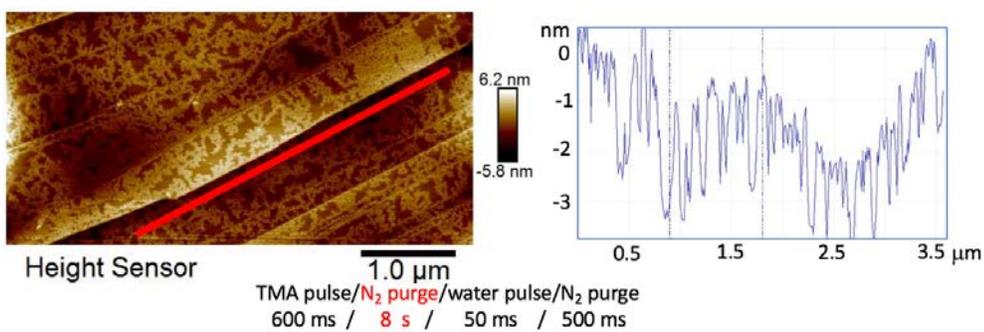
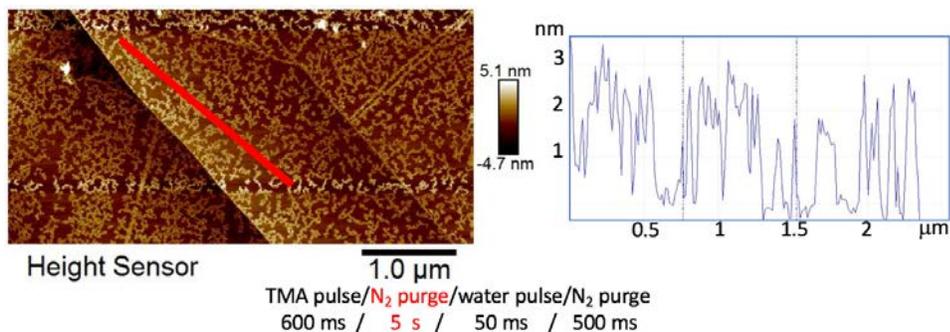
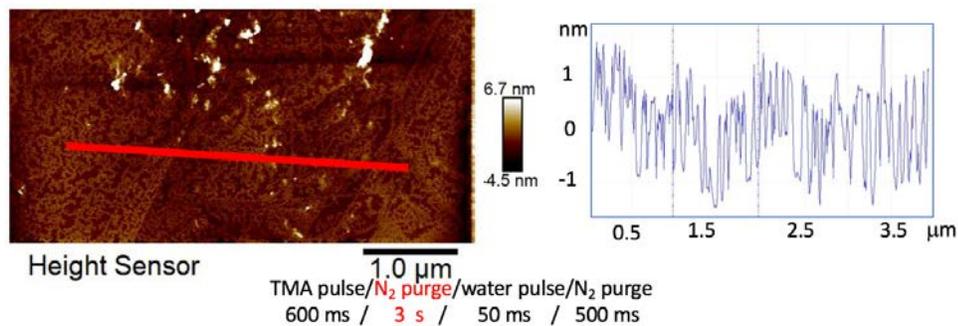
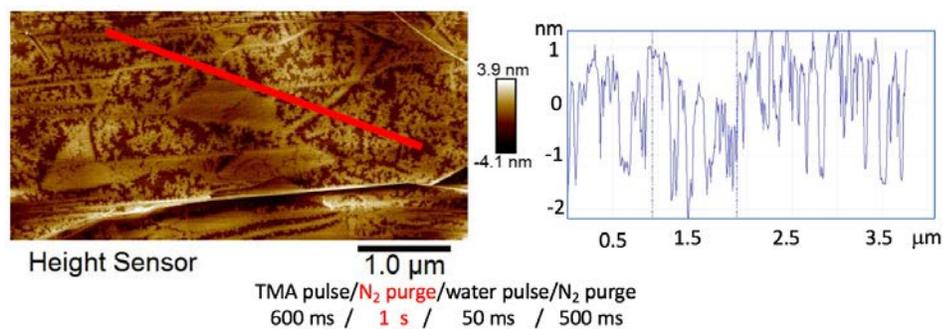


Figure 3.5. AFM images of 10-cycle Al₂O₃ deposition layer at 50 °C with increasing N₂ purge time after the TMA purge time. N₂ purge time was increased from 500 ms to 1, 3, 5, and 8 s.

3.2.2 Dependence of N₂ purge time after the H₂O pulse on Al₂O₃ nucleation on HOPG in the Savannah Cambridge 100 ALD system

In the next experiment, the N₂ purge after the TMA pulse was skipped altogether and a 10-cycle deposition was run in the sequence 600 ms TMA pulse/ 50 ms water pulse/ variable N₂ purge time. In this process, the pressure increases to ~1000 mTorr during the deposition due to pulsing TMA without an N₂ purge. Figure 3.6 shows the AFM image for this process that skipping the TMA purge leads to full nucleation all over the HOPG.

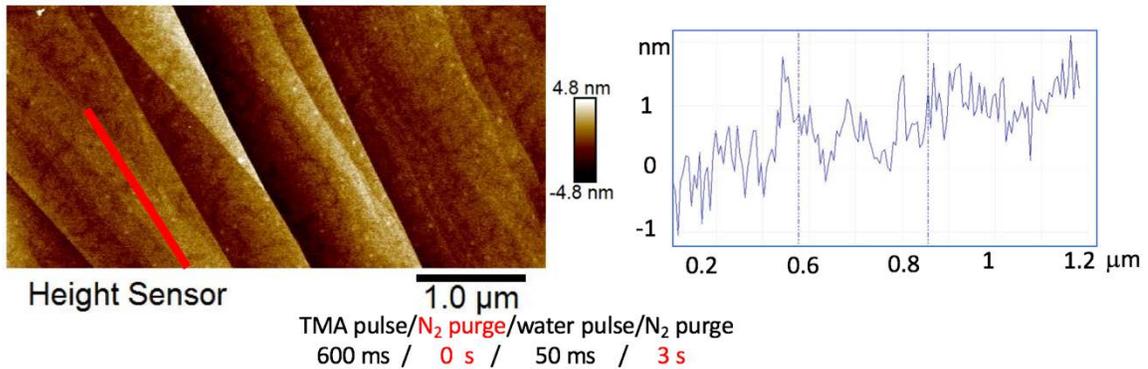


Figure 3.6. AFM image of 10-cycle Al₂O₃ deposition on HOPG at 50 °C. Skipping the TMA purge time leads to relatively complete and uniform nucleation.

Although skipping the purge time for TMA leads to full coverage, the deposition rate is relatively high around 4.6 Å/cycle. In order to decrease the deposition rate, N₂ purge time can be increased to lower the presence of H₂O before the TMA pulse. The results of increasing the water purge time from 3 s to 5 and 8 s is shown in Fig. 3.7. The deposition rate decreased from 4.6 to 4.1 and 3.7 Å/cycle, respectively. However, increasing the final

N₂ purge time resulted in more nonuniformity than observed with the 3 s N₂ purge as seen in Fig. 3.7.

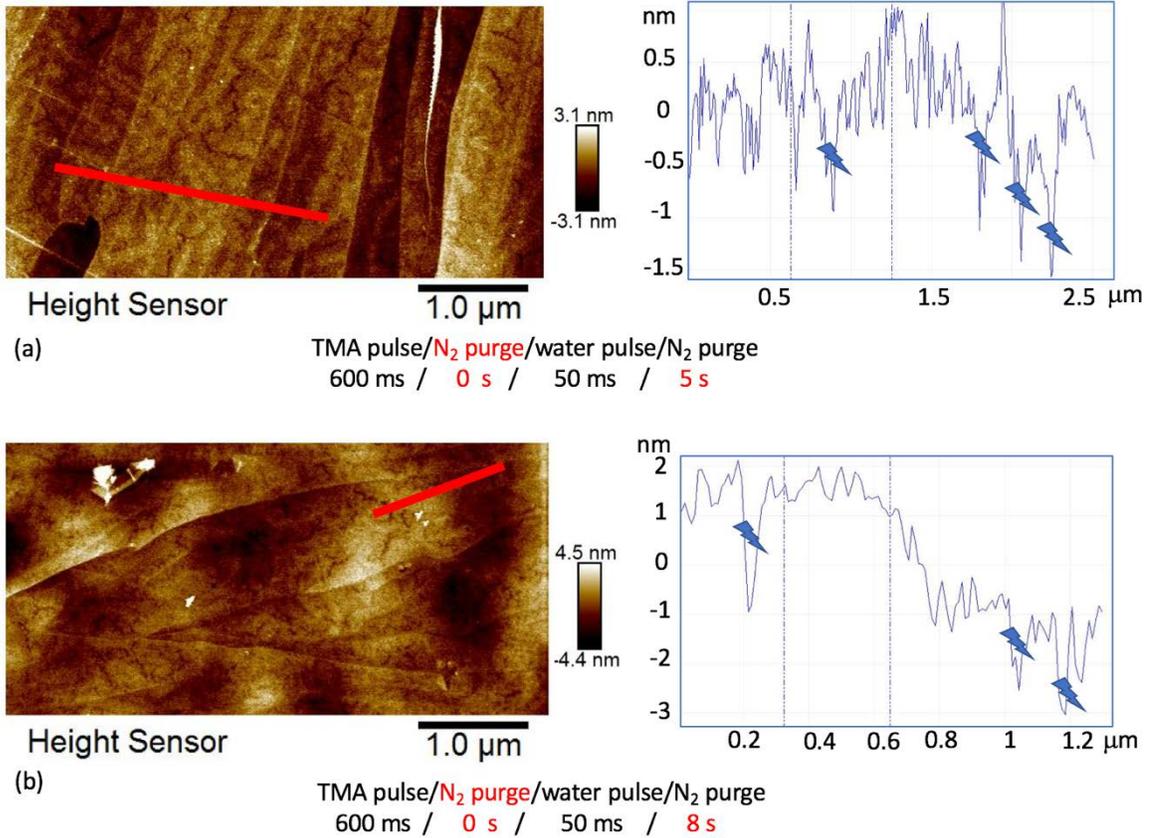


Figure 3.7. AFM image of 10-cycle Al₂O₃ deposition on HOPG at 50 °C: (a) 5 s N₂ purge after the H₂O pulse (b) 8 s N₂ purge time. Pinholes are labeled by marks in the line scan.

It can be concluded that increasing the N₂ purge time either after the TMA pulse or after the H₂O pulse results in pinhole formation on HOPG. From this growth set the best coverage was obtained with the 3 s N₂ purge time resulting in a 4.6 nm uniform Al₂O₃ nucleation layer. Decreasing the number of cycles is needed to lower the nucleation layer thickness.

3.2.3 5-cycle Al₂O₃ nucleation layer on HOPG in the Savannah Cambridge 100 ALD

To decrease the nucleation layer thickness, 5-cycle Al₂O₃ was deposited using the 4.6 Å/cycle recipe to reduce the thickness to 2.3 nm and the VASE ellipsometry measurements on a Si pilot shows a 2.8 nm nucleation layer. Figure 3.8 shows 5-cycle Al₂O₃ deposition using 600/50 ms pulse time for TMA and water and considering 3 s N₂ purge. There are many crack formations all over the HOPG. This shows that the deposition rate is not constant in early cycles of deposition. Although running 5-cycle Al₂O₃ deposition decreased the thickness to 2.8 nm, but it was not enough for providing continuously covered layer.

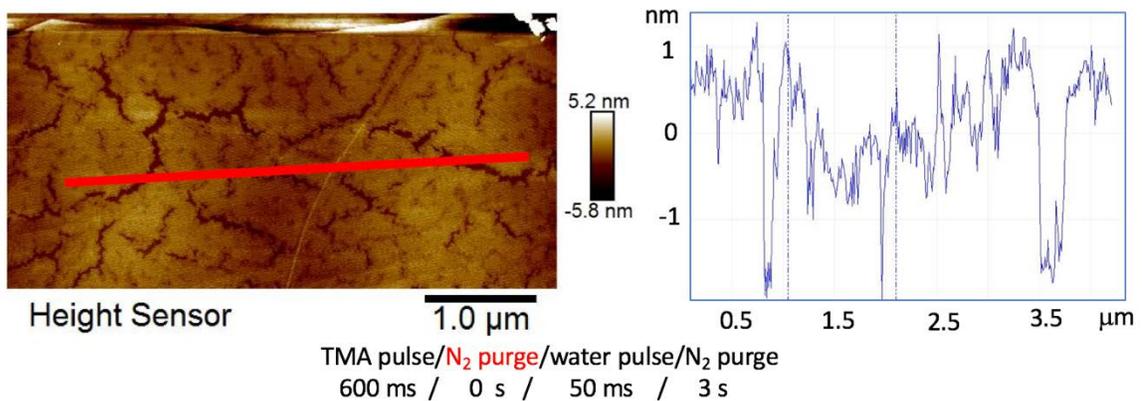


Figure 3.8. AFM image of 5-cycle Al₂O₃ deposition on HOPG at 50 °C using 600/50 ms pulse time for TMA and water with 3 s final purge.

3.2.4 Dependence of water pulse time on Al₂O₃ nucleation on HOPG in the Savannah Cambridge 100 ALD system

In this experiment, the number of cycles was kept at 5-cycle and water pulse time was increased from 50 ms to 300 and 600 ms to see if longer pulse can lead to more coverage. Figure 3.9 shows that water pulse time increases the nucleation density of Al₂O₃ on HOPG. Increasing the water pulse time to 600 ms leads to full surface coverage. A 1.5 nm film thickness is obtained for both cases.

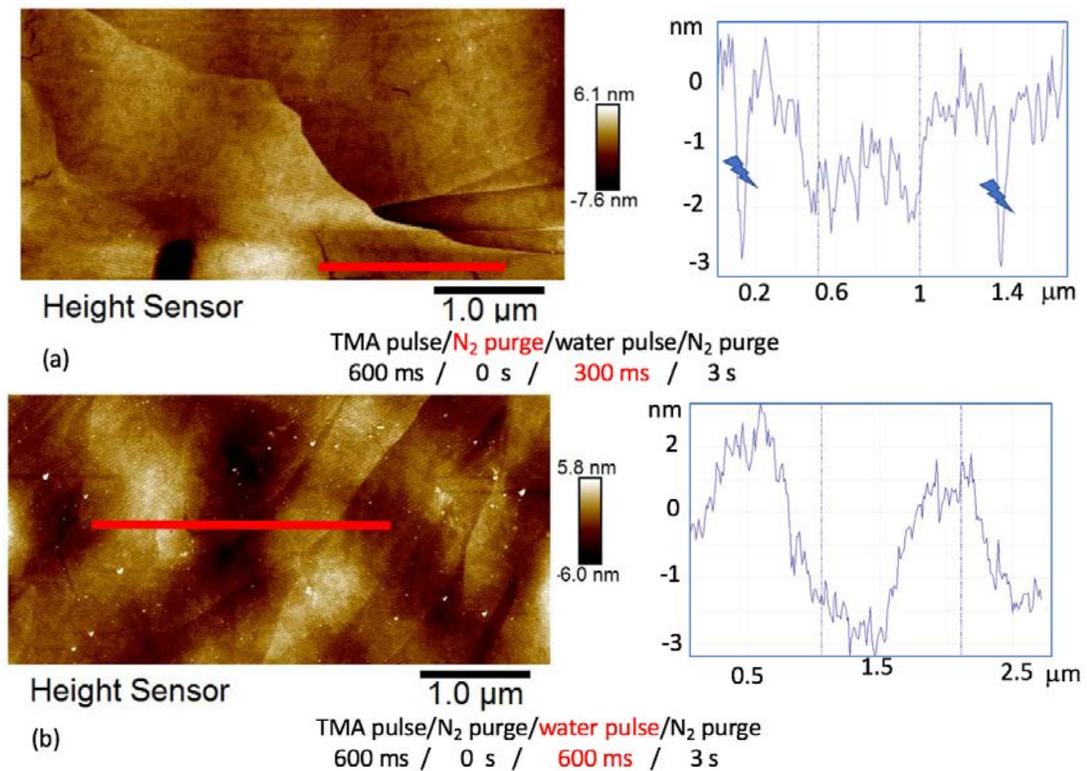


Figure 3.9. AFM images showing the surface after a 5-cycle Al₂O₃ deposition on HOPG at 50 °C: (a) 300 ms water pulse time. (b) 600 ms water pulse time. Marks on the line scans in (a) indicate cracks in the 300 ms water pulse time wafer which are not observed in the linescan of (b).

There are a few holes visible for the 300 ms water pulse time, but none apparent on HOPG for the 600 ms water pulse time. The 600 ms pulse time leads to some raised feature indicated by white spots in Fig. 3.9 (b).

In summary, a baseline recipe using TMA and water for Al₂O₃ deposition on HOPG was developed enabling nucleation at 50 °C. The best conditions are: 5-cycle Al₂O₃ with 600 ms TMA pulse/ 600 ms H₂O pulse/ 3 s N₂ purge to yield a 1.5 nm nucleation layer in the Savannah ALD system.

The next step is to nucleate the remainder of the Al₂O₃ gate oxide in a higher temperature ALD mode. For this purpose, 10 nm HfO₂ ALD was deposited on MOCVD WSe₂. FET characteristics showed negligible gate leakage current, less than 0.1 fA/μm² at 1 V, but there was hysteresis in the transfer characteristic, likely due to interface traps between the nucleation and WSe₂. This problem is mainly due to a limitation in the Savannah system. The Savannah ALD system lacks a load lock chamber, so wafers need to be unloaded and exposed to air while changing the temperatures. Since the vacuum was broken, the impurities and carbon molecules in air can adsorb on the surface leading to contamination of the surface before growth of the Al₂O₃. In order to solve this problem, the nucleation process was transferred to the Oxford ALD, which has a load lock and can accommodate the wafer while changing the temperature. Another advantages of Oxford ALD system is in situ ellipsometry which has been recently installed and makes real time thickness measurement possible. As the lowest possible temperature in Oxford Flexal ALD system is 110 °C, the recipe should be optimized at that temperature.

3.3 Deposition of Al₂O₃ on HOPG in the Oxford Flexal ALD system

The approach for developing the pulse and purge time for TMA and water was the same as discussed in the last section for the Savannah system. The process initially tested was 50-cycle Al₂O₃ using 600 ms TMA pulse/ 500 ms Ar purge/ 50 ms H₂O/ 500 ms Ar purge at 110 °C and 15 mTorr pressure. Deposition rate of 1.2 Å/cycle was recorded for Al₂O₃ in Oxford ALD that shows the coverage is fairly, see Fig. 3.10. The deposition rate is about 2.5 times smaller compared to the Savannah ALD; 3 Å/cycle was the lowest achievable rate in the Savannah system. The surface looks smooth with surface RMS roughness of 0.4 nm, but with spikes which reach from 1 to 1.5 nm. The line scan in 2.5 x 5 μm² area of AFM image shows pinhole free and smooth surface with no features that extend over the full thickness of the film, ~6 nm.

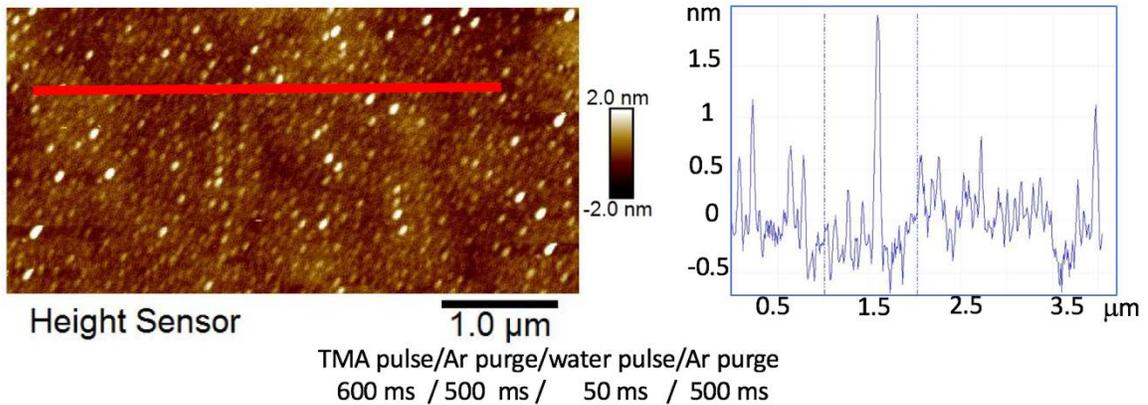


Figure 3.10. AFM image of 50-cycle Al₂O₃ deposition at 110 °C in the Oxford Flexal ALD system.

For the next experiment, 10-cycles Al_2O_3 deposition using the same recipe was performed at 110 °C on HOPG and Si substrate. The in situ ellipsometry measurement showed 1.1 nm thickness for this nucleation layer that is consistent with the deposition rate and indicated a uniform deposition rate. The surface shown in Fig. 3.11 looks smooth and pinhole free for the 10-cycle Al_2O_3 deposition. After the first 10 cycles, the wafers were transferred to the load lock for 10 minutes and temperature raised to 200 °C for the ALD process, without exposing the wafer to air. Then 100 cycles Al_2O_3 ALD at 200 °C was deposited on the nucleated layer using 30 ms TMA pulse/ 5 s Ar purge/ 2.5 s ozone pulse time/ 5 s Ar purge time. For the ALD process, Ozone was used instead of water as oxidant for Al_2O_3 deposition. This recipe was developed previously as standard recipe in Oxford ALD and resulting in a 1 Å/cycle deposition rate. Figure 3.11 shows the AFM images for both HOPG and WSe_2 after the bilayer stack with a line scan. The RMS surface roughness is 0.7 nm for WSe_2 and 0.58 nm for HOPG with no pinholes detected.

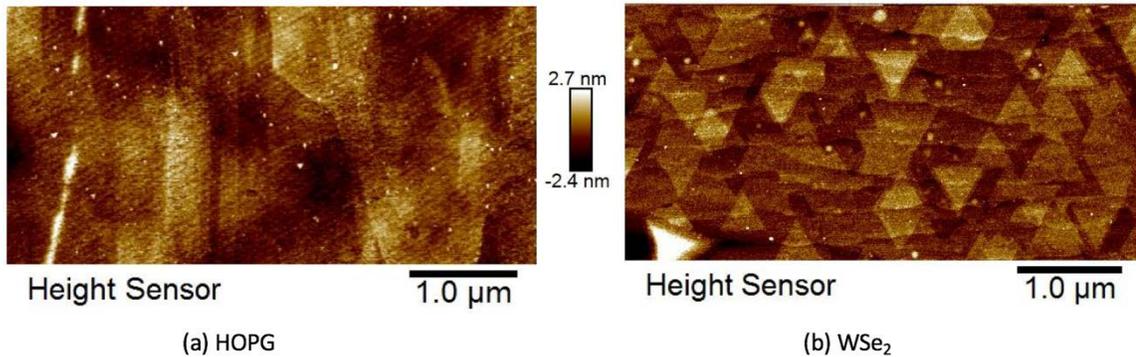


Figure 3.11. AFM image of 10-cycle Al_2O_3 deposition at 110 °C using 600 ms TMA pulse/ 500 ms Ar purge/ 50 ms H_2O pulse/ 500 ms Ar purge, following by 100 cycle Al_2O_3 ALD at 200 °C using 30 ms and 2.5 s pulse times for TMA and Ozone with 5 s purge time for each.

CHAPTER 4: TOWARD MOCVD WSe₂ TFET DEVELOPMENT

In this chapter, I demonstrate characterization of top-gated field-effect transistors (FET) which were fabricated utilizing second approach process flow (discussed in chapter 2.9) on few-layer chemical vapor deposition (CVD) WSe₂-on-sapphire. In this chapter, electrical characterization of 94 transistors with three different transistor structures is summarized.

For fabrication process, a positive bilayer resist is used in a stepper-based process for all 5 mask levels using MicroChem LOR5A on Megaposit SPR700. The first mask is used to pattern and lift-off a Ti/Au (20/30 nm) alignment mark. For the lift off and cleaning, wafers were successively soaked in 4 baths for 10 minutes each: 90°C acetone, 50°C MicroChem mr-Rem 700, 90°C isopropanol, 25°C isopropanol, then N₂ blow dry. AFM images confirm there is no resist residue. The second mask leaves the resist as an etch mask for defining the WSe₂ channels by reactive ion etching in SF₆:Ar for 10 s. This etch time is sufficient to remove the few-layer WSe₂ and expose the sapphire substrate. The sapphire provides an anchor for the S/D contacts. The third mask is used to lift off Ti/Pd (1/40 nm) S/D contacts. Mask four is used to lift off thicker Ti/Au (20/200 nm) pads and side gate electrodes for probing. An Al₂O₃ gate dielectric was deposited by atomic layer deposition (ALD) in an Oxford FlexAL ALD. The gate oxide deposition process is discussed in detail

in section 3.3, chapter 3. Low RMS roughness <1 nm was achieved on the WSe_2 after each fabrication step, indicating a clean surface. In order to dope the access regions, the Al_2O_3 was removed in 1:10 buffered HF using the gate and S/D metals as a mask. The solid polymer electrolyte PEO: CsClO_4 was drop-cast and annealed at 90°C for 3 minutes in an Ar glove box as detailed in [80]. Electrical measurements were performed in a Cascade PLC50 vacuum probe station at 1×10^{-6} Torr, at room temperature. The wafers were stored in the Ar glove box between measurements to minimize water absorption by the PEO. In this chapter, electrical characterization will be discussed mostly for transistors T1, T2, T3 labeled in Fig. 2.24.

4.1 WSe_2 -on-Sapphire FET before ion doping

Transfer and common-source characteristics are shown in Fig. 4.1(a,b) for transistor T1, with gate overlap. The transfer characteristic shows n -FET behavior with on/off current ratio exceeding 10^5 and noise-limited top-gate current. In Fig. 4.1(b) the common-source characteristic shows a sublinear turn-on resulting from the current-limiting action of the Ti/ WSe_2 Schottky contact. The measured transfer characteristics for 94 transistors on the wafer are summarized in Fig. 4.1(c) with 19 FETs in the geometry of T1, with gate overlap, and 75 in the geometry of T2 and T3, without gate overlap. The transistors with open access regions have lower current, limited by the Schottky contacts. The transistor with the highest current in Fig. 4.1(c) is the one shown in Figs. 4.1(a) and (b). To remove the variability associated with threshold voltage, V_{TH} , shifts, the threshold voltages are set to their values at $I_D/W = 0.01$ nA/ μm and the transfer characteristics are replotted as a function of overdrive voltage in Fig. 4.1(d). With V_{TH} variations removed,

I_D/W has a range I_{MAX}/I_{MIN} of approximately 12 which is closer to what is expected by W/L differences in this plot, 8. This shows that much of the variability is associated with V_{TH} shift, likely associated with substrate surface charge nonuniformity.

Cumulative distribution plots for I_D/W and V_{TH} are plotted in Figs. 4.1(e) and (f), respectively. The W/L varies by $8\times$ in these transistors, but the I_D/W cumulative distribution shows a 10-to-90% variation of $500\times$ for FETs with gate overlap, and $60\times$ for FETs without overlap. This reinforces the finding that variations beyond transistor geometry are controlling the transistor properties, including sapphire/WSe₂ surface charge, thickness uniformity, mobility, and WSe₂ background carrier density. Figure 4.1(f) shows that V_{TH} varies by volts across the wafer, consistent with the widely ranging on-currents. The particular transistors, T1, T2, and T3, selected for discussion in this section are indicated by arrows and labels on the cumulative distribution plots.

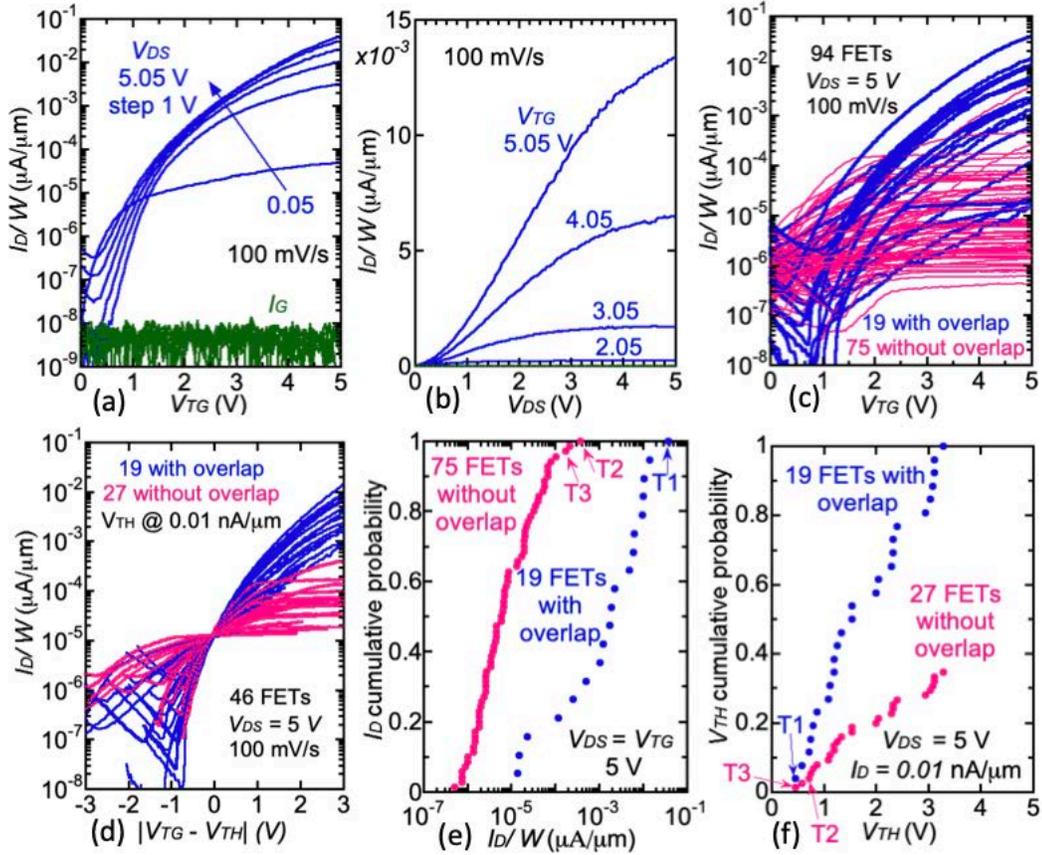


Figure 4.1. Top-gated WSe₂-on-sapphire FETs without PEO:CsClO₄. (a) Measured transfer and (b) common-source characteristics with the sapphire substrate at 0 V, for transistor T1, $W = 8 \mu\text{m}$, and $L_{TG} = 4 \mu\text{m}$. (c) Transfer characteristics for 94 FETs across the $1 \times 1 \text{ cm}^2$ wafer. (d) Drain current versus overdrive voltage for 46 FETs from 2(c) with V_{TH} defined at $I_D/W = 0.01 \text{ nA}/\mu\text{m}$. (e) Cumulative probability distribution of the drain current at $V_{DS} = V_{TG} = 5 \text{ V}$ from 2(c). (f) Cumulative probability distribution for the threshold voltage defined at a drain current of $I_D/W = 0.01 \text{ nA}/\mu\text{m}$. In (c, d, e, f) gate lengths vary from $L_{TG} = 2$ to $16 \mu\text{m}$ and include all three transistor geometries shown in Fig. 1. The particular transistors with measurements reported in this section are labeled T1, T2, and T3 in (e) and (f).

4.2 WSe₂ FET with ion doped access regions

The WSe₂ channel access regions are doped using PEO: CsClO₄ in conjunction with side gate electrodes biased to position the ions over the channel as discussed by Alessandri [81]. The Cs⁺ or ClO₄⁻ ions form electric double layers (EDLs) with electrons or holes respectively in the WSe₂. Figure 4.2 shows the transfer and common-source characteristics of transistor T3 before (blue) and after (green) application of PEO:CsClO₄. Transistor T3 has two side gates and these are both biased at 3 V to drift Cs⁺ to the exposed WSe₂ channel and induce electron conductivity. These side gate biases of 3 V are held through the course of the measurements. Before ion doping, the maximum on-current was limited to approximately 10⁻⁵ μA/μm. After ion doping, the drain current increased by four orders of magnitude (10⁻¹ μA/μm) as the Schottky contacts no longer limit the current. After ion doping, on/off current ratio increased to ~10⁴. Similarly, the common-source characteristics before ion doping show Schottky-limited currents, while after ion doping the FET turns-on linearly and saturates, Fig. 4.2(b). The measurements in Fig. 4.2 are analyzed by a PhD student, Paolo Paletti, using a 2D FET model from Marin [82] with mobility modeled after Iñíguez and Moreno [83] and Pei [84]. This model is detailed in the Appendix B and uses only 4 fitting parameters to account for the transport through both subthreshold and saturation regions.

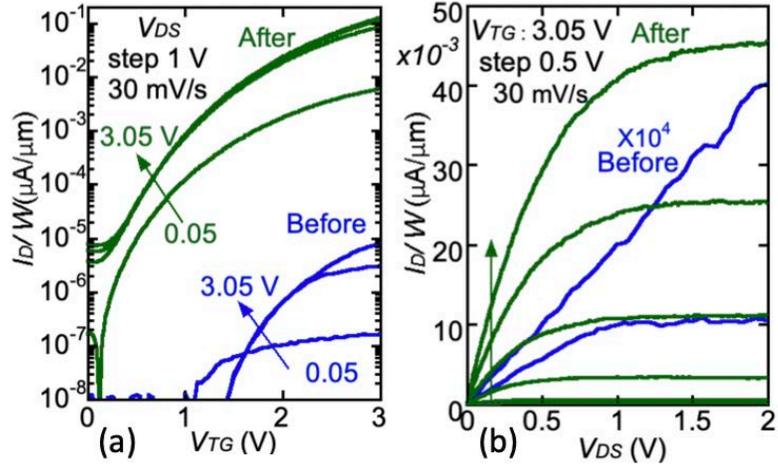


Figure 4.2: Measured n -FET characteristics for transistor T3 with $W = 8 \mu\text{m}$, $L_{TG} = 8 \mu\text{m}$, $L_A = 1 \mu\text{m}$ with a bias of 3 V applied to the two side gates: (a) transfer characteristics and (b) common-source characteristics before (blue) and after (green) ion doping.

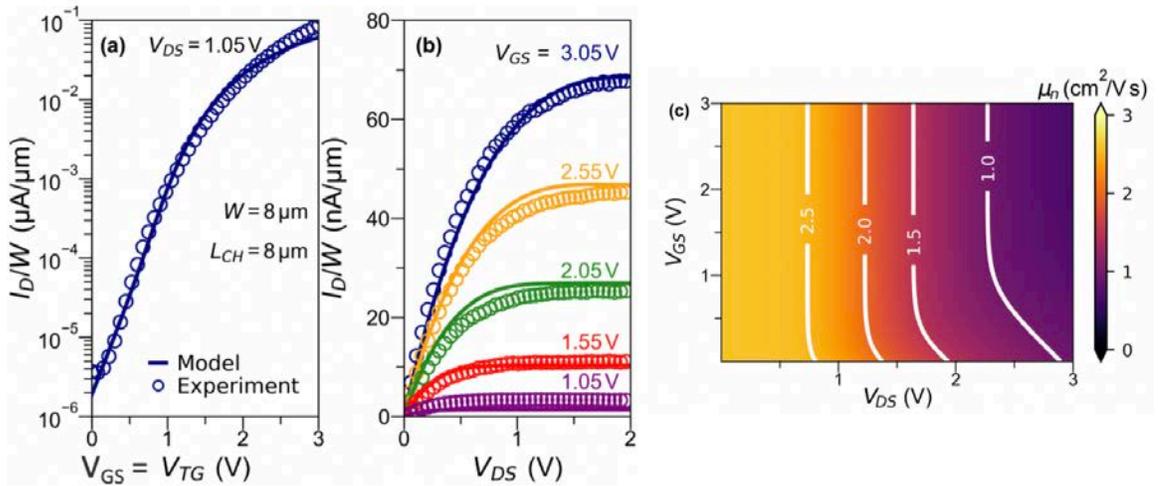


Figure 4.3: (a) Comparison of measurements (circles) and (b) simulation (lines) for the WSe_2 n -FET of Fig. 3. (c) Bias dependent electron mobility extracted from the model fits with 4 fitting parameters: $\mu_0 = 2.6 \text{ cm}^2/\text{Vs}$, $\theta^{-1} = 1.01 \text{ MV}/\text{cm}$, $v_{SAT} = 2.7 \times 10^4 \text{ cm}/\text{s}$, and $A_{TS} = 5$. Simulation by Paolo Palleti, Notre Dame.

Shown in Fig. 4.3 are the model fits showing good agreement with the measured transfer characteristics and common source characteristics. The model reveals the bias dependence of the mobility, which is shown in Fig. 4.3(c). The mobility in this CVD WSe₂ channel is found to range between 1 and 2.5 cm²/Vs. The model indicates a factor of 2× mobility decrease at large normal and longitudinal fields. These analytic mobility values are comparable to electron mobility of 16 ± 2 cm²/Vs on CVD WSe₂ FET reported by Lin [71] and recently average electron mobility of 11.2 ± 6.5 cm²/Vs on 5 CVD WSe₂ FETs gated by PEO: CsClO₄ electrolyte by Liang [85]. The square-law-model field-effect mobility, $\mu = (dI_D/dV_{GS})/[C_{ox}(W/L)V_{DS}]$, extracted from the transfer curve of Fig. 4.2(a) at $V_{DS} = 0.05$ V is 1.5 cm²/Vs.

While *n*-FET characteristics were found in transistor T3 of Figs. 4.2 and 4.3, on other transistors on this wafer it proved possible to ion dope the access regions *n* and *p*-type allowing the characterization of both *n* and *p*-FETs as shown in Fig. 4.4(a) for transistor T2. The single side gate in this transistor geometry is set to -5 V to move ClO₄⁻ ions to the channel for measurement of the *p*-FET or $+5$ V for the measurement of the *n*-FET. A 10 s hold of the side gate bias set the initial condition for the measurement before the common-source characteristics were initiated. The side gate was kept constant at either $+$ or -5 V through the measurement. The top gate bias was stepped negatively for the *p*-FET and positively for the *n*-FET. Since the ions are mobile at room temperature, one can expect the channel current to increase when the measurement is repeated because of the strengthening of the EDL with time. Three repeats are shown for each gate bias in Fig. 4.4(a) and (b) with the current increasing on each subsequent trace. The repeats are labeled 1, 2, and 3. The full-channel currents are found to be comparable for the *p* and *n*-

FET when biased under the same magnitudes.

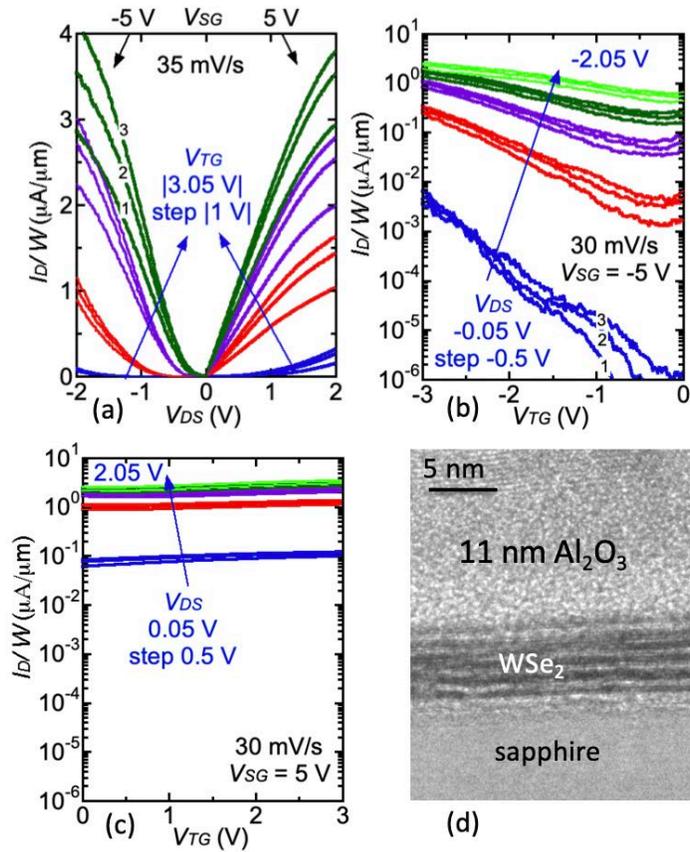


Figure 4.4: Measured WSe_2 n -FET and p -FET characteristics for T2 with $W = 8\ \mu\text{m}$, $L_{TG} = 4\ \mu\text{m}$, $L_A = 2\ \mu\text{m}$ using SG, repeated $3\times$ for each plot: (a) n -FET and p -FET common-source characteristics, (b) p -FET and (c) n -FET transfer characteristics, and (d) TEM cross section of CVD WSe_2 on sapphire with 11 nm Al_2O_3 TG oxide.

In contrast, the transfer characteristics for the p and n -FETs are shown to have

notably different subthreshold characteristics as shown in Figs. 4.4(b) and (c), respectively. The p -FET on/off current ratio biased at $V_{DS} = -0.05$ V is nearly 10^4 , but diminishes to ~ 5 at $V_{DS} = -2.05$ V. The subthreshold swing in Fig. 4.4(b) and on/off current ratio decreases as gate-source voltage is stepped to high negative voltages. This can be understood to result from the intercalation of ClO_4^- ions under the gate. The continuous accumulation of these ions with each sweep reduces the gate efficiency with time as V_{DS} is stepped from -0.05 to -2.05 V, thereby lowering the subthreshold swing and on/off ratio. A similar behavior is observed for the n -FET, but with greater degradation of subthreshold swing and on/off ratio, because of the easier intercalation of Cs^+ over ClO_4^- . This effect has previously also been observed by Alessandri [81] for Cs^+ doping of MoS_2 FETs gated with $\text{PEO}:\text{CsClO}_4$.

A transmission electron microscopy (TEM) image of CVD WSe_2 on sapphire is shown in Fig. 4.4(d). The cross section confirms the formation of an 11 nm Al_2O_3 layer on approximately 5 layers of WSe_2 on sapphire.

4.3 Ion gated FET

While the top-gate gate efficiency was degraded due to ion penetration under the gate, the ion gating can be used on the same transistor to obtain the full transfer characteristic. Figure 4.5(a) shows the measurement protocol that establishes the initial conditions and measurement sequence to obtain the transfer characteristics of the FET at room temperature using the same transistor measured in Fig. 4.4. The 5 measurement steps are labeled 1 to 5 and 1' to 5' to indicate the measurement sequence for the p -FET and n -FET, respectively. Step 1 is to ramp V_{SG} from 0 to -5 V with $V_{DS} = -0.2$ V in 1 hour to establish hole doping of the access regions. The voltages are then held steady for 40

minutes in step 2 to further strengthen the hole conductivity. Step 3 executes the transfer characteristics measurement with V_{DS} stepped from -0.1 to -1 V and V_{SG} swept between -5 and 5 V. The side gate is then returned to zero in step 4 and held constant in step 5 to re-establish the starting condition. The sequence is then repeated 3 times to assure the repeatability of the measurement as shown in Fig. 4.5(e). The second and third measurements are perfectly stable and slightly different from the first measurement.

The resultant transfer characteristic, acquired in step 3, is plotted in Fig. 4.5(b). The TG and SG currents are in the pA range and well below the drain current. Ambipolar behavior is apparent with strong and symmetric $3 \mu\text{A}/\mu\text{m}$ drain currents. The subthreshold swings are 260 and 180 mV/decade for the hole branch (left) and tunneling branch (right), respectively for $V_{DS} = -50$ mV. Although the ions are mobile at room temperature, using this protocol, repeatable measurements are achievable and no degradation in the characteristics was observed under repeated testing over a month.

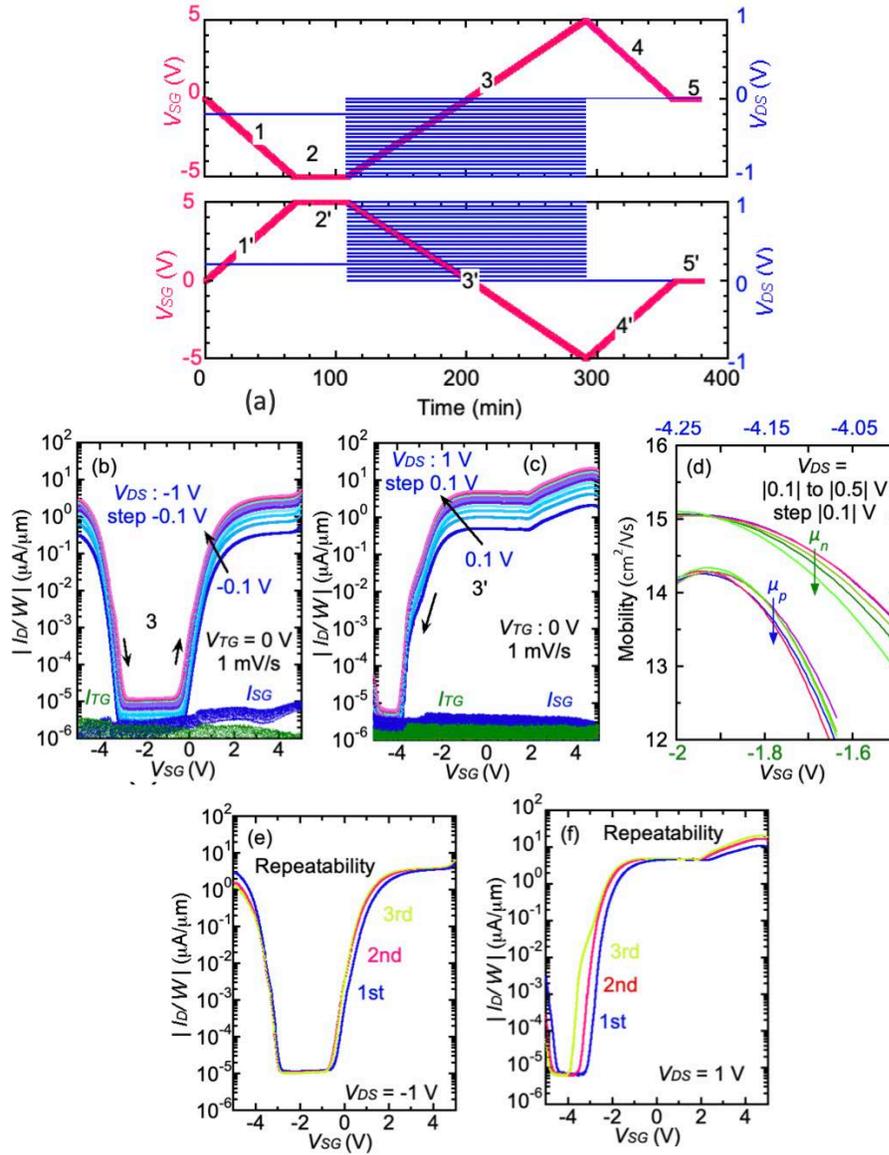


Figure 4.5: (a) Protocol for *p*-FET (top) and *n*-FET (bottom) measurement to fix the ions while sweeping the side gate voltage from -5 to 5 V for transistor T2 at room temperature, (b) *p*-FET ion gating transfer characteristics measurement at stepped drain-source voltages from -0.1 to -1 V, (c) *n*-FET ion gating transfer characteristics measurement at stepped drain-source voltages from 0.1 to 1 V, (d) the hole field-effect mobility extracted vs. side gate voltage for small V_{DS} ; the electron mobility was similarly extracted from transfer characteristics taken using an analogous protocol, (e) repeatability of *p*-FET transfer characteristics at $V_{DS} = -1$ V, and (f) repeatability of *n*-FET transfer characteristics at $V_{DS} = 1$ V.

The *n*-FET transfer characteristics is also achieved for opposite sweep direction using an analogous protocol. V_{DS} is stepped from 0.1 to 1 V and V_{SG} is ramped from 5 to -5 V, Fig. 4.5(c). Still ambipolar behavior is observed, but the hole branch is weak compare to electron branch and the current is not symmetric. This suggests when the negative bias is first applied to side gate electrode, the ClO_4^- ions move toward the channel and leads to *p*-type EDL formation. Then, by sweeping toward positive voltages, *p*-type EDL is gradually discharged (relaxed) and Cs^+ ions are attracted to the channel. Therefore, *n*-type EDL is formed. In this case, symmetric current is achieved for both *n* and *p* branches. But, when positive voltage is applied first to side gate electrode, Cs^+ ions move toward the channel and leads to strong electron branch. However, by sweeping toward negative voltages, Cs^+ ions are not completely replaced by ClO_4^- ions. Thus, weaker hole conduction is achieved. In other word, *n*-type EDL relaxation time is longer than *p*-type EDL relaxation time or longer relaxation time for Cs^+ ions. We were not able to find the reason for the existence of trenches at $V_{SG} = 2$ V in Fig. 4.5(c). Similar to *p*-FET, repeatability of the transfer characteristics is shown for three different measurements at $V_{DS} = 1$ V, Fig. 4.5(f).

The hole and electron field-effect mobilities were extracted from the transfer characteristics and are plotted vs. V_{SG} in Fig. 4.5(d). The mobilities for electrons and holes with PEO: CsClO_4 controlling the channel surface potential are larger (12 - 15 cm^2/Vs) than the mobility obtained using the top gate with Al_2O_3 (1 - 2.5 cm^2/Vs) perhaps resulting from the different interface to WSe_2 . The mobilities for these CVD films are considerably lower than reported for exfoliated WSe_2 . Fang [45] reported a hole field-effect mobility of 250 cm^2/Vs using an SiO_2 back-gate on Si, and Liu [86] reported electron field-effect

mobility of $202 \text{ cm}^2/\text{Vs}$ using an Al_2O_3 back-gate on n^+Si , indicating the higher mobility of back-gated exfoliated channels. The lower mobilities measured for CVD WSe_2 material in this work are not inconsistent with prior reports of CVD WSe_2 by Lin [71] and Liang [85].

Ion gating transfer characteristics are shown in Fig. 4.6, for (a) positive slew direction of V_{GS} and (b) for negative slew direction for transistor T3. A similar measurement protocol is used, except sweep rate is faster by $5\times$, 5 mV/s vs. 1 mV/s . Transistor T3 has two side gates and both side gate voltages were simultaneously swept from -5 to 5 V while drain-source voltage stepped from -0.05 to -1 V . The direction of side gate voltage is indicated by arrows in each plot. Similar to T2, a stronger hole branch is observed when side gates are swept from -5 to 5 V .

Subthreshold swing was extracted from the ion gating transfer characteristics in Fig. 4.6(a) for the hole and Fig. 4.6(b) for the electron branches. For the drain current less than $10^{-5} \mu\text{A}/\mu\text{m}$, a subthreshold swing less than 60 mV/decade was achieved for both electron and hole carriers, Fig 4.6(c). This steep SS can be attributed to a dynamic effect explained by Paolo Paletti in [87] attached as Appendix C. This arises from the introduction of a series resistance due to ion conduction in the $\text{PEO}:\text{CsClO}_4$.

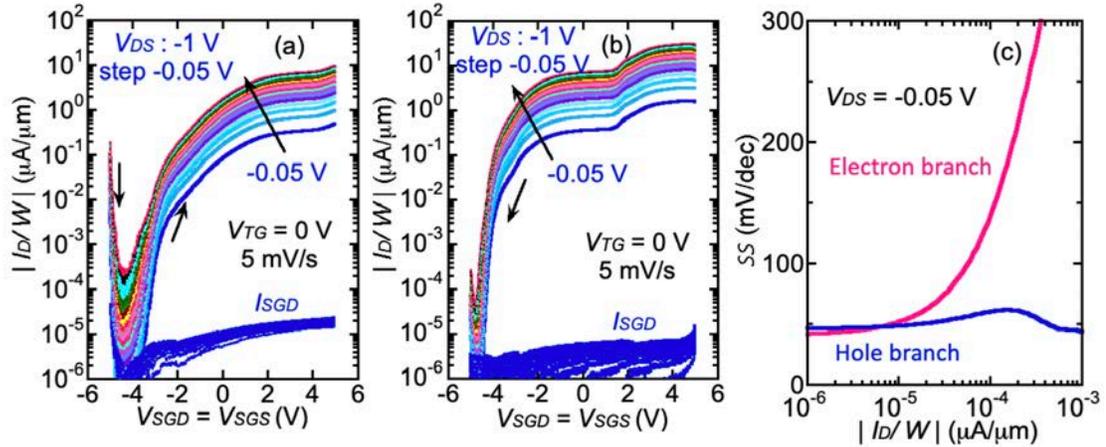


Figure 4.6: Ion gating transfer measurement for transistor T3. *p*-FET ion gating transfer characteristics measurement at stepped drain-source voltages from -0.05 to -1 V while sweeping side gate voltage from (a) -5 to 5 V and (b) 5 to -5 V, (c) subthreshold swing for hole and electron are extracted from (a) and (b), respectively.

Comparison between transfer characteristics of Fig. 4.5 and Fig. 4.6 which are on two different transistors, T2 and T3 shows that transistor T2 has a well-defined off-current region exceeding 3 V, where the current is fairly constant, while there is no similar flat region in transistor T3. The other notable difference is that the transistor with the well-defined off current region was taken at a sweep rate of 1 mV/s while the other was taken at a sweep rate of 5 mV/s. It is possible that the surface potential has not fully stabilized at each bias when the side gate is swept at the higher sweep rate, however it could also be related to unknown differences in materials or device structure between the two transistors. If the explanation that the ions have not fully stabilized at the slower sweep this could also be consistent with the observation of steep swing as discussed in Appendix C.

Another notable difference in the transistor of Fig. 4.6 is the surprising increase in current at $V_{SGD} \sim 4$ V in (a) and ~ 2 V in (b). It has the appearance of another transistor channel turning on at a threshold voltage which is approximately 2 V higher. No plausible explanation for this effect has been found.

CHAPTER 5: SUMMARY AND CONCLUSIONS

While much of the knowledge of TMD materials is based on exfoliated materials, this work has focused on large-area synthesized WSe₂ by metal organic chemical vapor deposition. A stepper-based process for FET and TFET fabrication was developed on 1 x 1 cm² WSe₂ substrates allowing characterization of multiple transistors across a wafer and ability to provide device level feedback to the growers in Prof. Josh Robinson's group at Penn State University.

As a start point in this research, assessment of received WSe₂ samples were the first and critical step before transistor fabrication, since the presence of tall agglomerates (taller than 10 nm) on WSe₂ sample led to short through gate oxide grown by ALD. Atomic force microscopy revealed the presence and density of these defects and the conditions were subsequently revised to take the density to less than 0.1 x 10⁸ cm⁻², a level suitable for batch fabrication.

An ALD technique for nucleation of oxides on WSe₂ was developed consisting of a low temperature physical vapor deposition step to initiate nucleate Al₂O₃ followed by a higher temperature ALD deposition to complete the formation. Deposition temperature, pulse and purge times for each precursor, and deposition rate were investigated to establish conditions suitable for ALD nucleation on WSe₂. Low temperature deposition (110°C in

Oxford ALD system), longer pulse time (600 and 50 ms for TMA and H₂O, respectively), shorter purge time (500 ms for each precursor), and low deposition rate (1.2 Å/cycle) were required to achieve smooth surface with RMS roughness of 0.4 nm and less than 0.1 fA/μm² leakage current at 1 V.

Two masks sets were developed in the course of this research, the first being a four-level mask set for FET and TFETs using an Autostep 200 i-line lithography system. Contact anchoring was one of the primary challenges faced in fabrication. Since WSe₂ weakly bonds to sapphire, probing contacts that are on top of the WSe₂ and that do not have any connection to the sapphire, results in delamination of the WSe₂ making repeated probing difficult. Despite the difficulty in probing results were achieved in the first mask set process.

WSe₂ FETs showed on/off current ratio exceeding 10³ at $V_{DS} = 3.05$ V and $V_{GS} = 5$ V with noise floor limited gate current with a Schottky-limited current density of 1.1 nA/μm. This is the first report of the characteristics of a top-gated WSe₂-on-sapphire FET. As a comparison, the only other top-gated report on CVD WSe₂ was grown on SiO₂ with a 50 nm Al₂O₃ dielectric by ALD [73]. In comparison with the *n*-FET reported, the WSe₂-on-sapphire FETs shows factor of 100× improvement in the reported *n*-FET on SiO₂ on-current and on-currents comparable to the reported *p*-FET at a factor 10× lower gate bias. WSe₂-on-sapphire does not permit back-gate biasing as the gate thickness is the thickness of the substrate. This means the contact resistance cannot be improved by back gate bias, so access region doping is needed to lower the contact resistance.

While transistors were demonstrated using the first process, the process was not reliable and yield was low. This was especially apparent when the gate oxide was removed

in the access regions to allow doping with PEO:CsClO₄. TEM cross sectional images revealed that strain in the S/D contacts could be the cause of contacts pulling off and disconnecting the devices. A revision to the process was prepared in which a thin metallization (1 nm Ti, 40 nm Pd) was made to anchor the S/D contact in a local region to the mesa, followed by a second patterning and metallization (20 nm Ti, 200 nm Au) with thicker metallization for probing. This added an additional mask level and resulted in the redesign of the full mask set which resulted in devices which could withstand repeated and stable testing over months.

As an example of the robustness of the process, on one set which characterized extensively the first 94 devices tested ALL were functional in that they yielded transfer characteristics without any open circuits or anomalous behavior. On this same set on/off current ratio exceeding 10^5 at room temperature with noise floor limited gate current and contact limited current density of 15 nA/ μm for FETs using a structure in which gate overlaps the source and drain contacts. In two other transistors geometries with open access regions, ion doping using PEO:CsClO₄ was used to induce electron and hole conductivity in the access regions of the WSe₂ channel. The on-current increased by four orders of magnitude with on/off current ratio greater than 10^6 at $V_{DS} = -0.05$ V.

Analytic 2D FET modeling by doctoral student Paolo Paletti showed that the current-voltage characteristic from subthreshold to saturation could be fully described. From this model the field-dependent electron mobility could be described and it was found to range from 1 to 2.6 cm²/Vs. This is part of a manuscript in preparation and included as Appendix E. In this paper we demonstrate the first report of a top-gated CVD few-layer WSe₂-on-sapphire FET and analyze the findings.

Measurements of WSe₂ FETs were made that show subthreshold swing less than 60 mV/decade in a WSe₂-on-sapphire FETs. This was thought to be somehow an artifact of the measurements, related to ion dynamics and our ability to reach equilibrium as we were sweeping the measurement. This mechanism was explained by Paolo Paletti as arising from ionic delay, the result was presented at the DRC and is included as an Appendix C.

The main purpose of this investigation was to use atomically thin WSe₂ channels for TFET applications. To achieve sub 60 mV/decade in TFET, the EOT likely needs to be pushed below 1 nm. This means further development of the gate nucleation process. Also, all the electrical measurements shown in this research were performed at room temperature. In order to use ions in a practical application they need to be immobilized by cooling the device. Ions in PEO are therefore not suitable for room temperature operation and methods are still needed to form abrupt *p-n* tunnel junctions for the TFET.

APPENDIX A:
FET AND TFET PROCESS FLOW

Process Summary:

- Formation of alignment marks:
 - Photolithography using LOR 5A¹ (under layer) + SPR 700² (positive tone PR)
 - Pattern using Mask #1 (*Alignment*) (Autostep 200)
 - Metal evaporation and lift-off 20/30 nm Ti/Au
- Mesa formation:
 - Photolithography using LOR 5A (under layer) + SPR 700 (positive tone PR)
 - Pattern using Mask #2 (*Channel*) (Autostep 200)
 - Anisotropic etch on surface with reactive ion etching (RIE)
- Formation of thin source/drain contacts (This step is in the five-level masks approach):
 - Photolithography using LOR 5A (under layer) + SPR 700 (positive tone PR)
 - Pattern using Mask #3 (*S/D*) (Autostep 200)
 - Metal evaporation and lift-off: 1/40 nm Ti/Pd
- Formation of thick pads and side gates:
 - Photolithography using LOR 5A (under layer) + SPR 700 (positive tone PR)
 - Pattern using Mask #4 (*S/D*) (Autostep 200)
 - Metal evaporation and lift-off: 20/200 nm Ti/Au
- Gate oxide deposition:

¹<http://microchem.com/pdf/PMGI-Resists-data-sheetV-rhccedit-102206.pdf>.

²http://docs.capitolscientific.com/manufacture/dow_electronic_materials/datasheets/SPR700_Photoresist.pdf.

- Photolithography using LOR 5A (under layer) + SPR 700 (positive tone PR)
 - Pattern using Mask #3 (*S/D*) (Autostep 200)
 - Oxide deposition
 - Formation of gate contacts:
 - Photolithography using LOR 5A (under layer) + SPR 700² (positive tone PR)
 - Pattern using Mask #4 (*Gate*) (Autostep 200)
 - Metal evaporation and lift-off: 20/80 nm Ti/Au
- I. Formation of alignment marks:
- a. Photolithography
 - i. Spin on LOR5A
 1. Speed: 4000 RPM
 2. Accel: 500 RPM/s
 3. Time: 30 s
 4. Target thickness: 450 nm
 - ii. Pre-processing bake:
 1. Temperature: 180 °C
 2. Time: 180 s
 - iii. Spin-on [MEGAPOSIT SPR 700-1.2 positive-tone photoresist (PR)]
 1. Speed: 4000 RPM
 2. Accel: 500 RPM/s
 3. Time: 30 s
 4. Target thickness: 1.2 μm
 - iv. Hot plate pre-exposure bake for evaporating solvents
 1. Temperature: 90 °C
 2. Time: 45 s
 - v. Exposure (*Autostep 200*)
 1. Mask #1: *Alignment*
 2. Exposure time: 0.28
 - vi. Develop to remove unexposed resist
 1. Developer: (caustic) AZ 917 Metal-Ion Free (MIF)³
 - a. Time: 45 s
 2. DI rinse
 - a. Time: 10 s
 - vii. Microscope inspection using *Olympus MX61* optical microscope
 - b. Metallization

³<https://wcam.engr.wisc.edu/Public/Safety/SDS%20%20GHS/SDS%20ECOPY/AZ%20917%20MIF%20Developer.pdf>.

(FC1800 #1 evaporator)

Add (10/100 nm) Ti/Au Alignment Marks

- Ti Flash: keep shutter closed during initial Ti evaporation to lower pressure and remove impurities
Was Ti Flash performed? YES
Record final pressure: $<5e-7$ mbar

i. Ti Deposition

1. Initial Pressure: $\leq 5 \times 10^{-7}$ mbar
2. Deposition Rate: 1.5 A/s
3. Final Thickness: 20 nm
4. Beam Voltage: 10 kV
5. Beam Current: 30 mA
6. Final Pressure: $\leq 4-7$ mbar
7. Frequency: 3 Hz

ii. Au Deposition

1. Initial Pressure: $\leq 5e-7$ mbar
2. Deposition Rate: 3 A/s
3. Final Thickness: 30 nm
4. Beam Voltage: 10.2 kV
5. Beam Current: 100 mA
6. Final Pressure: $\leq 8e-7$ mbar
7. Frequency: 3 Hz

iii. Lift-Off

1. Photoresist Removal
 - a. Solvent 1: Hot Aceton⁴(ACE), to remove photoresist. (5 min)
 - b. Solvent 2: Hot mr rem700, to remove LOR5A (10 mins) followed by 5 min hot Isopropanol (IPA)⁵
2. Microscope inspection using *Olympus MX61* optical microscope
- c. Surface study by AFM

⁴(CH₃)₂CO (Acetone) – Semiconductor Grade, BDH Acetone, Distributed exclusively by VWR International.

⁵Isopropanol 2-Propanol, for CMOS Avantor Performance Materials.

- II. Mesa formation
 - a. Photolithography, the same as alignment mark
 - b. Reactive ion etching (anisotropic etch process)
 - (*PlasmaTherm 790 Series* reactive ion etcher (RIE))
 - i. Place sample in RIE
 - I. Pressure: 10 mTorr
 - II. Gases/Flow:
 - a. (15sccm / SF₆)
 - b. (10 sccm / Ar)
 - III. Etch Time: 10 s
 - IV. RF Power: ≤100 W
 - V. DC voltage: ~252 V
 - ii. Microscope inspection
 - c. Resist removal
 - I. Photoresist Removal
 - a. Solvent 1: 90°C Acetone (ACE), to remove photoresist. (10 min)
 - b. Solvent 2: 50°C mr rem700, to remove LOR5A (10 mins)
 - c. Solvent 3: 90°C IPA
 - d. Solvent 3: Room temperature IPA to remove remaining Acetone
 - II. Microscope inspection using *Olympus MX61* optical microscope
 - d. Surface study by AFM
- III. Formation of thin source/drain contacts:
 - a. Photolithography
 - b. Microscope inspection:
 - (*Olympus MX61* optical microscope)
 - c. Metallization
 - (*FC1800 #1* evaporator)
 - Add (1/180 nm) Ti/Pd
 - Ti Flash: keep shutter closed during initial Ti evaporation to lower pressure and remove impurities
 - Was Ti Flash performed? YES
 - Record final pressure: ≤5e-7 mbar, and time: 60 (s)
 - i. Ti Deposition
 - 1. Initial Pressure: ≤ 5 x 10⁻⁷ mbar
 - 2. Deposition Rate: 1 Å/s
 - 3. Final Thickness: 1 nm
 - 4. Beam Voltage: 10 kV

- 5. Beam Current: 10 mA
- 6. Final Pressure: $\leq 4 \times 10^{-7}$ mbar

ii. Pd Deposition

- 1. Initial Pressure: $\leq 5 \times 10^{-7}$ mbar
- 2. Deposition Rate: 3 A/s
- 3. Final Thickness: 40 (Thin deposition)
- 4. Beam Voltage: 10 kV
- 5. Beam Current: 15 mA
- 6. Final Pressure: $\leq 8 \times 10^{-7}$ mbar

iii. Lift-Off

iv. Microscope inspection using *Olympus MX61* optical microscope

d. Surface study by AFM

IV. Formation of thick pads/side gates:

- a. Photolithography
- b. Microscope inspection:
(*Olympus MX61* optical microscope)
- c. Metallization
(*FC1800 #1* evaporator)
Add (1/180 nm) Ti/Au

- Ti Flash: keep shutter closed during initial Ti evaporation to lower pressure and remove impurities
Was Ti Flash performed? YES
Record final pressure: $\leq 5 \times 10^{-7}$ mbar, and time: 60 (s)

i. Ti Deposition

- 1. Initial Pressure: $\leq 5 \times 10^{-7}$ mbar
- 2. Deposition Rate: 1 A/s
- 3. Final Thickness: 20 nm
- 4. Beam Voltage: 10 kV
- 5. Beam Current: 10 mA
- 6. Final Pressure: $\leq 4 \times 10^{-7}$ mbar

ii. Pd Deposition

- 1. Initial Pressure: $\leq 5 \times 10^{-7}$ mbar
- 2. Deposition Rate: 3 A/s
- 3. Final Thickness: 200 (Thick deposition) nm
- 4. Beam Voltage: 10 kV
- 5. Beam Current: 15 mA
- 6. Final Pressure: $\leq 8 \times 10^{-7}$ mbar

iii. Lift-Off

iv. Microscope inspection using *Olympus MX61* optical microscope

d. Surface study by AFM

V. Gate oxide deposition:

- a. 1 nm Al₂O₃ nucleation layer at 110 °C in Oxford Flexal ALD
 - I. Base pressure: 15 mTorr
 - II. TMA pulse/ Ar purge/ H₂O pulse/ Ar purge: 600 ms/ 500 ms/50 ms/ 500 ms
 - III. Number of cycle: 10
 - IV. Unload the sample in load lock to change the temperature to 200 °C for ALD process
- b. 10 nm Al₂O₃ ALD at 200 °C in Oxford Flexal ALD:
 - I. Base pressure: 15 mTorr
 - II. TMA pulse/ Ar purge/ Ozone pulse/ Ar purge: 30 ms/5 s/2.5 s/ 5 s
 - III. Number of cycle: 100

VI. Formation of gate contacts:

- a. Photolithography
- b. Microscope inspection:
(*Olympus MX61* optical microscope)
- c. Metallization

(*FC1800 #1* evaporator)

Add (20/80 nm) Ti/Au

- Ti Flash: keep shutter closed during initial Ti evaporation to lower pressure and remove impurities
Was Ti Flash performed? YES
Record final pressure: $\leq 5 \times 10^{-7}$ mbar, and time: 60 (s)

v. Ti Deposition

1. Initial Pressure: $\leq 5 \times 10^{-7}$ mbar
2. Deposition Rate: 1 A/s
3. Final Thickness: 20 nm
4. Beam Voltage: 10 kV
5. Beam Current: 10 mA
6. Final Pressure: $\leq 4 \times 10^{-7}$ mbar

vi. Au Deposition

1. Initial Pressure: $\leq 5 \times 10^{-7}$ mbar
2. Deposition Rate: 2.5 ~ 3 A/s
3. Final Thickness: 80 nm
4. Beam Voltage: 10 kV
5. Beam Current: 20 mA
6. Final pressure: $\leq 8 \times 10^{-7}$ mbar

- 7. mbar
 - vii. Lift off
 - d. Surface study by AFM

- VII. Oxide removal in access region for doping purpose
 - a. Immersing the wafer in Buffer HF (1:10) for 10 s
 - b. 20 S DI water rinse
 - c. Surface study by AFM

- VIII. Drop casting PEO: CsClO₄
 - a. Anneal the wafer at 125 °C for 10 minutes in glove box
 - b. Let it cool for 4 minutes
 - c. Drop cast PEO: CsClO₄
 - d. Wait 10 minutes
 - e. Anneal the sample at 90 °C for 3 minutes.

APPENDIX B:
2D FET MODEL

A 2D FET model was developed by doctoral student Paolo Paletti to further our quantitative understanding of the transistor characteristics. This model is described in a paper prepared for submission to the IEEE Transactions on Electron Devices, which is attached as Appendix E.

The fundamental relation between the gate voltage, V_{GS} , and the position-dependent quasi-Fermi levels, E_{Fn} , and electron sheet carrier density, n_{2D} , can be written

$$\left(1 + \frac{C_{IT}}{C_{OX}}\right) k_B T \ln \left[\exp \left(\frac{n_{2D}(x)}{N_{2D}} \right) - 1 \right] + \frac{q^2 n_{2D}(x)}{C_{OX}} = q(V_{GS} - V_{TH}) + E_{Fn}(x) - E_{FS} \quad (\text{B.1})$$

with interface trap capacitance density C_{IT} , TG oxide capacitance density C_{OX} , Fermi level $E_{Fn}(x)$, Fermi level at the source E_{FS} , threshold voltage V_{TH} , degenerate quantum sheet carrier density $N_{2D} = k_B T g_V g_S (m_C^* m_O / 2\pi \hbar^2)$, with Boltzmann constant k_B , temperature T , valley g_V and spin g_S degeneracies, electron effective mass m_C^* , electron mass m_O , and reduced Planck's constant \hbar . Following the derivation of Marin [82], an expression for the drain current, I_D , under the gradual channel approximation is given by

$$I_D = -q\mu_{EFF} \frac{W}{L} V_T \int_{n_{2D,S}}^{n_{2D,D}} n_{2D}(x) \left[\frac{\left(\frac{\gamma}{N_{2D}} + \frac{1}{N_{OX}} \right) \exp\left(\frac{n_{2D}(x)}{N_{2D}} \right) - \frac{1}{N_{OX}}}{\exp\left(\frac{n_{2D}(x)}{N_{2D}} \right) - 1} \right] dn_{2D}(x) \quad (\text{B.2})$$

where the thermal voltage $V_T = k_B T/q$, electron densities at the drain and source are $n_{2D,D}$ and $n_{2D,S}$, respectively, $\gamma = 1 + C_{IT}/C_{OX}$, and $N_{OX} = C_{OX} V_T/q$. The electron mobility μ_{EFF} is modeled after Iñíguez and Moreno [83] and Pei [84] to include semiempirically the dependence on the lateral and normal electric fields, $\mu_{EFF} = \mu/(1 + \mu V_{D,EFF}/v_{SAT} L)$, $L = L_{TG}$, and relations for the effective drain voltage $V_{D,EFF}$ and the saturated velocity v_{SAT} given by

$$V_{D,EFF} = V_{SAT} - V_{SAT} \frac{\ln\left[1 + \exp\left(A_{TS}(1 - V_{DS}/V_{SAT})\right)\right]}{\ln\left[1 + \exp\left(A_{TS}\right)\right]} \quad (\text{B.3})$$

$$V_{SAT} = -\frac{Lv_{SAT}}{\mu} + \sqrt{\left(\frac{Lv_{SAT}}{\mu}\right)^2 + \frac{2Lv_{SAT}Q_S}{\mu C_{OX}}} \quad (\text{B.4})$$

The dimensionless factor A_{TS} connects the triode and saturation regions. The drain-field mobility is given by $\mu = \mu_0/(1 + \theta E_\perp)$, where μ_0 is the effective zero-field mobility, θ is a mobility degradation factor accounting for increased scattering at large gate bias, and E_\perp is the vertical electric field, $E_\perp = (Q_S + Q_D)/2\epsilon_{2D}$. Finally, the source Q_S and drain Q_D charges are simply qn_{2D} at the S and D ends, respectively, with perpendicular WSe₂ dielectric constant $\epsilon_{2D} = 6$. With just four fitting parameters, μ_0 , θ^{-1} , v_{SAT} , and A_{TS} , the model

is able to effectively describe the experimental results both above and below threshold, in the triode region as well as in saturation. Other physical parameters needed for the computation are summarized below.

TABLE B.1.
MODEL CONSTANTS

t_{OX}	11 nm	$C_{OX} = \epsilon_{OX}/t_{OX}$	0.56 $\mu\text{F}/\text{cm}^2$
ϵ_{OX}	7	$C_{IT} = q^2 D_{IT}$	2.88 $\mu\text{F}/\text{cm}^2$
V_{TH}	2.4 V	N_{OX}	9.1E10 cm^{-2}
D_{IT}	1.8E13 $\text{cm}^{-2}\text{eV}^{-1}$	N_{2D}	2.27E13 cm^{-2}
m_c^*	0.35	g_v, g_s	6, 2

APPENDIX C:
STEEP SUBTHRESHOLD SWING ORIGINATING FROM GATE DELAY

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Steep Subthreshold Swing Originating from Gate Delay

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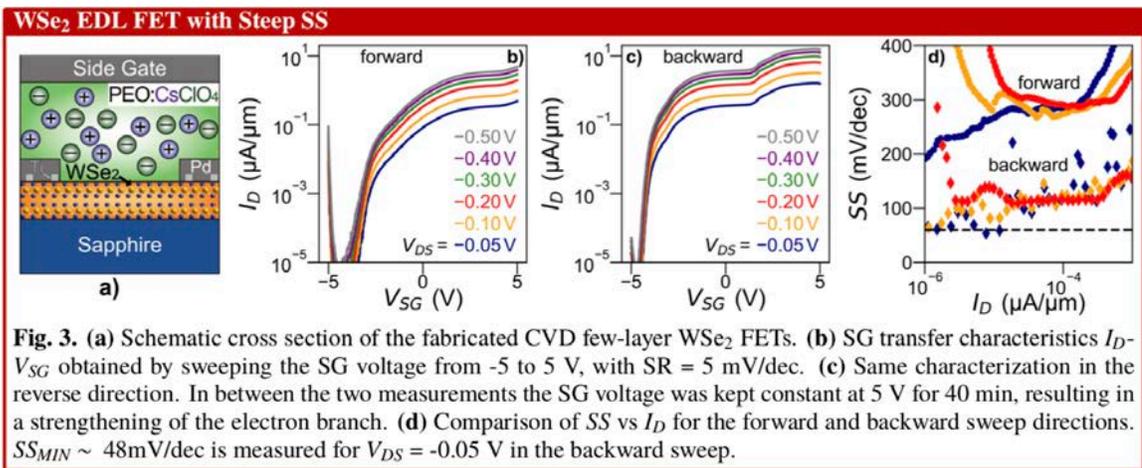
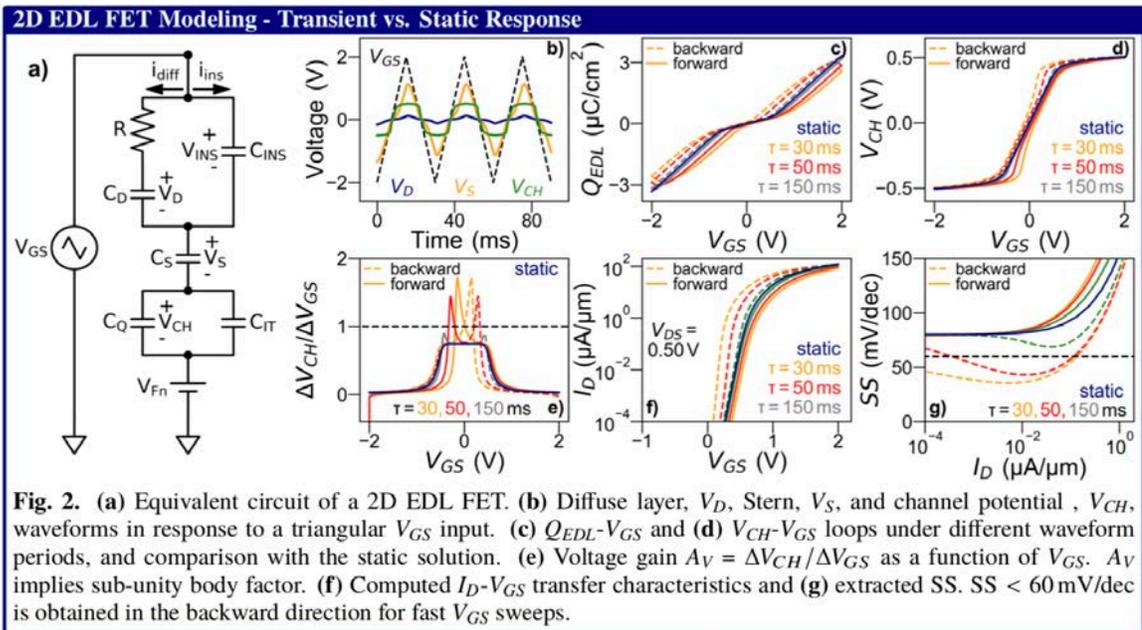
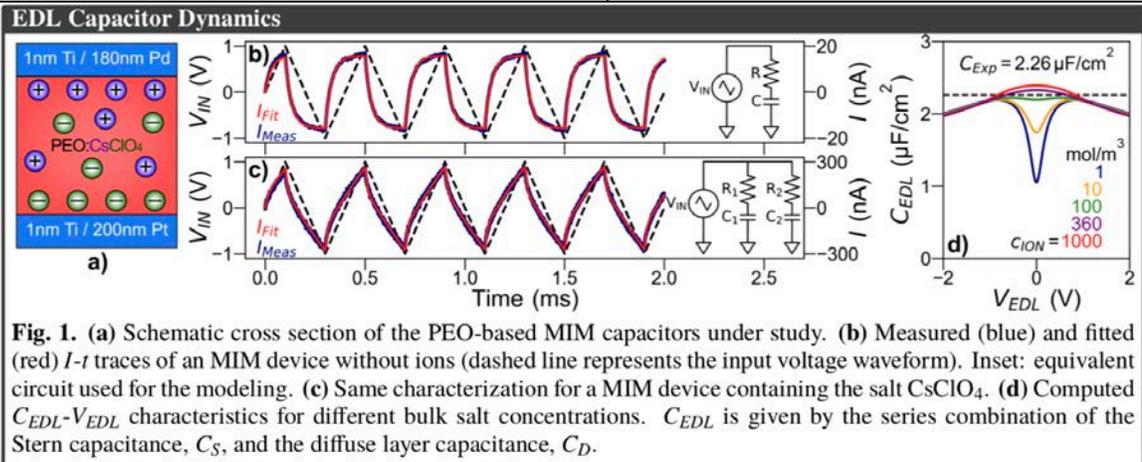
Apparent Steep Subthreshold Swing. Complex gate dielectrics are being widely explored to provide voltage amplification leading to steep subthreshold swing (SS) in transistors [1]. Here we show that hysteretic steep SS can arise simply from the introduction of a series resistance in the gate of a metal-oxide-semiconductor field-effect transistor (MOSFET), i.e. as a dynamic effect. The choice of measurement slew rate (SR) and slew direction then directly affects the measured SS as has been previously reported [2]. We use an ionic polymer gate dielectric to illustrate how the series resistance arises from the ionic conductance controlling the time response of the electric double layer (EDL) at the polymer/metal [3] or polymer/semiconductor interface [4]. While the ionic polymer in an EDL transistor is used to illustrate the effects, the principles apply generally to other complex insulating gates including ferroelectrics and piezoelectrics.

EDL Capacitor Dynamics. We first show that in a polyethylene oxide (PEO)-based metal-insulator-metal (MIM) capacitor with drop-cast PEO thickness of $\sim 1 \mu\text{m}$, the RC response of the dielectric is controlled by the ionic conductivity of the PEO. Two capacitors were fabricated, one with pure PEO and one containing the salt CsClO_4 (ether oxygen to Cs^+ molar ratio of 76:1, corresponding to an ion concentration of $\sim 2.2 \times 10^{20} \text{ cm}^{-3}$). In response to a triangular waveform of amplitude of $\pm 1 \text{ V}$, with a period of $400 \mu\text{s}$, the dynamic response of the pure PEO capacitor is well described by a simple RC equivalent circuit stemming from EDLs formed by background OH^- and H^+ ions. The dynamic response of the second PEO capacitor with CsClO_4 exhibits a time evolution characterized by two distinct time constants, with 16x higher current. Fitting to those measurements can be used to extract the R and C components. The slow response is a result of the low conductance of the Cs^+ and ClO_4^- ions in PEO, in series to an EDL capacitance density C_{EDL} of $2.26 \mu\text{F}/\text{cm}^2$. More rigorously, C_{EDL} results from the series combination of the Stern layer and diffuse layer capacitance [5], analytical modeling of the bias dependence of the EDL differential capacitance show that it depends on the salt concentration and can be nonmonotonic.

Two-Dimensional (2D) EDL FET Modeling – Transient vs. Static Response. An analytic model of the ionic polymer gate on a 2D FET has been implemented to explore the dynamic behavior of the combination. The equivalent circuit of the gate dielectric is readily captured by a series resistance represented by a series RC circuit shunted by the geometrical capacitance of the polymer dielectric, C_{INS} , on a generic 2D FET [6]. The FET electrostatics is described by a quantum capacitance, C_Q , and an interface trap capacitance which accounts for deviations from ideality in the subthreshold regime. The model reveals the partitioning of voltage drops across the diffuse layer, V_D , the Stern layer, V_S , and the 2D channel, V_{CH} . The lag induced by the gate time constant opens up a $Q_{EDL}-V_{GS}$ hysteresis loop that widens for decreasing waveform periods while decreasing the maximum charge density accumulated within the EDL. Dynamics are also revealed in the $V_{CH}-V_{GS}$ relation, where it is interesting to note that during the backward sweep, due to a decrement in the total gate capacitance within the subthreshold region, the voltage gain ($A_V = \Delta V_{CH}/\Delta V_{GS}$) exceeds unity, an indication of a sub-unity body factor. The computed current for an nFET ($W/L = 1$, $\mu_n = 100 \text{ cm}^2/\text{Vs}$) reveals that SS becomes less than 60 mV/dec in the backward sweep becoming steeper as sweep rate is increased, while the extent of the sub-60 region expands.

WSe₂ EDL FET with Steep SS. Multilayer WSe₂ EDL FETs were fabricated following the process described in [7] and the same PEO:CsClO₄ ionic gate was utilized. In this transistor a side gate (SG) electrode was employed to record the I_D-V_{GS} transfer characteristics. First the SG was swept from -5 to 5 V with a SR of 5 mV/s to show a Schottky barrier FET characteristic exhibiting ambipolar transport and strong electron conduction ($I_D \sim 4.8 \mu\text{A}/\mu\text{m}$ for $V_{SG} = 5 \text{ V}$, and $V_{DS} = -0.05 \text{ V}$). After a hold time of 40 minutes, the backward sweep was recorded displaying a clear counterclockwise hysteresis. The SS is more than 3x steeper in the reverse direction with a $SS_{MIN} \sim 48 \text{ mV/dec}$ at low currents ($V_{DS} = -0.05 \text{ V}$). Similarly, for the hole branch the delayed discharge of the hole/ ClO_4^- EDL results in a $SS < 50 \text{ mV/dec}$. In summary, we show that apparent SS less than 60 mV/dec can result simply from gate delay. In measurement of SS, care must be taken to ensure that SS does not depend on SR or slew direction.

[1] H. Agarwal <i>et al.</i> , <i>IEEE-EDL</i> , vol. 39, p. 1254, (2018).	[2] H. Wang <i>et al.</i> , <i>IEDM Tech. Dig.</i> , p. 31-1, (2018).
[3] T. Asano <i>et al.</i> , <i>ACS Appl. Mater. Interfaces</i> , vol. 9, 5056 (2017).	[4] K. Xu <i>et al.</i> , <i>ACS Appl. Mater. Interfaces</i> , 10, 43166 (2018).
[5] M. S. Kilic <i>et al.</i> , <i>Phys. Rev. E</i> , vol. 75, p. 021503, (2007).	[6] E. G. Marin <i>et al.</i> , <i>IEEE-TED</i> , vol. 65, p. 1239, (2018).



APPENDIX D:
SUPERCAPACITY ($>1000 \mu\text{F}/\text{CM}^2$) CHARGE RELEASE IN A CVD-GROWN WSe_2
FET INCORPORATING A PEO:CSClO₄ SIDE GATE

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Supercapacity ($>1000 \mu\text{F}/\text{cm}^2$) charge release in a CVD-grown WSe₂ FET incorporating a PEO:CsClO₄ side gate

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We report extraordinarily high capacitance density in tungsten diselenide (WSe₂) field-effect transistors (FETs) capped with polyethylene oxide (PEO) and ion doped with cesium perchlorate (CsClO₄). The FETs have 3-4 monolayer WSe₂ channels grown by chemical vapor deposition (CVD) using W(CO)₆ and H₂Se at 800 °C for 30 minutes [1]. A stepper-based process was used to fabricate the transistors and an 11 nm Al₂O₃ atomic layer deposited (ALD) gate dielectric was formed on the WSe₂ with a low temperature nucleation layer, 1 nm Al₂O₃, deposited at 110 °C to facilitate nucleation followed by a 10 nm Al₂O₃ deposited at 200 °C, after Kwak [2]. The *n*-FET achieves an ON/OFF ratio of 10⁶ with noise-floor-limited gate current. Most prior studies of WSe₂ FETs have been on exfoliated materials and to our knowledge there is only one prior report of a top-gated CVD WSe₂ *p*-FET [3]. Following FET characterization PEO:CsClO₄ was drop-cast and annealed at 90 °C for 3 minutes in Ar after Xu [4], yielding a layer thickness of 400 nm as measured by transmission electron microscopy (TEM). Ion gating using a side gate (6 μm from the WSe₂ mesa edge) produces ambipolar transfer characteristics with approximately equal ON-currents of 2 μA/μm attributed to the multi-work-function source/drain contacts [5]. ON/OFF current ratio exceeds 10⁶ with field-effect electron and hole mobilities of 10 and 25 cm²/Vs respectively and subthreshold swings of 260 and 180 mV/decade respectively. Atomic force microscope images show that the WSe₂ nucleates in triangles which are apparent in Fig. 1; FET characteristics after testing of the transistor are shown in Fig. 2 along with TEM.

Supercapacitance findings. We carefully control the measurement protocol when using polymer ion gating, to establish the initial conditions and repeatability. A representative measurement sequence, used to obtain the ambipolar transfer characteristic of the FET is shown in Fig. 3 where the side gate voltage V_{SG} and drain source voltage V_{DS} vs. time are plotted; this sequence is controlled by a B1500 semiconductor parameter analyzer with the measurement divided into five panels. In the first panel V_{SG} is ramped from 0 to -5 V with $V_{DS} = -0.2$ V and top gate voltage $V_{TG} = 0$. The resultant drain current I_D is plotted in panel 1. The negative V_{SG} moves ClO₄⁻ ions to the WSe₂ channel and induces hole conductivity. The side gate voltage is then held constant in panel 2 to show that the anion-hole electric double layer (EDL) continues to strengthen with time. Panel 3 then executes the transfer characteristic measurement; as V_{SG} is ramped, V_{DS} is stepped. Panel 4 shows the drain current dependence as all measurement terminals are returned to zero to reset the measurement for subsequent repeats. With all voltages returned to zero, one would expect all currents to be zero. However, in panel 5, with all measurement terminals set to zero, I_D is positive with a decay time constant of approximately 95 minutes, at room temperature. Another surprising phenomena, the source current I_S is approximately equal and opposite to I_D . By integrating the current transient, the stored charge Q can be determined and by using the top gate as a Kelvin probe it is possible to estimate the voltage $\Delta V \sim 0.5$ V across the polymer/semiconductor charge storage layer. The capacitance density is then $Q/\Delta V$ per unit area. It is not clear whether the charge is stored, primarily over the WSe₂ mesa, $8 \times 8 \mu\text{m}^2$, or encompassing the source drain pads, $15,800 \mu\text{m}^2$. Using the larger number as a conservative estimate the capacitance density is found to exceed $1000 \mu\text{F}/\text{cm}^2$. This is much too high to be explained by the EDL capacitance density of $10 - 20 \mu\text{F}/\text{cm}^2$. This charge release is repeatable and easily reproduced in other transistors on the wafer. If the polarity of the V_{SG} ramp is reversed to end the sequence by driving ClO₄⁻ ions to the WSe₂ surface no charge release is observed. Charge storage of this type could be used for transistor self-biasing or circuit powering.

Acknowledgments This research was supported in part by the Center for Low Energy Systems Technology (LEAST) sponsored by MARCO and DARPA. **References:** [1] Lin et al., *ACS Nano* 12, 965 (2018). [2] I. Kwak et al., *ECS Transactions* 75, 143 (2016). [3] Y. Gong et al., *J. Electron. Mater.* 45, 6280 (2016). [4] H. Xu et al. *ACS Nano* 9, 4900 (2015). [5] S. Fathipour et al., *J. Appl. Phys.* 120, 234902 (2016).

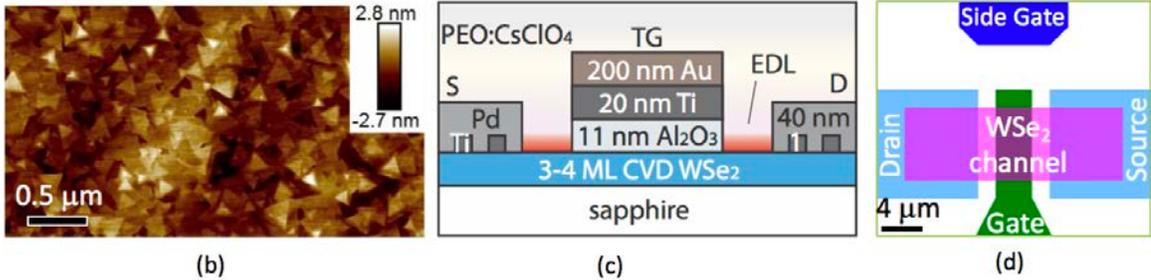


Fig. 1. Top-gated CVD WSe₂ FET: (a) atomic force micrograph of WSe₂ surface, (b) transistor cross section and (c) transistor top view with $W = 8 \mu\text{m}$, $L_G = 4 \mu\text{m}$, $L_A = 2 \mu\text{m}$.

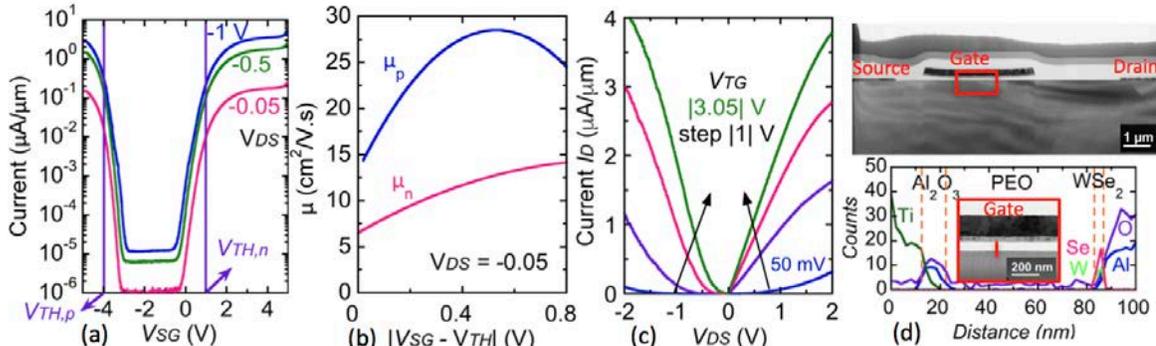


Fig. 2. (a) Room temperature transfer characteristics for three different drains-source voltages, (b) mobility extraction, (c) common-source characteristics, and (d) transmission electron microscopy of FET along with energy dispersive spectroscopy under gate area. Measurements were performed in a Cascade PLC50 vacuum probe station at 1.2×10^{-6} Torr, at room temperature.

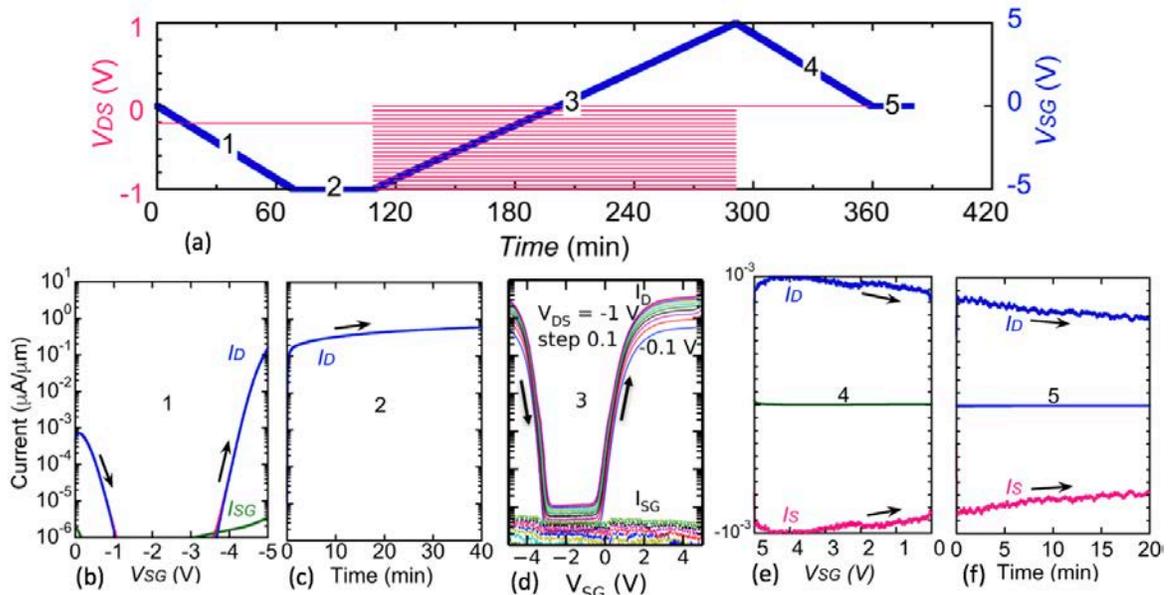


Fig. 3. (a) Protocol for FET measurement at room temperature to fix the ions, (b) setting the ions by sweeping the side gate from 0 to -5 V , (c) stabilizing the ions by applying -5 V to side gate electrode for 40 minutes, (d) transfer measurement at stepped drain-source voltages from 0 to -1 V , (e) ramping all terminal voltages to 0 V, and (f) extraordinary current sourcing and sinking with a time constant of 99 minutes. This characteristic is repeatable and reproducible and observed in FETs across the wafer.

APPENDIX E:
WSe₂-ON-SAPPHIRE FIELD-EFFECT TRANSISTORS GROWN BY CHEMICAL
VAPOR DEPOSITION

Manuscript in preparation for *IEEE Transactions on Electron Devices*.

WSe₂-on-sapphire field-effect transistors grown by chemical vapor deposition

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Abstract— Stepper-based batch fabrication of top-gated field-effect transistors (FETs) is demonstrated on few-layer WSe₂-on-sapphire grown by chemical vapor deposition (CVD). This paper reports electrical characterization of 94 transistors with three different transistor structures. On/off current ratio exceeding 10⁵ at room temperature with noise floor limited gate current and contact limited current density of 15 nA/μm was achieved for FETs using a structure in which gate overlaps the source (S) and drain (D) contacts. Two other transistors with open access regions are used to allow ion doping using PEO:CsClO₄ to induce electron and hole conductivity in access regions. The on-current increased to four orders of magnitude with on/off current ratio greater than six orders of magnitude at $V_{DS} = -0.05$ V compare to before ion doping. An analytic 2D FET model was refined and applied to extract a true field-effect mobility and its gate and drain field dependence. The fit of the measured characteristics from subthreshold to saturation is made with only 4 fitting parameters revealing a field dependent electron mobility ranging from 1 to 2.6 cm²/Vs.

Index Terms— field-effect transistor, polyethylene oxide, PEO:CsClO₄, chemical vapor deposition, tungsten diselenide, WSe₂.

I. INTRODUCTION

Transistors based on two-dimensional semiconductor channels are being widely developed for applications in electronics [1]. Among the transition metal dichalcogenides (TMDs), WSe₂ has been identified by Sylvia [2] as having the best mix of properties for field-effect transistors (FETs) operated at low voltage, 0.3 V, and at the limits of gate length scaling, $L_G = 5.9$ nm. Simulations by Sylvia indicate that WSe₂ should deliver ~9× higher drive current vs. ultrathin Si FETs at 0.3 V. Tungsten diselenide transistor development to date has largely utilized exfoliated materials, but deposited channels formed by molecular beam epitaxy (MBE) [3], chemical vapor deposition (CVD) [4, 5, 6, 7, 8, 9, 10], and atomic layer deposition (ALD) [11] are widely desired. Methods for forming top gate stacks on WSe₂ and MoS₂ [12] FETs are reported on exfoliated channels, but to our knowledge there is only a single report of a CVD WSe₂ channel with a top gate; channel mobility was ~0.01 cm²/Vs for this growth on SiO₂ [8]. Beyond CVD WSe₂ there are a few reports of CVD MoS₂ with a top gate. Alharbi reported a carrier mobility of 50–60 cm²/Vs on

monolayer CVD MoS₂ using HfOx as the top gate oxide [13]. Similar carrier mobility, around 30 cm²/Vs was reported for a top-gated CVD MoS₂ FET by Sun [14] and Kang [15]. In this paper we analyze the transport properties of top-gated CVD WSe₂ FETs grown on sapphire. Polymer ion doping using polyethylene oxide: cesium perchlorate (PEO:CsClO₄) is used to dope the FET access regions and minimize the effects of the Schottky contacts. An analytic model of the FET is in good agreement with the experimental transfer and common-source characteristics and reveals the bias dependence of the carrier mobility. Because the WSe₂ is grown on ~1 x 1 cm² wafers, a stepper lithographic process is utilized allowing the device-to-device variations to be reported.

II. DEVICE STRUCTURES

The WSe₂ was grown by chemical vapor deposition [9] using W(CO)₆ and H₂Se at 800 °C for 30 minutes leading to 3-4 monolayers of WSe₂ on sapphire. Annealing the sapphire substrates prior to growth creates terraces to enhance nucleation and promote uniform WSe₂ coverage [9]. Figure 1(a) shows an atomic force microscope (AFM) image of the WSe₂ on sapphire revealing triangular WSe₂ submicron grains that have coalesced into a polycrystalline WSe₂ film.

Three different transistor structures were fabricated and these are labeled T1, T2 and T3 in Fig. 1 and shown in (b, c) cross sections and in (d, e, f) top-view layouts. Transistor T1 has the gate overlapping the source and drain; transistors T2 and T3 have the gate positioned between the source and drain with access regions on either side of the gate. Transistors T2 and T3 have one or two side gates, respectively, which are used as field plates to control the access region carrier type and conductivity as will be explained with the measurements. In Fig. 1(e) the label SG means single-side gate; in (f) SGS refers to the side gate on the source side, and SGD, the side gate on the drain side. The labels S, D, and TG refer to source, drain, and top gate. The gate width is 8 μm on all the transistors with gate lengths of 1, 2, 4, 8, and 16 μm. For each of these gate lengths, access region lengths of 1, 2, 3 and 6 μm have been characterized.

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III. DEVICE FABRICATION

A positive bilayer resist is used in a stepper-based process for all 5 mask levels using MicroChem LOR5A on Megaposit SPR700. The first mask is used to pattern and lift-off a Ti/Au (20/30 nm) alignment mark. For the lift off and cleaning,

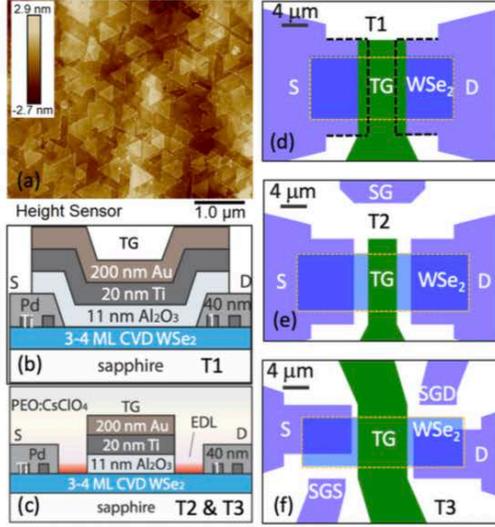


Figure 1: (a) AFM image of WSe_2 on sapphire, (b) cross section of transistor T1 with 2 μm gate overlap, (c) cross section of transistors T2 and T3 with access regions colored in (c) to indicate the accumulation of ions at the WSe_2 surface to form an electric double layer (EDL) with induced carriers in the WSe_2 . The ions are positioned by an electric field controlled by side gates shown in (e) and (f). Dimensionally accurate top-view layouts of the three transistors T1, T2, and T3, respectively. The WSe_2 mesa is indicated by tan dashed line; the black dashed line in (d) indicate the S and D contact edges which extend under the gate.

wafers were successively soaked in 4 baths for 10 minutes each: 90°C acetone, 50°C MicroChem mr-Rem 700, 90°C isopropanol, 25°C isopropanol, then N_2 blow dry. AFM images confirm there is no resist residue. The second mask leaves the resist as an etch mask for defining the WSe_2 channels by reactive ion etching in SF_6/Ar for 10 s. This etch time is sufficient to remove the few-layer WSe_2 and expose the sapphire substrate. The sapphire provides an anchor for the S/D contacts. The third mask is used to lift off Ti/Pd (1/40 nm) S/D contacts. Mask four is used to lift off thicker Ti/Au (20/200 nm) pads and side gate electrodes for probing; these are not shown in Fig. 1(c-e-f). The use of a two-mask process for S/D contacts and pads was adopted because a single thick S/D metallization tended to cause the WSe_2 to detach at the metal/channel edge, apparently due to strain in the metal.

An Al_2O_3 gate dielectric was deposited by atomic layer deposition (ALD) in an Oxford FlexAL ALD. The gate oxide deposition process starts with a 1 nm Al_2O_3 nucleation layer

deposited at 110 °C followed by a 10 nm Al_2O_3 deposition at 200 °C, after Kwak [16]. The TG is formed by evaporation of Ti/Au (20/200 nm) using the fifth mask. Low RMS roughness <1 nm was achieved confirmed on the WSe_2 after each fabrication step, indicating a clean surface. In order to dope the access regions, the Al_2O_3 was removed in 1:10 buffered HF using the gate and S/D metals as a mask. The solid polymer electrolyte PEO:CsClO₄ was drop-cast and annealed at 90 °C for 3 minutes in an Ar glove box as detailed in [17]. Electrical measurements were performed in a Cascade PLC50 vacuum probe station at 1×10^{-6} Torr, at room temperature. The wafers were stored in the Ar glove box between measurements to minimize water absorption by the PEO.

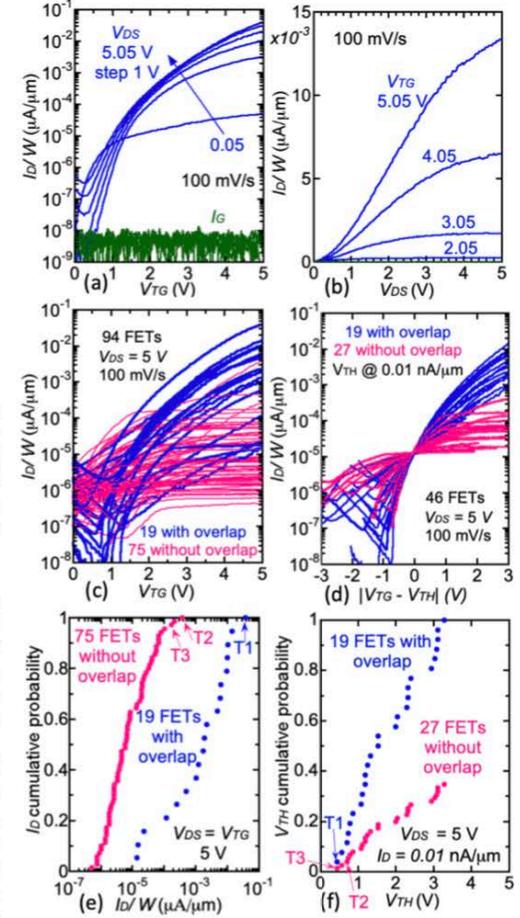


Figure 2: Top-gated WSe_2 -on-sapphire FETs without PEO:CsClO₄. (a) Measured transfer and (b) common-source characteristics with the sapphire substrate at 0 V, for transistor T1, $W = 8 \mu\text{m}$, and $L_{TG} = 4 \mu\text{m}$. (c) Transfer characteristics for 94 FETs across the $1 \times 1 \text{ cm}^2$ wafer. (d) Drain current versus overdrive voltage for 46 FETs from 2(c) with V_{TH} defined at $I_D/W = 0.01 \text{ nA}/\mu\text{m}$. (e) Cumulative probability distribution of the drain current at $V_{DS} = V_{TG} = 5 \text{ V}$

from 2(c). (f) Cumulative probability distribution for the threshold voltage defined at a drain current of $I_D/W = 0.01$ nA/ μm . In (c, d, e, f) gate lengths vary from $L_{TG} = 2$ to 16 μm and include all three transistor geometries shown in Fig. 1. The particular transistors with measurements reported in this paper are labeled T1, T2, and T3 in (e) and (f).

IV. WSe₂-ON-SAPPHIRE FET

Transfer and common-source characteristics are shown in Fig. 2(a, b) for transistor T1, with gate overlap. The transfer characteristic shows n -FET behavior with on/off current ratio exceeding 10^5 and noise-limited top-gate current. In Fig. 2(b) the common-source characteristic shows a sublinear turn-on resulting from the current-limiting action of the Ti/WSe₂ Schottky contact. The measured transfer characteristics for 94 transistors on the wafer are summarized in Fig. 2(c) with 19 FETs in the geometry of T1, with gate overlap, and 75 in the geometry of T2 and T3, without gate overlap. The transistors with open access regions have lower current, limited by the Schottky contacts. The transistor with the highest current in Fig. 2(c) is the one shown in Figs. 2(a) and (b). To remove the variability associated with threshold voltage, V_{TH} , shifts, the threshold voltages are set to their values at $I_D/W = 0.01$ nA/ μm and the transfer characteristics are replotted as a function of overdrive voltage in Fig. 2(d). With V_{TH} variations removed, I_D/W has a range I_{MAX}/I_{MIN} of approximately 12 which is closer to what is expected by W/L differences in this plot, 8. This shows that much of the variability is associated with V_{TH} shift, likely associated with substrate surface charge nonuniformity.

Cumulative distribution plots for I_D/W and V_{TH} are plotted in Figs. 2(e) and (f), respectively. The W/L varies by $8\times$ in these transistors, but the I_D/W cumulative distribution shows a 10-to-90% variation of $500\times$ for FETs with gate overlap, and $60\times$ for FETs without overlap. This reinforces the finding that variations beyond transistor geometry are controlling the transistor properties, including sapphire/WSe₂ surface charge, thickness uniformity, mobility, and WSe₂ background carrier density. Figure 2(f) shows that V_{TH} varies by volts across the wafer, consistent with the widely ranging on-currents. The particular transistors, T1, T2, and T3, selected for discussion in this paper are indicated by arrows and labels on the cumulative distribution plots.

V. WSe₂ FET WITH ION-DOPED ACCESS REGIONS

The WSe₂ channel access regions are doped using PEO:CsClO₄ in conjunction with side gate electrodes biased to position the ions over the channel as discussed by Alessandri [18]. The Cs⁺ or ClO₄⁻ ions form electric double layers (EDLs) with electrons or holes respectively in the WSe₂. Figure 3 shows the transfer and common-source characteristics of transistor T3 before (blue) and after (green) application of PEO:CsClO₄. Transistor T3 has two side gates and these are both biased at 3 V to drift Cs⁺ to the exposed WSe₂ channel and induce electron conductivity. These side gate biases of 3 V are held through the course of the measurements. Before ion doping, the maximum on-current was limited to approximately 10^{-5} $\mu\text{A}/\mu\text{m}$. After ion doping, the drain current increased by four orders of magnitude (10^{-1} $\mu\text{A}/\mu\text{m}$) as the Schottky contacts no longer limit the current. After ion doping, on/off current ratio increased to $\sim 10^4$. Similarly, the common-source characteristics

before ion doping show Schottky-limited currents, while after ion doping the FET turns-on linearly and saturates, Fig. 3(b).

The measurements in Fig. 3 are analyzed using a 2D FET model from Marin [19] with mobility modeled after Iñiguez

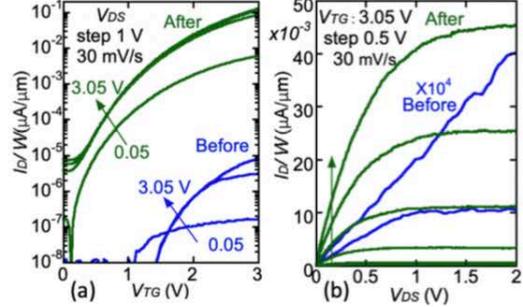


Figure 3: Measured n -FET characteristics for transistor T3 with $W = 8$ μm , $L_{TG} = 8$ μm , $L_A = 1$ μm with a bias of 3 V applied to the two side gates: (a) transfer characteristics and (b) common-source characteristics before (blue) and after (green) ion doping.

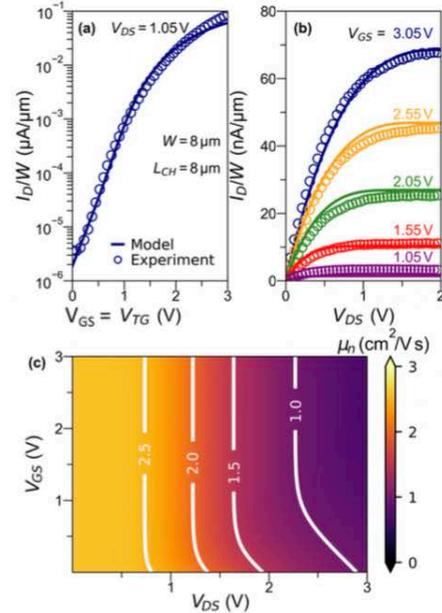


Figure 4: (a) Comparison of measurements (circles) and (b) simulation (lines) for the WSe₂ n -FET of Fig. 3. (c) Bias dependent electron mobility extracted from the model fits with 4 fitting parameters: $\mu_0 = 2.6$ cm^2/Vs , $\theta^{-1} = 1.01$ MV/cm, $v_{s,0} = 2.7 \times 10^4$ cm/s, and $A_{TS} = 5$.

and Moreno [20] and Pei [21]. This model is detailed in the Appendix and uses only 4 fitting parameters to account for the transport through both subthreshold and saturation regions.

Shown in Fig. 4 are the model fits showing good agreement with the measured transfer characteristics and common source characteristics. The model reveals the bias dependence of the mobility, which is shown in Fig. 4(c). The mobility in this CVD WSe₂ channel is found to range between 1 and 2.5 cm^2/Vs . The

model indicates a factor of $2\times$ mobility decrease at large normal and longitudinal fields. These analytic mobility values are comparable to electron mobility of $13 \text{ cm}^2/\text{Vs}$ on CVD WSe_2 FET reported by Lin [9] and recently average electron mobility of $11.2 \pm 6.5 \text{ cm}^2/\text{Vs}$ on 5 CVD WSe_2 FETs gated by PEO: CsClO_4 electrolyte by Liang [22]. The square-law-model field-effect mobility, $\mu = (dI_D/dV_{GS})/[C_{ox}(W/L)V_{DS}]$, extracted from the transfer curve of Fig. 3(a) at $V_{DS} = 0.05 \text{ V}$ is $1.5 \text{ cm}^2/\text{Vs}$.

While n-FET characteristics were found in transistor T3 of Figs. 3 and 4, on other transistors on this wafer it proved possible to ion dope the access regions *n* and *p*-type allowing the characterization of both *n* and *p*-FETs as shown in Fig. 5(a) for transistor T2. The single side gate in this transistor geometry is set to -5 V to move ClO_4^- ions to the channel for measurement of the *p*-FET or $+5 \text{ V}$ for the measurement of the *n*-FET. A 10 s hold of the side gate bias set the initial condition for the measurement before the common-source characteristics were initiated. The side gate was kept constant at either $+5$ or -5 V through the measurement. The top gate bias was stepped negatively for the *p*-FET and positively for the *n*-FET. Since the ions are mobile at room temperature, one can expect the channel current to increase when the measurement is repeated because of the strengthening of the EDL with time. Three repeats are shown for each gate bias in Fig. 5(a) with the current increasing on each subsequent trace. The repeats are labeled 1, 2, and 3. The full-channel currents are found to be comparable for the *p* and *n*-FET when biased under the same magnitudes.

In contrast, the transfer characteristics for the *p* and *n*-FETs are shown to have notably different subthreshold characteristics as shown in Figs. 5(b) and (c), respectively. The *p*-FET on/off current ratio biased at $V_{DS} = -0.05 \text{ V}$ is nearly 10^4 , but diminishes to ~ 5 at $V_{DS} = -2.05 \text{ V}$. The subthreshold swing in Fig. 5(b) and on/off current ratio decreases as gate-source voltage is stepped to high negative voltages. This can be understood to result from the intercalation of ClO_4^- ions under the gate. The continuous accumulation of these ions with each sweep reduces the gate efficiency with time as V_{DS} is stepped from -0.05 to -2.05 V , thereby lowering the subthreshold swing and on/off ratio. A similar behavior is observed for the *n*-FET, but with greater degradation of subthreshold swing and on/off ratio, because of the easier intercalation of Cs^+ over ClO_4^- . This effect has previously also been observed by Alessandri [18] for Cs^+ doping of MoS_2 FETs gated with PEO: CsClO_4 .

A transmission electron microscopy (TEM) image of CVD WSe_2 on sapphire is shown in Fig. 5(d). The cross section confirms the formation of an 11 nm Al_2O_3 layer on approximately 5 layers of WSe_2 on sapphire.

VI. ION GATED FET

While the top-gate gate efficiency was degraded due to ion penetration under the gate, the ion gating can be used on the same transistor to obtain the full transfer characteristic. Figure 6(a) shows the measurement protocol that establishes the initial conditions and measurement sequence to obtain the transfer characteristics of the FET at room temperature using the same transistor measured in Fig. 5. The 5 measurement steps are labeled 1 to 5 to indicate the measurement sequence for the *p*-FET. Step 1 is to ramp V_{SG} from 0 to -5 V with $V_{DS} = -0.2 \text{ V}$ in 1 hour to establish hole doping of the access regions. The voltages are then held steady for 40 minutes in step 2 to further strengthen the hole conductivity. Step 3 executes the transfer characteristics measurement with V_{DS} stepped from -0.1 to -1 V and V_{SG} step between -5 and 5 V . The side gate is then returned to zero in step 4 and held constant in step 5 to re-establish the starting condition. The sequence is then repeated 3 times to assure the repeatability of the measurement.

The resultant transfer characteristic, acquired in step 3, is plotted in Fig. 6(b). The TG and SG currents are in the pA range and well below the drain current. Ambipolar behavior is apparent with strong and symmetric $3 \mu\text{A}/\mu\text{m}$ drain currents. The subthreshold swings are 260 and $180 \text{ mV}/\text{decade}$ for the hole branch (left) and tunneling branch (right), respectively for $V_{DS} = -50 \text{ mV}$. Although the ions are mobile at room temperature, using this protocol, repeatable measurements are achievable and no degradation in the characteristics was observed under repeated testing over a month.

The hole and electron field-effect mobilities were extracted from the transfer characteristics and are plotted vs. V_{SG} in Fig. 6(c). The mobilities for electrons and holes with PEO: CsClO_4 controlling the channel surface potential are larger ($12 - 15 \text{ cm}^2/\text{Vs}$) than the mobility obtained using the top gate with Al_2O_3 ($1 - 2.5 \text{ cm}^2/\text{Vs}$) perhaps resulting from the different interface to WSe_2 .

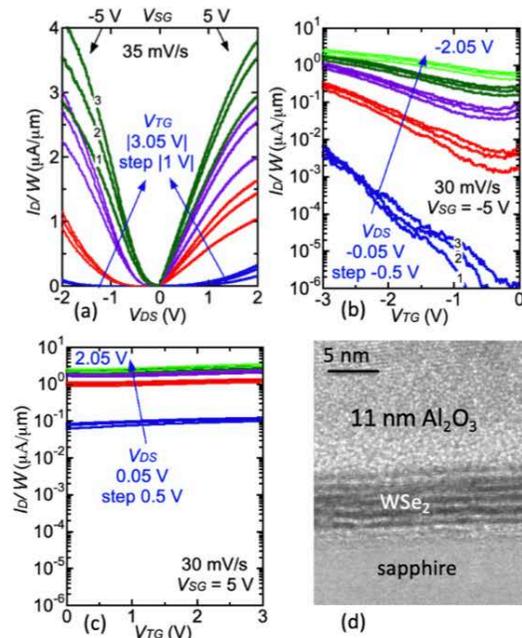


Figure 5: Measured WSe_2 *n*-FET and *p*-FET characteristics for T2 with $W = 8 \mu\text{m}$, $L_{TG} = 4 \mu\text{m}$, $L_A = 2 \mu\text{m}$ using SG, repeated $3\times$ for each plot: (a) *n*-FET and *p*-FET common-source characteristics, (b) *p*-FET and (c) *n*-FET transfer characteristics, and (d) TEM cross section of CVD WSe_2 on sapphire with 11 nm Al_2O_3 TG oxide.

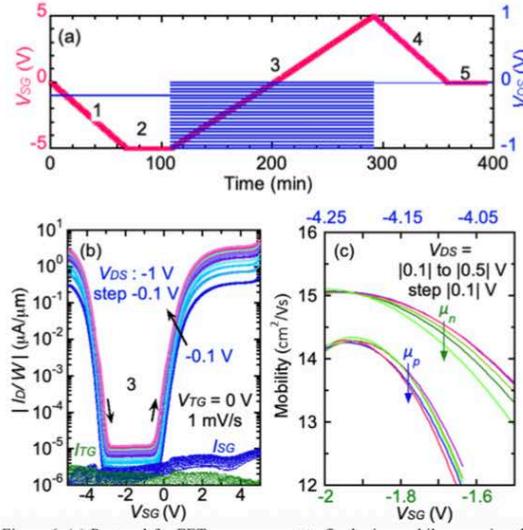


Figure 6: (a) Protocol for FET measurement to fix the ions while sweeping the side gate voltage from -5 to 5 V for transistor T2 at room temperature, (b) ion gating transfer characteristics measurement at stepped drain-source voltages from -0.1 to -1 V, (c) the hole field-effect mobility extracted vs. side gate voltage for small V_{DS} ; the electron mobility was similarly extracted from transfer characteristics taken using an analogous protocol.

The mobilities for these CVD films are considerably lower than reported for exfoliated WSe_2 . Fang [23] reported a hole field-effect mobility of $250 \text{ cm}^2/\text{Vs}$ using an SiO_2 back-gate on Si, and Liu [24] reported electron field-effect mobility of $202 \text{ cm}^2/\text{Vs}$ using an Al_2O_3 back-gate on n+Si, indicating the higher mobility of back-gated exfoliated channels. The lower mobilities measured for CVD WSe_2 material in this work are not inconsistent with prior reports of CVD WSe_2 by Lin [9] and Liang [22].

VII. CONCLUSIONS

We developed a stepper-based top-gated fabrication approach for WSe_2 -on-sapphire FETs allowing characterization of a wide variety of FETs across a $1 \times 1 \text{ cm}^2$ wafer. A quantitative analysis of the transport is obtained by fitting to an analytic transistor model allowing extraction of the field-dependence of the mobility which ranges from 1 to $2.6 \text{ cm}^2/\text{Vs}$.

APPENDIX: 2D FET MODEL

The fundamental relation between the gate voltage, V_{GS} , and the position-dependent quasi-Fermi levels, E_{Fn} , and electron sheet carrier density, n_{2D} , can be written

$$\left(1 + \frac{C_{IT}}{C_{OX}}\right) k_B T \ln \left[\exp \left(\frac{n_{2D}(x)}{N_{2D}} \right) - 1 \right] + \frac{q^2 n_{2D}(x)}{C_{OX}} = q(V_{GS} - V_{TH}) + E_{Fn}(x) - E_{FS} \quad (1)$$

with interface trap capacitance density C_{IT} , TG oxide capacitance density C_{OX} , Fermi level $E_{Fn}(x)$, Fermi level at the

source E_{FS} , threshold voltage V_{TH} , degenerate quantum sheet carrier density $N_{2D} = k_B T g_V g_S (m_c^* m_0 / 2\pi\hbar^2)$, with Boltzmann constant k_B , temperature T , valley g_V and spin g_S degeneracies, electron effective mass m_c^* , electron mass m_0 , and reduced Planck's constant \hbar . Following the derivation of Marin [19], an expression for the drain current, I_D , under the gradual channel approximation is given by

$$I_D = -q\mu_{EFF} \frac{W}{L} V_T \int_{n_{2D,S}}^{n_{2D,D}} n_{2D}(x) \left[\frac{\left(\frac{\gamma}{N_{2D}} + \frac{1}{N_{OX}} \right) \exp \left(\frac{n_{2D}(x)}{N_{2D}} \right) - \frac{1}{N_{OX}}}{\exp \left(\frac{n_{2D}(x)}{N_{2D}} \right) - 1} \right] dn_{2D}(x) \quad (2)$$

where the thermal voltage $V_T = k_B T / q$, electron densities at the drain and source are $n_{2D,D}$ and $n_{2D,S}$, respectively, $\gamma = 1 + C_{IT}/C_{OX}$, and $N_{OX} = C_{OX} V_T / q$. The electron mobility μ_{EFF} is modeled after Iníguez and Moreno [20] and Pei [21] to include semiempirically the dependence on the lateral and normal electric fields, $\mu_{EFF} = \mu / (1 + \mu V_{D,EFF} / v_{SAT} L)$, $L = L_{TG}$, and relations for the effective drain voltage $V_{D,EFF}$ and the saturated velocity v_{SAT} given by

$$V_{D,EFF} = V_{SAT} - V_{SAT} \frac{\ln \left[1 + \exp \left(A_{TS} (1 - V_{DS} / V_{SAT}) \right) \right]}{\ln \left[1 + \exp \left(A_{TS} \right) \right]} \quad (3)$$

$$V_{SAT} = -\frac{L v_{SAT}}{\mu} + \sqrt{\left(\frac{L v_{SAT}}{\mu} \right)^2 + \frac{2 L v_{SAT} Q_S}{\mu C_{OX}}} \quad (4)$$

The dimensionless factor A_{TS} connects the triode and saturation regions. The drain-field mobility is given by $\mu = \mu_0 / (1 + \theta E_{\perp})$, where μ_0 is the effective zero-field mobility, θ is a mobility degradation factor accounting for increased scattering at large gate bias, and E_{\perp} is the vertical electric field, $E_{\perp} = (Q_S + Q_D) / 2\epsilon_{2D}$. Finally, the source Q_S and drain Q_D charges are simply $q n_{2D}$ at the S and D ends, respectively, with perpendicular WSe_2 dielectric constant $\epsilon_{2D} = 6$. With just four fitting parameters, μ_0 , θ^{-1} , v_{SAT} , and A_{TS} , the model is able to effectively describe the experimental results both above and below threshold, in the triode region as well as in saturation. Other physical parameters needed for the computation are summarized below.

TABLE I. Model constants

t_{OX}	11 nm	$C_{OX} = \epsilon_{OX} / t_{OX}$	0.56 $\mu\text{F}/\text{cm}^2$
ϵ_{OX}	7	$C_{IT} = q^2 D_{IT}$	2.88 $\mu\text{F}/\text{cm}^2$
V_{TH}	2.4 V	N_{OX}	9.1E10 cm^{-2}
D_{IT}	1.8E13 $\text{cm}^2 \text{eV}^{-1}$	N_{2D}	2.27E13 cm^{-2}
m_c^*	0.35	$g_V g_S$	6, 2

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