InAs-on-SOI MOSFETS WITH EXTREME LATTICE MISMATCH

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___________________________________
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Abstract

by

Bin Wu

Both molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) have been used to explore the growth of InAs on Si. Despite 11.6% lattice mismatch, planar InAs structures have been observed by scanning electron microscopy (SEM) when nucleating using MBE on patterned submicron Si-on-insulator (SOI) islands. Planar structures of size as large as $500 \times 500 \text{ nm}^2$ and lines of width 200 nm and length a few microns have been observed. MOCVD growth of InAs also generates single grain structures on Si islands when the size is reduced to $100 \times 100 \text{ nm}^2$. By choosing SOI as the growth template, selective growth is enabled by MOCVD.

Post-growth pattern-then-anneal process, in which MOCVD InAs is deposited onto unpatterned SOI followed with patterning and annealing of InAs-on-Si structure, is found to change the relative lattice parameters of encapsulated 17/5 nm InAs/Si island. Observed from transmission electron diffraction (TED) patterns, the lattice mismatch of 17/5 nm InAs/Si island reduces from 11.2 to 4.2% after being annealed at 800 °C for 30 minutes.
High-k Al₂O₃ dielectrics have been deposited by both electron-beam-enabled physical vapor deposition (PVD) and atomic layer deposition (ALD). Films from both techniques show leakage currents on the order of 10⁹ A/cm², at ~1 MV/cm electric field, breakdown field > ~6 MV/cm, and dielectric constant > 6, comparable to those of reported ALD prior arts by Groner.

The first MOSFETs with extreme lattice mismatch InAs-on-SOI channels using PVD Al₂O₃ as the gate dielectric are characterized. Channel recess was used to improve the gate control of the drain current.
I am dedicating this dissertation to my parents, Wu Xizhou and Liang Guohui, who brought me to this universe, nurtured me with their hearts, and gave me the freedom to become me! I love you dearly!

献给我的父母，吴溪洲和梁国惠。他们领我进入这个宇宙，用心养育我自由成长！

我爱你们！

Also, to my dear grandma, Hu Wen, who had loved me all her life without condition for more than ninety years!

也献给我的奶奶，胡纹，回报她给予我的一生无条件的爱护！
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Chapter 1

Introduction

Metal-oxide-semiconductor field effect transistors (MOSFETs) are the building blocks of large-scale integrated circuits (ICs), e.g. microprocessors, semiconductor memories, etc. Following the first demonstration by Kahng and Atalla [1], Si-based MOSFETs have become the most ubiquitous digital electronic devices. As the semiconductor industry approaches the scaling limit of the planar Si-based MOSFET technology, materials innovations are becoming important for performance enhancement. The most appealing reason for investigating III-V devices for logic application is the possibility of obtaining high device operation speed at a low supply voltage $V_{CC}$ (e.g. ~0.5 V) [2].

Most III-V compound semiconductors, e.g. GaAs, InP, In$_x$Ga$_{1-x}$As, InAs, InSb, have significantly higher electron mobility than Si. Among all the binary III-V semiconductor materials, InAs, with a room temperature high electron mobility of 33,000 cm$^2$/Vs at 300 K [3] is particularly attractive as a channel material for field-effect transistors (FETs). This electron mobility is almost three times higher than in GaAs, and more than twenty times higher than in Si. Although high electron mobility at low electric field is attractive, for extremely scaled FETs, the low density of state limits the carrier density, hence the drain current, that can be obtain in an InAs channel [4] [5]. InAs could
still be an intriguing choice as a channel material for high-speed, low-power FETs, and particularly interesting is to have the InAs channel on a Si device platform.

In this chapter, III-V and IV channels are compared. The InAs/Si composite channel MOSFETs are introduced. Processes required for constructing the composite channel MOSFETs are discussed and the fabrication of the InAs/Si composite channel MOSFETs is outlined.

1.1 High electron mobility III-V materials

Table 1.1 lists transport-related properties of selected zinc-blende binary and ternary direct bandgap III-V compound semiconductors. This Table includes the energy bandgap, $E_G$, the energy separation between the conduction band $\Gamma$-valley and the nearest satellite valley, $\Delta E$, the electron density of state effective mass, $m_D$, the low field electron mobility, $\mu$, the peak electron drift velocity, $v_p$, and the electric field corresponding to this peak velocity, $\zeta_p$. Indium arsenide has room temperature low-field electron mobility of 33,000 cm$^2$/V·s [6], which is second to InSb’s 80,000 cm$^2$/V·s [6]. The high electron mobility of InAs results from its small $\Gamma$-valley electron effective mass, $0.023m_0$ ($m_0$ is the electron rest mass).
Table 1.1

Transport-related properties of selected zinc-blende binary and ternary direct bandgap III-V compound semiconductors

<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>$E_G^a$ (eV)</th>
<th>$\Delta E^a$ (eV)</th>
<th>$m_p^a$ ($m_0$)</th>
<th>$\mu_p^a$ (cm$^2$/V·s)</th>
<th>$v_p$ ($10^2$ cm/s)</th>
<th>$\xi_p$ (kV/cm)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al$<em>{0.175}$Ga$</em>{0.825}$As</td>
<td>1.643</td>
<td>0.178</td>
<td>0.081</td>
<td>4956</td>
<td></td>
<td></td>
<td>[7]$^{cal}$</td>
</tr>
<tr>
<td>Al$<em>{0.325}$Ga$</em>{0.675}$As</td>
<td>1.830</td>
<td>0.0874</td>
<td>0.094</td>
<td>2406</td>
<td>0.5</td>
<td>5</td>
<td>[7]$^{cal}$</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.425</td>
<td>0.284</td>
<td>0.067</td>
<td>8500</td>
<td>2.1</td>
<td>2.8</td>
<td>[7]$^{cal}$</td>
</tr>
<tr>
<td>GaN</td>
<td>3.279</td>
<td>1.4</td>
<td>0.15</td>
<td>450</td>
<td></td>
<td></td>
<td>[8]$^{exp}$</td>
</tr>
<tr>
<td>InP</td>
<td>1.35</td>
<td>0.54</td>
<td>0.078</td>
<td>4600</td>
<td>2.6</td>
<td>10</td>
<td>[9]$^{cal}$</td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>0.75</td>
<td>0.58</td>
<td>0.0463</td>
<td>11000</td>
<td>3.1</td>
<td>2.2</td>
<td>[10]$^{cal}$</td>
</tr>
<tr>
<td>InAs</td>
<td>0.354</td>
<td>0.79</td>
<td>0.023</td>
<td>33000</td>
<td>4.3</td>
<td>2.3</td>
<td>[11]$^{exp}$</td>
</tr>
<tr>
<td>InSb</td>
<td>0.17</td>
<td>0.51</td>
<td>0.0136</td>
<td>80000</td>
<td>5.7</td>
<td>0.51</td>
<td>[12]</td>
</tr>
</tbody>
</table>

$^a$ From Brennan and Brown [3] except those of InSb which is from Sze [16]
$^{cal}$ indicates a calculated result
$^{exp}$ indicates a measured result
all values are for 300 K unless otherwise indicated.

Transistors with III-V channels show higher electron mobility and conductivity than those with Si. In Figure 1.1 and 1.2, Chau et al. compares electron mobility and channel conductivity measured in various III-V quantum well structures to those of Si MOSFETs as a function of electron density [2]. III-V channels have lower electron density, but their high mobilities compensate for it and result in higher conductivity than Si. In Figure 1.2 the InAs/AlSb system shows the highest conductivity, followed by InGaAs/InAlAs and InSb/AlInSb.
Figure 1.1 Electron mobility $\mu$ versus sheet electron density $n_s$ in n-channel FETs [2].

Figure 1.2 Electron conductivity $\sigma \mu n_s$ versus sheet electron density $n_s$ in n-channel FETs [2].
The velocity-field characteristics quantify the relationship between drift velocity and electric field. Figure 1.3 summarizes low-field measurements of carry velocity in semiconductors of interest: velocity-field characteristics of InAs [13], InSb [17], GaAs [17], InP [11], Si [18], and Ge [19]. At low electric fields the velocity-field curve is linear with a slope given by $\mu = v/\xi$. Electrons with higher mobility reach higher velocities at lower electric fields. The electron peak velocity of $4.3 \times 10^7$ cm/s at 77 K [13] in InAs is more than twice that of GaAs and about twenty times the electron velocity of Si at the same bias. Moreover, this peak velocity in InAs appears at an electric field of 2.3 kV/cm, which is amongst the lowest of any semiconductor. InSb has high electron peak velocity, $\sim 4.2 \times 10^7$ cm/s, at an even lower electric field, 0.5 kV/cm. It can also be an interesting candidate as a MOSFET channel.

![Figure 1.3 Measured electron drift velocity versus electric field in bulk semiconductors. Unless marked the measurements were made at room temperature (plotted by Peter van Loon, Notre Dame).](image-url)
The data of InAs [13] and InSb [17] shown in the velocity-field plot, Figure 1.3, are for 77 K, when intrinsic carrier concentration is low, using ultra fast laser pulses. From the slopes of the velocity-field curves of InAs and InSb, low-field mobilities of approximately, 30,000 and 100,000 cm²/V·s, respectively, are obtained, consistent with the low-field room temperature Hall-effect of Table 1.1. The higher mobility, velocity, and conductivity of III-Vs motivate interest in these materials to replace Si as the MOSFET channel material.

1.2 Density-of-states in III-V n-MOSFETs

Fischetti and Laux showed that “low energy concepts, such as low-field mobility and effective mass, fail to describe charge transport” in devices with gate length smaller than 250 nm [20]. Using a self-consistent two-dimensional Monte Carlo program, they found that when MOSFETs are scaled to less than 250 nm the speed of Si, Ge and GaAs FETs becomes largely independent of the semiconductor, but with InP and In₀.₅₃Ga₀.₄₇As channels the speed is improved. Figure 1.4 shows their simulation results from [20], illustrating maximum transconductance, $g_m$, as a function of metallurgical⁠¹ channel length at 77 and 300 K for $n$-channel Ge, Si, GaAs, InP, In₀.₅₃Ga₀.₄₇As, and Si MOSFETs. The $g_m$ is taken at drain biases, $V_{DS}$, of 2.5, 1.0 and 0.7 V and for gate lengths of 250, 100 and 70 nm, respectively, and maximum is selected between three overdrives, $V_{GS}$-$V_{TH}$: 0.5, 0.7 and 1.7 V.

¹ The metallurgical channel length in Figure 1.4 refers to the distance between two junctions, where the dopant concentration profile of source and drain meets that of channel acceptor.
Figure 1.4 Large-signal transconductance as a function of metallurgical channel length at (a) 77 K and (b) 300 K for MOSFETs with different channel materials simulated at the bias conditions discussed in the text from Fischetti and Laux [20].

In 2005, Rahman et al. [5], using a 20-band tight-binding model to determine the band structure and a ballistic transport model for the MOSFET, showed that the low electron density resulting from the low density-of-states (DOS) in III-V channels limits the on-current at a given gate drive for 9-nm gate length III-V n-MOSFETs (body thickness 19 atomic layers, effective oxide thickness is ≤ 1 nm). Figure 1.5 [5] shows the simulated drain currents, $I_D$, of $p$- and n-MOSFETs with Si, Ge, GaAs and InAs channels. While GaAs and InAs have higher electron mobilities, Table 1.1, higher velocities, Fig. 1.3, and higher conductivities, Fig. 1.2, than Si, these low-field properties do not compare favorably vs. Si MOSFET simulations especially when the overdrive is kept constant between materials. A primary reason is that the III-V channels have low conduction band DOS relative to Si.
Figure 1.5 Simulated ballistic drain current Vs. drain bias for Si, Ge, GaAs and InAs p- and n-MOSFETs with effective oxide thickness of 0.5 nm and fixed overdrive from Rahman et al. [5].

From Rahman, the simulated carrier density vs. gate bias is shown in Figure 1.6 [5]. The low DOS effective-mass and single gamma conduction band in the III-V materials significantly limits the channel density that can be achieved at a given gate bias relative to Ge and Si.

Figure 1.6 Simulated carrier density as a function of gate bias for Si, Ge, GaAs and InAs p- and n- MOSFETs from Rahman et al. [5].
The relationship between transconductance, effective mobility, and DOS effective mass is encapsulated in the following relation by Thompson et al. [21],

\[
g_m = \frac{dI_{sat}}{dV_g} \propto \frac{d(n\mu)}{dV_g} \propto \mu \frac{d(n)}{dV_g} \propto \mu \frac{d(m_D E_F)}{dV_g} \propto \mu m_D \frac{d(V_g)}{dV_g} = \mu m_D
\]

(1.1)

where \(I_{sat}\) is the saturation drain current, \(V_g\), gate bias, \(n\), the electron density in the channel, \(\mu\) is the channel mobility, \(m_D\), the DOS effective mass, and \(E_F\), the Fermi energy.

Using the mobility and DOS effective-mass product as a figure of merit and normalizing this product to unstrained Si, Thompson et al. [21] compared alternate channel materials, Table 1.2, concluding that III-V channels do not compare favorably to strained Si. However, Table 1.2 does show that InAs and InSb offer improvements. What is needed is a way to increase the DOS effective mass of a III-V channel while still maintaining a high channel mobility relative to Si.

<table>
<thead>
<tr>
<th>Channel Material</th>
<th>(E_g) (eV)</th>
<th>(\mu_n) (cm²/V·s)</th>
<th>nDOS (cm⁻²·eV⁻¹)</th>
<th>Normalized (g_m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>1450</td>
<td>(1.59 \times 10^{14})</td>
<td>1</td>
</tr>
<tr>
<td>Ge</td>
<td>0.67</td>
<td>3900</td>
<td>(5.67 \times 10^{13})</td>
<td>.92</td>
</tr>
<tr>
<td>InSb</td>
<td>0.17</td>
<td>(7.7 \times 10^4)</td>
<td>(5.87 \times 10^{12})</td>
<td>1.9</td>
</tr>
<tr>
<td>InAs</td>
<td>0.35</td>
<td>(2.3 \times 10^4)</td>
<td>(1.01 \times 10^{13})</td>
<td>1.29</td>
</tr>
<tr>
<td>GaSb</td>
<td>0.73</td>
<td>3750</td>
<td>(1.66 \times 10^{13})</td>
<td>0.28</td>
</tr>
<tr>
<td>InP</td>
<td>1.34</td>
<td>5370</td>
<td>(3.31 \times 10^{13})</td>
<td>0.77</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.42</td>
<td>9200</td>
<td>(2.6 \times 10^{13})</td>
<td>1.03</td>
</tr>
<tr>
<td>Strained Si</td>
<td>1.08</td>
<td>2900</td>
<td>(1.59 \times 10^{14})</td>
<td>2.0</td>
</tr>
</tbody>
</table>

Note: mobilities are for low field/bulk.
1.3 Engineering density-of-state effective mass

It is possible to engineer the DOS effective mass of a channel by creating a composite-channel, i.e. a channel composed of two channel materials. If the channel material thickness is commensurate with the electron wavefunction, then the electron is not in one material or another but is extended over both materials. The band structure of such an ultrathin channel then takes on a character which has a bandgap and energy dispersion between the two bulk band structures. Prada et al. [22] examined, using a tight-binding model simulator NEMO-3D, how the band structure of an InAs/Si composite channel is related to the relative thicknesses of InAs and Si layers. The bands shift is calculated with respect to the valence band of Si [22] [23]. The Si tight-binding parameters are calibrated in NEMO-3D to match the band offsets [22]. Further bending, observed in accordance to [23], is obtained numerically. The local band structure numerical results for the unit cell are represented in the inset in Figure 1.7 [22], 2/6 nm InAs/Si.

![Figure 1.7 Schematic representation of band shifts in a Si/InAs heterostructure: NEMO-3D numerical results of local band structure. Inset: unit cell of the structure. Lattice mismatch in the heterostructure causes changes in band alignment from Prada et al. [22].](image-url)
The InAs/Si heterostructure consists of a polar compound semiconductor, InAs, on a nonpolar elemental one, Si [24]. In the growth of polar-on-nonpolar materials like III-Vs on Si, the interface is a key concern. Compared to the elementary substrate which has two identical atoms in the primitive cell, a binary compound has two different atoms. When a binary compound is being grown on an elementary substrate [25], there exists two different atom nucleation sequences. Crystallographic orientation of the elementary substrate becomes critical for a defect-free growth of the epitaxial polar compound layer because it is important that the interface charge density be zero to minimize Coulomb scattering [25].

As pointed out by Kroemer [26] antiphase domains form at the growth interfaces which introduce interface charge that is detrimental to device performance. With Wright and Polasko [24], he showed that it is possible on a higher index, charge neutral surface to circumvent both antiphase domains and interface charge. Low-index polar interfaces, such as (100) or (111) interfaces, have charged planes carrying opposite charges next to each other. This arrangement of oppositely charged plane generates electric fields of the order 40 M V/cm [25]. The large electric field causes the disordering of the atoms near the interface during epitaxial growth [25]. Low-index (110) and high-index (211) planes are preferred orientations for polar-on-nonpolar growth for their electrical neutrality at the interface [25]. According to Kroemer et al. growth on (211) surfaces is preferable to (110), because when growing polar-on-non-polar structures, growth along the (110) direction requires the control of atomic disorder on the polar semiconductor [24], while growth along (211) does not [25]. Prada reports three crystallographic orientations including the (211) orientation which is charge neutral. Her findings are summarized in
Figure 1.8 [22]. For a fixed channel thickness of 8 nm, composed of z nm of InAs and 8-z nm of Si, Prada computed the energy bandgaps as a function of the thickness of the InAs grown on (100), (110), and (211) orientations, Figure 1.8. A sharp transition from a Si bandgap to an InAs bandgap occurs as the proportion of InAs layers increases from 1.5 to approximately 3 nm out of a total of 8 nm channel thickness.

![Energy bandgap and DOS effective mass for electrons in (100)-, (110)- and (211)-oriented heterostructures as a function of InAs thickness, x. Open symbols correspond to the indirect bandgap situations after Prada et al. [22].](image)

Simulation results of the 8-nm InAs/Si composite material shows that both DOS effective mass and bandgap decrease with the InAs thickness. All the values of bandgap and effective mass converge to the pure InAs QW when InAs thickness becomes 8 nm. So, it is possible that an engineered composite-channel heterostructure can optimize the electron mass and bandgap for FET applications, optimum $m_D$ and $E_G$. 

12
It appears possible then, to construct an ultrathin channel (< 10 nm) that takes on properties which are intermediate between high mobility material, e.g. InAs, and high DOS mass, high charge density Si [22]. Figure 1.9 (a) proposes an InAs/Si composite channel design on SOI and shows in (b) the unstrained straddling junction band lineup, from the band-offset calculations of van de Walle [27]. It is the goal of this research to experimentally explore the growth of InAs/Si composite channels to raise both the DOS effective mass relative to InAs and the electron velocity relative to Si and lead to higher MOSFET channel currents.

Figure 1.9 (a) Schematic drawing of an InAs/Si composite channel MOSFETs and (b) flat-band diagram for Si/InAs. The band lineup predictions are obtained from Van de Walle [27].

1.4 Mismatched epitaxial growth

This dissertation explores the fabrication of MOSFETs formed with InAs on SOI channels deposited by molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD). Growth of InAs on Si faces two challenges: (1), the extreme lattice mismatch, 11.6%, and (2) the transition from nonpolar to a polar crystal structures, i.e. from Si to InAs. In Chapter 2, growth of InAs on Si is explored, using both MBE and MOCVD, towards the construction of the first InAs/Si composite-channel MOSFET.
To form an InAs/Si composite channel, a thin InAs film must be epitaxially grown on a Si template. The most apparent difficulty of growing InAs on Si is the difference in lattice constant. Lattice constants and critical layer thicknesses of III-V materials on bulk Si and Ge, (100), computed from Matthews and Blakeslee [28], are shown in Table 1.3. Note that the critical layer thickness for Ge on Si is just 12 Å and for III-V materials on both Si and Ge it is less than a monolayer. These thicknesses were computed by Tom Kosel, Notre Dame.

Table 1.3

Matthews-Blakeslee critical layer thickness, $h_c$, and crystal misfit, $f$, for selected materials grown on bulk (100) Si and Ge substrates

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Lattice</td>
<td>% Mismatch</td>
<td>Critical layer</td>
<td>% Mismatch</td>
<td>Critical layer</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Constant</td>
<td>on Si</td>
<td>hickness on S</td>
<td>on Ge</td>
<td>hickness on Ge</td>
</tr>
<tr>
<td>3</td>
<td>Crystal</td>
<td>a (Å)</td>
<td>$f$ (Si)</td>
<td>$h_c$ (Si) (Å)</td>
<td>$f$ (Ge)</td>
<td>$h_c$ (Ge) (Å)</td>
</tr>
<tr>
<td>4</td>
<td>Si</td>
<td>5.4309</td>
<td></td>
<td>0</td>
<td>4.48</td>
<td>11.95</td>
</tr>
<tr>
<td>5</td>
<td>Ge</td>
<td>5.6577</td>
<td>4.18</td>
<td>11.27</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>6</td>
<td>GaSb</td>
<td>6.0959</td>
<td>12.24</td>
<td>0</td>
<td>7.75</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>InAs</td>
<td>6.0583</td>
<td>11.55</td>
<td>0</td>
<td>7.08</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>InSb</td>
<td>6.479</td>
<td>19.3</td>
<td>0</td>
<td>14.52</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: courtesy Thomas Kosel.

1.4.1 Growth of InAs on patterned SOI

Growth on a patterned substrate, either by forming mesas as a growth template [29] [30] or by opening windows through a growth mask [31] [32], has been previously proposed to effectively reduce the threading dislocation density in an epitaxial layer and increase the critical layer limit. The reduction of dislocation density results from the moving of threading dislocations to the mesa edges during growth [33]. It was shown by
Fitzgerald et al. [33] that growth of \( \text{In}_{0.05}\text{Ga}_{0.95}\text{As} \) on (100) GaAs island with diameters in the range 10 – 400 µm allowed a 100 to 10 times reduction in density of interface dislocation, respectively, from that on diameters larger than 1 cm. The lattice mismatch of \( \text{In}_{0.05}\text{Ga}_{0.95}\text{As} \) grown on GaAs is approximately 0.4%. Zubia and Hersee [30] show, theoretically, that with islands size of ~10 – 100 nm, dislocations can be eliminated from heterojunctions that are mismatched by as much as 4.2% (Ge on Si). In this thesis research, patterned heteroepitaxial growth has been explored to achieve an ultrathin film, < 10 nm of InAs on Si.

InAs is nucleated directly onto bulk (100) Si substrates and (100) SOI. Both patterned and unpatterned growths have been explored. Growth on patterned SOI starts with the formation of islands of Si from an SOI substrate. InAs is then deposited onto the substrate using MBE or MOCVD. Figure 1.10 shows a process cross section. These Si islands, Figure 1.10 (a), are submicron in at least one planar dimension, which is intended to reduce the formation of threading dislocations [30] [34] [35] arising from the extreme lattice mismatch of InAs on Si, by providing a nearby edge to terminate the misfit dislocations. In patterned growth of InAs on SOI islands the growth can be selective or nonselective. The two cases are represented in Figure 1.10 (b) and (c), respectively.
Figure 1.10 Cross-section schematic drawings of the pattern-then-growth process for InAs-on-SOI with extreme lattice mismatch. The process starts with (a) submicron Si island formation on SOI, followed with InAs growth: (b) selective or (c) nonselective.

1.4.2 Post-growth pattern-then-anneal process

Post-growth patterning combined with annealing has been shown to improve the crystalline quality of epitaxial films deposited on lattice mismatched substrates [36][37][38]. Post-growth patterning followed by a thermal treatment at 850 °C for 15 minutes eliminates antiphase domain dark loops in 15 × 15 µm², 2 – 3 µm thick GaAs, deposited on Si substrate, which is 4° off (100) towards <011> [36]. Zhang et al. [37] reported complete removal of threading dislocations from 70 × 70 µm², 200 – 600 nm thick ZnSe, grown on (100) GaAs using MOCVD, following post-growth patterning annealing at 600 °C for 30 minutes.

In Chapter 2, the post-growth pattern-then-anneal approach is applied to InAs-on-SOI system, showing in cross section in Figure 1.11(a) – (c). InAs is first deposited onto unpatterned thinned SOI, Figure 1.11(a), then the InAs/Si layers are patterned into...
submicron islands, Figure 1.11(b). To prepare for the annealing, InAs/Si islands are encapsulated in PECVD SiO$_2$, Figure 1.11 (c).

![Cross-section schematic drawings of the post pattern-then-anneal process of InAs-on-SOI structures with extreme lattice mismatch. The process starts with (a) growth of InAs on thinned SOI substrate and followed with (b) post growth patterning and (c) annealing of encapsulated InAs/Si structures.](image)

Both methods, deposition on patterned substrate templates [29] [30] [31] [32] and post-growth pattern-then-annealed structures [36] [37], are shown capable of realizing less defective epitaxial layers on lattice-mismatched substrates. Chapter 2 presents the InAs growth findings on Si by MBE and MOCVD using the patterning methods.

1.5 High-$k$ gate dielectrics

Aggressive scaling of transistors requires that the SiO$_2$ layer be reduced to under 2 nm where electron leakage current can exceed 1 A/cm$^2$ [39] [40] caused by electrons tunneling directly from channel to gate. The reason to replace SiO$_2$ in a Si-based MOSFET with a gate insulator of higher dielectric constant is to maintain a high channel
current density while keeping the gate leakage current low. Direct tunneling current through the gate insulator decreases exponentially with increasing tunneling distance from the gate electrode to the channel, which corresponds to the thickness of the insulator.

The technologically-relevant high-\(k\) dielectrics, loosely defined as oxides having dielectric constants greater than \(\text{SiO}_2\), are typically not native oxides of the underlying semiconductors. Table 1.4 compares properties of some high-\(k\) dielectrics [40] [41].

Table 1.4

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>(k^a)</th>
<th>(E_G^b) (eV)</th>
<th>(E_A^b) (eV)</th>
<th>(\Delta E_{C,\text{Si}}^b) (eV)</th>
<th>(\Delta E_{V,\text{Si}}^b) (eV)</th>
<th>(\Delta E_{C,\text{InAs}}^b) (eV)</th>
<th>(\Delta E_{V,\text{InAs}}^b) (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\text{HfO}_2)</td>
<td>25</td>
<td>6</td>
<td>2.4</td>
<td>1.48</td>
<td>3.4</td>
<td>2.48</td>
<td>3.16</td>
</tr>
<tr>
<td>(\text{ZrO}_2)</td>
<td>25</td>
<td>5.8</td>
<td>2.5</td>
<td>1.4</td>
<td>3.28</td>
<td>2.44</td>
<td>3</td>
</tr>
<tr>
<td>(\text{HfSiO}_4)</td>
<td>11</td>
<td>6.5</td>
<td>2</td>
<td>2.03</td>
<td>3.35</td>
<td>3</td>
<td>3.14</td>
</tr>
<tr>
<td>(\text{La}_2\text{O}_3)</td>
<td>30</td>
<td>6</td>
<td>2</td>
<td>2.36</td>
<td>2.52</td>
<td>3.35</td>
<td>2.29</td>
</tr>
<tr>
<td>(\text{LaAlO}_3)</td>
<td>30</td>
<td>5.6</td>
<td>2.5</td>
<td>1.53</td>
<td>2.95</td>
<td>2.52</td>
<td>2.72</td>
</tr>
<tr>
<td>(\text{SrTiO}_3)</td>
<td>2000</td>
<td>3.3</td>
<td>3.9</td>
<td>0.11</td>
<td>2.07</td>
<td>1.19</td>
<td>1.75</td>
</tr>
<tr>
<td>(\text{Ta}_2\text{O}_5)</td>
<td>22</td>
<td>4.4</td>
<td>3.3</td>
<td>0.4</td>
<td>2.88</td>
<td>1.46</td>
<td>2.58</td>
</tr>
<tr>
<td>(\text{Al}_2\text{O}_3)</td>
<td>9</td>
<td>8.8</td>
<td>1</td>
<td>2.6</td>
<td>5.08</td>
<td>3.6</td>
<td>4.84</td>
</tr>
<tr>
<td>(\text{SiO}_2)</td>
<td>3.9</td>
<td>9</td>
<td>0.9</td>
<td>3.2</td>
<td>4.68</td>
<td>4.1</td>
<td>4.54</td>
</tr>
<tr>
<td>(\text{Si}_3\text{N}_4)</td>
<td>7</td>
<td>5.3</td>
<td>2.1</td>
<td>1.7</td>
<td>2.48</td>
<td>2.7</td>
<td>2.24</td>
</tr>
</tbody>
</table>

\(^a\) Static dielectric constants are from Robertson [40]

\(^b\) Bandgap, electron affinity and conduction band offsets are collected from Robertson and Falabretti [41]

When choosing gate dielectric, higher dielectric constant is not the only concern. Band offsets, thermodynamic stability, kinetic stability, interface quality with the underlying channel material, density of electrically-active defects all need to be
considered [40]. The above aspects have been analyzed by Robertson [40] and Wong and Iwai [39]. For more rigorous and conclusive discussion on high-\(k\) dielectrics, references [39], [40], [41], [42], and [43] are a resource. Here a few of the selection factors are outlined.

The gate dielectric must be an insulator. To be a good insulator, both conduction and valence band offsets, between the semiconductor and gate dielectric, need to be higher than 1 eV to limit conduction by thermionic emission of electrons or holes into the oxide bands. Figure 1.12 illustrates the conduction and valence band offsets, from Table 1.4, of selected dielectrics to InAs.

![Figure 1.12 Calculated conduction band and valence band offsets of dielectrics to InAs](image)

All the materials listed in Table 1.4 have suitable band alignment to InAs. Among all the dielectrics, \(\text{Al}_2\text{O}_3\) has the second highest band offset in the conduction band to InAs, and highest in the valence band. These are due to its second highest band gap, 8.8 eV, which is only 0.2 eV less than that of \(\text{SiO}_2\), 9 eV. The dielectric constant of \(\text{Al}_2\text{O}_3\) is
not of the most desirable, only $9 - 10$ [39], but it still doubles the tunneling distance while maintaining the same drain current drive vs. SiO$_2$. Lin [44] and Wu [45] show ALD Al$_2$O$_3$ films, 12 – 60 Å, on GaAs have leakage current as low as $10^9 - 10^7$ A/cm$^2$ at 1 MV/cm electric field and breakdown fields as high as 30 MV/cm, at room temperature. The interface trap density between Al$_2$O$_3$ and some III-V compound semiconductors is reported to be $\sim 10^{12}$cm$^{-2}$eV$^{-1}$ on InSb [46], $\sim 10^{12}$cm$^{-2}$eV$^{-1}$ on InGaAs [47] and as low as $2.9 \times 10^{11}$cm$^{-2}$eV$^{-1}$[48] on InGaAs.

Demonstrations of III-V MOSFETs with Al$_2$O$_3$ as the gate dielectric have been reported. Ye [49] showed 1-µm-gate-length In$_{0.8}$Ga$_{0.2}$As/GaAs MOSFET with 16-nm-thick ALD Al$_2$O$_3$ gate dielectric with gate leakage current less than $10^{-4}$ A/cm$^2$, in the range of $V_D = 0 - 3$ and $V_{GS} = -4 - 3$ V, and maximum transconductance higher than 100 mS/mm at $V_D = 3$ and $V_{GS} = 0.5$ V, and low field channel electron mobility higher as high as 660 cm$^2$/Vs. Recently, Li [50] showed In$_{0.8}$Ga$_{0.2}$As channel MOSFETs with 21 nm Al$_2$O$_3$ deposited using molecular-atom-deposition, showing transconductance of $\sim 40$ mS/mm, $V_D = 4$ and $V_{GS} = -0.7$ V, measured from a device with 2 µm gate and low field channel electron mobility of 900 cm$^2$/Vs. Pure InAs-channel MOSFETs formed with ALD 30-nm Al$_2$O$_3$ gate dielectric, were reported by Li [51] and a transconductance of $\sim 2$ mS/mm at $V_D = 0.2$ and $V_{GS} = -4.8$ V is demonstrated for device with 5-µm length gate. The device results reported by Ye [49] show Al$_2$O$_3$-III/V MOS systems are suitable for building III-V MOSFETs.

Aluminum oxide has a dielectric constant of $\sim 9$, barrier height to InAs of 3.6 eV [40], and room temperature leakage current and breakdown voltage of $10^9 - 10^7$ A/cm$^2$ and 30 MV/cm, respectively. An interface trap density as low as $2.9 \times 10^{11}$cm$^{-2}$eV$^{-1}$[48]

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between Al₂O₃ and InGaAs has been demonstrated. Aluminum oxide adheres well to many different surfaces and is thermodynamically and chemically stable [40] [52]. These properties make Al₂O₃ suitable as the gate dielectric for the InAs-channel MOSFET. This research uses Al₂O₃ as the gate dielectric for InAs/Si channel MOSFETs. Chapter 3 shows two different approaches, PVD and ALD for realizing Al₂O₃ gate dielectrics. The Al₂O₃ film qualities are tested physically and electronically through the formation of MOS diodes.

1.6 InAs-on-SOI MOSFETs approach

The fabrication of InAs-on-SOI MOSFETs with extreme lattice mismatch and Al₂O₃ as gate dielectric is explored in this work on (100) SOI. While (211) and (110) surfaces are needed, at this time SOI material with these orientations had not been available. The fabrication steps are outlined below and illustrated by scaled drawings of the device cross-section in Figure 1.13(a) – (f):

1. Thin down SOI 50 nm Si layer to 10 nm, Figure 1.13 (a) and (b)
2. Form submicron Si islands, Figure 1.13(c)
3. Deposit InAs film on Si islands using MBE or MOCVD, Figure 1.13(d)
4. Deposit Ti/Au source and drain contacts, Figure 1.13(e)
5. Deposit Al₂O₃/Ti/Pt/Au gate stack, Figure 1.13(f)

The detailed fabrication process is attached at the end of this thesis as Appendix A.
Figure 1.13 Scaled cross-section drawings of the forming of an InAs/Si composite channel MOSFET: (a) SOI substrate with 50 nm of Si, (b) Si layer thinned to 10 nm, (c) submicron Si template is formed, (d) InAs deposited on Si, (e) source and drain contacts are deposited, and with final step (f) gate stack with Al₂O₃ as the dielectric deposited.
1.7 Dissertation overview

This dissertation explores the fabrication and characterization of MOSFETs with InAs/Si as the channel material and Al₂O₃ as the gate dielectric. Chapter 2 reports the growth of InAs on Si using both MBE and MOCVD. Planar morphology of InAs has been achieved using both techniques by depositing InAs onto patterned SOI substrate. The selective growth of InAs onto Si islands is demonstrated using MOCVD. The post-growth pattern-then-anneal process is also shown. Changes, compared to unannealed structures, upon annealing are observed and analyzed.

Chapter 3 shows two different approaches, PVD and ALD, for realizing Al₂O₃ as the gate dielectric material. Physical and electrical properties of Al₂O₃ films are characterized and compared with prior arts. Chapter 4 characterizes MOSFETs with InAs/Si as the channel and PVD Al₂O₃ as the gate dielectric. The fabrication and DC characterization of the device are reported and discussed. Chapter 5 summarizes the achievements and outlooks to the future.
Chapter 2

Epitaxial Growth of InAs-on-SOI with Extreme Lattice Mismatch

Growth of InAs on Si have been explored using both MBE and MOCVD towards the construction of InAs/Si composite-channel MOSFETs. This chapter details the processes that lead to the formation of InAs-on-SOI with extreme lattice mismatch. The most promising results, with planar InAs structures, are observed when InAs has been grown on submicron Si islands formed on thinned SOI substrate, using both MBE and MOCVD growth methods. The post-growth pattern-then-anneal process of InAs-on-SOI is explored and characterized by transmission electron microscopy (TEM) and transmission electron diffraction (TED).

2.1 Submicron Si island formation

2.1.1 SOI thinning and characterization

A process for thinning SOI from 200 to 1.5 nm has been outlined by Tabe et al. [53], consisting of thermal oxidation followed by SiO₂ removal using an HF/H₂O mixture to thin SOI to approximately 4 nm. Further thickness reduction proceeds by alternating oxidation in H₂SO₄/H₂O₂ and wet-chemical etch steps to the desired thickness at a rate of 0.5 nm/cycle.

In this thesis research, an oxidize-then-etch process is used to thin down the SOI Si layer from 50 to ~10 nm. The SIMOX (separation by implantation of oxygen)-SOI
starting substrate was 100 mm in diameter, obtained from Ibis Technology. The process starts from a p-type (100) SOI substrate with 50 nm Si top layer and a 1400 nm buried SIMOX layer (BOX). The top Si layer is first dry oxidized at 950 °C for 90 minutes. Following the oxidation, the substrate is etched in 1:10 buffered-oxide etchant (BOE) to remove the SiO₂ layer, thinning the Si layer down to ~10 nm. Then, the substrate goes through one RCA² cycle to achieve a Si layer thickness of 7 ± 2 nm.

The measurement of SOI thickness is done using a variable-angle spectroscopic ellipsometer (VASE), J. A. Woollam Co., Inc. and ellipsometric analysis software, WVASE32, using a three-layer Si/SiO₂/Si structure modeled with Cauchy approximation. Table 2.1 shows the results of the VASE measurements at the last step of the thinning process. Table 2.1 shows that Si island thicknesses less than 10 nm are achieved and also shows the BOX thickness to be ~140 nm. Uniformity of the film thickness is checked by measuring in five locations across the 100 nm diameter of the substrate and about 2 cm apart from each other.

² One RCA cycle includes: RCA1 (DI: NH₄OH: H₂O₂=40-50:1:1) bath, 70 °C, 10 minutes, DI rinse; RCA2 (HCl: H₂O₂:DI=40-50:1:1) bath, 70 °C, 10 minutes, DI rinse; 1HF: 50DI dip, 30 s.
Table 2.1

Measurements taken using VASE from a 100 mm diameter SOI with thinned Si layer

<table>
<thead>
<tr>
<th>position</th>
<th>center</th>
<th>2 cm from center</th>
<th>2 cm from center</th>
<th>4 cm from center</th>
<th>4 cm from center</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si thickness (Å)</td>
<td>67 ± 6</td>
<td>58 ± 18</td>
<td>82 ± 4</td>
<td>57 ± 9</td>
<td>64 ± 5</td>
</tr>
<tr>
<td>BOX thickness (Å)</td>
<td>1428 ± 11</td>
<td>1407 ± 16</td>
<td>1428 ± 4</td>
<td>1417 ± 13</td>
<td>1447 ± 9</td>
</tr>
</tbody>
</table>

Figure 2.1 traces the thickness of the SOI through the thinning procedure. The spreading of data reduces from ±4 nm at the 52 nm starting step to ±2 nm at the 7 nm final step, suggesting that the thinning procedure improve the uniformity.

Figure 2.1 Variable-angle spectroscopic ellipsometer measurements of the thinning SOI thickness across a 100 mm diameter substrate before and after 2 layer removal steps.

Figure 2.2 confirms, using TEM, the thickness of the thinned Si layer is 5 ± 1 nm. The TEM image is taken by Tung-Sheng Kuan, State University of New York at Albany. The structure shown in Figure 2.2 is the cross-section of the thinned Si SOI followed by MOCVD InAs growth and PECVD SiO₂ deposition, discussed in Section 2.3.
Figure 2.2 Transmission electron microscopy (TEM) image, taken by Tung-Sheng Kuan, State University of New York at Albany, showing the Si layer can be thinned down to be 5 ± 1 nm.

The thinned SOI in Figure 2.2 was used as the substrate for the MOCVD InAs growths. When the MBE growths were explored, at an earlier time, thin, 50 nm SOI was not available. The starting wafers for MBE growth were 100-mm-diameter (100) SIMOX SOI from Ibis Technology Corp, but with Si layer thickness of 7 ± 0.04 µm. To thin down this thick layer more aggressive methods were employed. The top Si layer was thinned to approximately 500 nm from the initial thickness in a Logitech CDP (chemical delayering and planarization) system using an experimental slurry from Cabot Microelectronics, EXP-0012. Thermal oxidation followed by oxide removal in BOE was then used to remove the SiO₂ to obtain a Si thickness of few hundred nanometers. Figure 2.3 is the cross-section of the SOI wafer, showing the top Si layer thickness of ~144 nm and BOX of ~273 nm and a surface flatness within ± 1 nm at the imaged region.
Figure 2.3 SEM cross-section of a (100) SIMOX-SOI wafer after CMP and thermal oxidation thinning, showing a top Si layer of 144 nm. The original Si thickness was $7 \pm 0.04 \mu m$.

2.1.2 Submicron SOI island etching

Electron beam lithography (EBL) was employed to form submicron Si islands on the thinned SOI. Dow Corning’s FOx-12 flowable oxide, a flowable inorganic polymer, spin-coated onto the substrate, was used as the EBL resist. The active component in this EBL resist is hydrogen silsesquioxane (HSQ). The primary constituent of this resist, $(\text{HSiO}_{3/2})_n$, forms cross-linked SiO$_2$ after exposure which can be removed in BOE.

Once formed into islands, HSQ acts as a protecting mask for the underlying Si during an inductively-coupled plasma (ICP) etch to define the SOI islands. This ICP etch is performed in an Alcatel 601e reactive-ion etch system (RIE) using SF$_6$ and O$_2$ at -120 °C. Low temperature is used to achieve high selectivity between the mask and Si [54]. The etch recipe is selective between Si and HSQ to avoid the erosion of HSQ during the formation of Si islands. The Si etch rate is approximately 186 nm/minute with a 20:1
etch selectivity between Si (100) and HSQ at -120 °C, Figure 2.4. Using this selective etch, the lateral shrinkage of the HSQ mask is negligible during the 2 minutes of ICP etch to form the Si islands.

Figure 2.4 Etch rate selectivity between Si (100) and etch mask, hydrogen silsesquioxane (HSQ), using SF$_6$ and O$_2$ reactive ion etch at -120 °C.

After the formation of the Si islands, InAs was grown using either MBE, a Riber 2300 solid source MBE system, by the April Brown group, Duke University, or using MOCVD, a house-constructed horizontal MOCVD reactor, by the Thomas Kuech group, University of Wisconsin at Madison.
2.2 Growth of InAs on patterned submicron SOI islands

2.2.1 MBE Growth of InAs on patterned submicron SOI islands

On different substrates, the MBE growth condition has been explored in multiple dimensions. More than thirty growths were performed. The growth variables include the Si substrate orientation, III/V flux ratio, III/V source materials, growth temperature, and post growth annealing. Table 2.2 illustrates the explorations using MBE at Duke.

Table 2.2

Thirty-two MBE growths of InAs on Si vs. substrate orientation, III/V flux ratio, As source, growth temperature, and post growth annealing.

<table>
<thead>
<tr>
<th>32 GROWTHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 surfaces</td>
</tr>
<tr>
<td>Si (100), (111), and (211)</td>
</tr>
<tr>
<td>SOI (100) and SiO₂</td>
</tr>
<tr>
<td>2 templates</td>
</tr>
<tr>
<td>bulk and patterned</td>
</tr>
<tr>
<td>6 different V/III flux ratios</td>
</tr>
<tr>
<td>from 4.65 to 58.14</td>
</tr>
<tr>
<td>As₂ and As₄ sources</td>
</tr>
<tr>
<td>7 different growth temperatures</td>
</tr>
<tr>
<td>110, 150, 220, 230, 250,</td>
</tr>
<tr>
<td>3 post-growth annealing temperatures</td>
</tr>
</tbody>
</table>

The characteristics of the InAs growths on unpatterned substrates at different growth conditions, some of which are listed in Table 2.2, have been reported by collaborators from Duke University in [55]. Yoon et al. show that the substrate
orientation has no effect on the size and density of InAs quantum dots (QDs) while V/III beam fluxes ratio and growth temperature do [55]. By lowering the V/III flux ratios from 58:1 to 10:1 at a growth temperature of 230 °C, Yoon decreased the height and increased the density of InAs QDs by 47% and 75%, respectively. Increasing growth temperature from 220 to 300 °C under a V/III beam ratio of 29:1, Yoon reported an increase of InAs QDs height by 62% [55]. Yoon shows Si native oxide reduces from 1 to 0.5 nm when treated with 0.01% - 1% HF solutions before loading to the MBE growth chamber [55]. More detailed analysis on the growth of InAs on unpatterned Si substrates should be read from [55]. This section focuses on MBE growth of InAs on patterned (100) SOI substrates.

This section presents one experimental set designed to show the Si island size and growth temperature effects on MBE InAs-on-SOI structures. After the thinning of SOI from 7 μm to a few hundred nanometers, negative EBL and low temperature RIE then follow, as have been described in Section 2.1, to create the submicron islands on three 1.5 × 1.5 cm² samples, Figure 2.3. Using 3D-SEM and atomic force microscopy (AFM) measurements, the island heights are show ranging from 150 to 400 nm in a 10 micron field. Submicron patterns include Si islands size of 200 × 200 and 400 × 400 nm² and Si linewidths of 200 and 400 nm. After patterning, samples with the Si islands protected with FOx-12, were transferred to Duke University. FOx-12 was next removed in a 15 s buffered-HF dip, Figure 2.5, and samples were loaded directly into the MBE system. To observe the influence of the temperature on the film, 40 nm of InAs was deposited with a V:III flux ratio of 33:1 at three different temperatures, 110, 150 and 250 °C.
Figure 2.5 SEM image of an array of 400 × 400 µm$^2$ SOI islands after F0x-12 removal and before MBE growth on InAs.

At 250 °C, two different kinds of InAs morphology on submicron Si islands are observed, planar and grainy, shown in Figure 2.6(a) and (b), respectively. The original Si island size, 500 × 500 nm$^2$, is indicated by the dashed box in Figure 2.6(a). Flat morphology, observed in SEM, indicates the possibility of a single-crystalline film. At 250 °C, about 25% of 500 × 500 nm$^2$ and 75% of 200 × 200 nm$^2$ Si islands generate flat InAs morphology. Figure 2.7 shows that two adjacent 200 × 200 nm$^2$ Si islands both exhibit flat morphology.
Figure 2.6 SEM images of 250 °C MBE InAs growths on (100) 500 × 500 nm$^2$ SOI islands with a V/III ratio of 33:1: (a) around one-in-four growths appear to be single-crystal, (b) some appear to be polycrystalline. The dashed outline in (a) is the size of the Si island underneath.

Figure 2.7 SEM images of 250 °C MBE InAs growths on (100) 200 × 200 nm$^2$ SOI islands.
In Figure 2.6(b), the growth of InAs appears to be in the Volmer-Weber (VW) growth mode, which is expected for the high lattice mismatch of InAs to Si, 11.6%. The VW island size is about 50 – 75 nm. The flat morphology in Figure 2.6(a) could be formed from merging of multiple InAs islands which have the same vertical growth rate, nucleated at the same time. In Figure 2.7, the Si mesa template is only 200 nm. Since the growth conditions are the same as Figure 2.6, it is likely that 50 – 75 nm VW islands nucleated at the same time and merged together as they grew.

From SEM images of nucleation at two other lower temperatures explored, 110 and 150 °C with V:III ratio of 33:1, only granular structures are observed on both 500 × 500 and 200 × 200 nm² size Si islands. In Figure 2.8 (a), at 110 °C, little irregular shaped InAs pebbles have been deposited on three out of four 500 × 500 nm² Si islands, leaving the fourth one blank. On Si islands of the same size in Figure 2.8 (b), InAs nucleation at 150 °C results in an apparent polycrystalline structure, formed on all three of the islands.

![Figure 2.8 SEM images of MBE growth of InAs-on-SOI islands: (a) at 110 °C and (b) at 150 °C.](image-url)
One of the islands has disengaged from the surface, leaving an empty pit and revealing the underlying BOX. Generally as shown in Figures 2.6 and 2.8, the coverage of InAs on the Si islands is reduced with temperature.

In addition to SOI island patterns, SOI lines with submicron width were also formed. By just having the size of patterns submicron in one planar dimension, lines with submicron width can achieve smooth morphology. For the 250 °C growth temperature, patterned SOI lines of width 200 nm also appear by SEM to produce smooth, flat InAs along Si lines as long as a few microns, Figure 2.9(a). Wider 500 nm lines, all had a granular structure, Figure 2.9(b), similar to that shown in Figure 2.6(b). No smooth morphology of InAs has been observed for 500 nm wide lines across a 1 × 1 cm² area covered with patterns.

![SEM images of the 250 °C MBE InAs growth on patterned SOI lines](image)

Figure 2.9 SEM images of the 250 °C MBE InAs growth on patterned SOI lines: (a) 200 nm width and (b) 500 nm width. Only on the 200-nm-width lines is smooth, flat growth of InAs observed.

The flat InAs line morphology could also result from the merging of VW islands nucleated at the same time and having the same vertical growth rate along the Si line. The
nucleation of the VW islands could have been enhanced at the Si pattern edge. That is, the edge may act as a heterogeneous nucleation site, increasing the nucleation rate there and forming nuclei at about the same time in the early stage of growth. If they grow at the same rate, they would then have the same height and when they merge together as they grow laterally as well as upwards, they would form a film of uniform thickness. When the Si lines are narrow, most of the InAs nucleation sites sit right next to the edge of the line, and merge into a flat line. This edge influence can also be observed in both Figures 2.6(b) and 2.9(b), showing some flat regions right along the edge of the patterns. If it is true that enhanced nucleation at edges results in early nucleation there, it is possible that nucleation is also enhanced on the flat surface adjacent to the edge nuclei. This could explain why at least some of the Si islands grow an essentially uniform film. The 500 nm lines do not form a uniform film, although at least some of the Si islands of the same dimension do. This may be because the Si islands have four nearby edges to generate the initial edge nuclei, compared to two edges for the lines.

Lower temperatures, 110 and 150 °C, show only irregular InAs nucleation on lines of widths, 200 and 500 nm. Similar to what has been observed on the growth on square patterns shown in Figure 2.8, the coverage of InAs over the Si lines, shown in Figures 2.10, decreases with temperature.
Growth of InAs on Si with mesa size of more than 1 µm in both planar dimensions only generates granular structures at all three temperatures, Figure 2.11. The density and size of InAs islands increase with temperature. In SEM images shown in Figure 2.11, at 250 and 150 °C, InAs islands form into a film, while at 110 °C InAs islands appears to be discontinuously distributed. Zhao also reported increase of InAs island size while depositing InAs on (100) Si substrate in the range 295 to 410 °C [56]. At higher substrate temperature, adatoms diffuse more rapidly, causing more significant coalescing of small InAs islands to form larger ones [56].

Although at 250 °C, an InAs film of uniform thickness can be formed on 500 and 200 nm Si islands, Figure 2.6(a) and Figure 2.7, respectively, InAs islands in Figure 2.11(a) are all less than 200 nm. This is consistent with the edge nucleation concept,
because far from edges, nucleation of InAs islands would nucleate more slowly, and could nucleate at different times and grow to different heights, as observed.

Figure 2.11 SEM images of the MBE InAs growth on a 100-μm-scale Si pad at (a) 250 °C, (b) 150 °C and (c) 110 °C, with V:III flux ratio of 33:1.

In conclusion, using MBE, InAs films of uniform thickness can be grown on patterned SOI structures at growth temperature of 250 °C and V:III ratio of 33:1. By depositing InAs on patterned submicron SOI, granular morphology can be suppressed to produce planar InAs structures on Si islands as large as 500 × 500 nm² squares and 200-nm-wide lines of microns long at 250 °C. When growth temperature is lower than 150 °C, no flat films are achieved and the coverage of the InAs film on Si islands decreases as well.
Other than a temperature window for the planar growth of InAs, there is also a pattern size limit to the underlying Si islands, which act as the crystal template. The size limit of Si islands for planar nucleation is different for different types of patterns. Although planar InAs/Si structures does not appear for lines of width 500 nm, they have been seen on square patterns of size $500 \times 500$ nm$^2$.

2.2.2 MOCVD growth of InAs on submicron Si islands on SOI

Growth of InAs films were explored using a custom horizontal MOCVD system, by collaborators Smita Jha and Dr. Thomas Kuech at University of Wisconsin, Madison. Similar to the exploration of MBE InAs process, MOCVD growths have been made vs. Si substrate orientation (100), (111) and (211), and on (100) SOI, vs. growth temperature, 280 – 650 °C, vs. V/III ratio, 28 – 120, and vs. patterned and unpatterned substrates.

The characteristics of MOCVD InAs growth on unpatterned (100), (111) and (211) Si substrates have been reported by Jha et al. in [57] and [58]. On all Si substrate orientations, InAs growth resulted in the VW island nucleation over the investigated temperature range, 280 – 650 °C. The island size increases from ~20 nm at 280°C to 5-6 μm at 650 °C [58], which is attributed to the increase in lateral surface diffusion with temperature [59]. At 280°C, the root-mean-square (RMS) roughness of the InAs film grown on (211) Si was 0.56 nm, which is less than 0.9 and 1.3 nm roughness found when InAs was grown on (100) or (111) Si, respectively. The smoother InAs films on (211) Si may be a results of its being a neutral interface between the polar InAs and the non-polar Si [58] [60] and its lower density of anti-phase domains as (211) Si provides two distinct bonding sites for the incoming group III and the group V atoms [58] [61]. Jha found that
V:III ratio has to be increased with decreasing growth temperature to prevent vapor-liquid-solid growth, which forms droplets and nanorods on the surface [58]. V/III ratio was increased from 25 to 90 for growths below 300 °C [58]. More detailed discussion of the MOCVD growth of InAs on unpatterned Si substrates can be found in [58].

This section focuses on the growth of patterned submicron (100) SOI and discusses one experimental set designed to show the Si island size and growth temperature effects on MOCVD InAs-on-SOI structures. The experiment started with the thinning of a 100 mm diameter (100) SOI substrate from 50 to ~5 ± 1 nm thickness. Three samples, ~1.5 × 1.5 cm², were cleaved from the thinned substrate and patterned separately. The detailed thinning and patterning has been discussed, Section 2.1. After the patterning, three samples with Si islands still covered with negative EBL resist, Fox-12, were sent to collaborators at the University of Wisconsin for MOCVD growth. Before the samples were loaded into MOCVD reactor, FOx-12, was removed in 1:10 BOE. The MOCVD chamber pressure of the system was 76 Torr. Trimethylindium (TMIn) was used as the group III precursor and tertiarybutyl arsine (TBAs) as well as arsine (AsH₃) were used as the group V precursors, with Pd-diffused hydrogen as the carrier gas. After loading into the reactor and prior to growth, the substrates were annealed under AsH₃/H₂ (P_{AsH₃} = 0.7 Torr) at 800°C for 5 minutes to transfer the H-terminated surface to an As-terminated surface [62]. After annealing, the substrate temperature was lowered to the specific growth temperatures, 450, 400 and 350 °C at a V:III ratio of 25. The targeted InAs thickness was 40 nm.

In the previous section, it was observed that MBE-grown InAs grows flat on patterned submicron SOI squares as large as 500 × 500 nm² and lines as wide as 200 nm.
However, in MBE growth, only two island sizes and line widths were explored, 200 and 500 nm. New patterns, as small as 100 nm and ranging from 100 to 1000 nm at a 100 step, were designed for the exploration of the MOCVD process. Figure 2.12 shows the test structure from the mask layout, with (a) squares size ranging from 100 × 100 to 1000 × 1000 nm² and (b), 10 µm long lines with widths ranging from 100 to 1000 nm. Figure 2.12(c) and (d) also presents the SEM images of the patterned Si islands corresponding to the designed square and line test structures. In Figure 2.12(d), part of the Si line is missing. The defects shown in Figure 2.12(d) could be the results of defects in the SOI revealed through the thinning process.
Figure 2.12 Test structures designed to explore the effect of Si pattern size on MOCVD growth of InAs: (a) matrix of squares, and (b) array of lines, with size changing from 0.1 to 1 µm, and the corresponding SEM images of Si islands and lines formed on SOI substrate (c) and (d), respectively.

Figure 2.13 shows an SEM image of MOCVD InAs growth at 450 °C on square and line test structures. Only the column with 100 nm squares appears to have one single InAs crystal nucleated. All the other squares, size 200 – 1000 nm, and all lines, width 100 – 1000 nm, appear to have multiple InAs grain nucleation, with average grain size of 100 - 200 nm. InAs grains do not appear to nucleate significantly on the SiO₂ surface. A few
InAs dots of 50-100 nm size are spotted on the SiO$_2$ in Figure 2.13 and could be the nucleation of some residue on the surface, which need to be further confirmed.

Figure 2.13 SEM image of MOCVD InAs nucleating on 100 – 1000 nm square and line test structures on SOI at 450 °C.

Although the targeted InAs growth thickness is 40 nm, the AFM measurements show the actual thickness deposited at 450 °C is 120 ± 30 nm. This discrepancy arises from assuming the growth rate on bulk Si would be the same as the growth on SOI islands. The SOI pattern used is only sparsely covered with Si islands. In Figure 2.13,
SEM image shows most of InAs nucleates on Si islands. The islands collected InAs from the greater SiO$_2$ surface resulting in a much thicker film than expected.

Figures 2.14 and 2.15 show SEM images of MOCVD InAs growths on square test structures sized 100 – 600 nm and line test structures with widths 100 – 1000 nm, respectively, at two growth temperatures, 400 and 350 °C. At 400 °C, InAs crystals of size 100 – 200 nm formed only on SOI islands; at 350 °C, InAs crystals of size 20 – 50 nm nucleated mostly around the edge of Si islands, leaving the Si islands uncovered.

![Figure 2.14 MOCVD InAs growth on six square test structures, 100 – 600 nm, at (a) 400 and (b) 350 °C.](image-url)
Figure 2.15 MOCVD InAs growth on line test structures, 100 -1000 nm wide, at (a) 400 and (b) 350 °C.

From SEM observations, at growth temperatures of 400 and 450 °C, with a V:III ratio of 25, growth of InAs seems to be selective. InAs film deposition only occurs on exposed Si crystal surfaces and is circumvented on surrounding SiO₂ surfaces. SEM observations of selective growth of InAs on Si over SiO₂ has been reported by Choi et al. [63] at a growth temperature of 430 °C when grown in patterned and opened SiO₂ windows on Si substrates. Choi et al. has interpreted the selective growth as a result of larger In adatom diffusion coefficients on SiO₂ over Si, $7 \times 10^{-9}$ over $10^{-20}$ cm²/s [63], and larger surface energy of SiO₂ over Si, 3.83 over 0.483 eV [63], causing the migration of In adatoms migrate from SiO₂ to Si at the pattern boundary, and resulting in the formation of InAs nucleation selectively on Si.

In summary, MOCVD growth of InAs on patterned SOI islands was examined as a function of island size between 100 and 1000 nm, and for growth temperatures 350, 400
and 450 °C. Single grain InAs nucleation was observed at an SOI island size of 100 × 100 nm² at 450 °C. All patterns larger produced multigrained growths.

The other discovery, under SEM, is that at higher growth temperature, 400 and 450 °C, InAs nucleates on crystalline Si islands on SOI substrates selectively. The advantage of selective growth of InAs over patterned Si structure on SOI substrate is that no further patterning is required to isolate devices. Once the growth is completed, the InAs/Si structure is ready for source and drain metallization or gate stack formation. Using this selective growth approach, MOSFETs, with MOCVD InAs/Si structure as the channel, have been fabricated, Chapter 4.

2.3 Post-growth pattern-then-anneal process

In this approach, InAs was deposited by MOCVD onto an unpatterned SOI substrate. Then InAs/Si islands were formed and capped with PECVD SiO₂ and annealed. Annealing is intended to recrystallize the as-grown polycrystalline InAs film as outlined in Chapter 1, Figure 1.11.

The SOI samples used in this experiment was cleaved from the same thinned 100 mm (100) SOI used for MOCVD growth described in Section 2.1 and 2.2.2. The growths of InAs are performed in the same MOCVD system at University of Wisconsin. Two thicknesses, nominally 10 and 30 nm, of InAs were grown at 350 °C. Following the growth, InAs/Si islands were formed by etching InAs in an acetic-acid-based solution (1 acetic: 2 peroxide: 20 H₂O), and Si in an Alcatel 601e RIE with SF₆ and O₂ at -120 °C using Fox-12 as the mask and negative EBL process. After the formation of the InAs/Si mesas, Fox-12 was removed in BOE and 50 nm of PECVD SiO₂ was deposited to
encapsulate the InAs/Si mesa for the high-temperature annealing process. The encapsulated InAs/Si structures were annealed in the MOCVD system at 800 °C for 30 minutes in AsH₃ and then analyzed by transmission electron microscopy (TEM) and transmission electron diffraction (TED) in a JEOL 2010F system by Professor Tung-Sheng Kuan, State University of New York, Albany.

Figure 2.16 shows the TEM cross section, (a), and corresponding TED pattern, (b), at a corner of an unannealed InAs/Si control structure encapsulated in PECVD SiO₂. The cross section in Figure 2.16(a) shows that InAs forms into isolated islands on the Si template. Without including the taper at the edge of the InAs/Si mesa and the gap between the two InAs islands, the actual thickness of InAs is read to be around 17 ± 2 nm, which is thicker than the targeted 10 nm.

Electron diffraction patterns were taken at the InAs/Si interface along the [110]_{Si} zone axis. The size of the selected area aperture (SAD) is chosen so that only a circular sample area of 200 nm in diameter is contributing to the diffraction pattern. Although this is larger than the thickness of the BOX, the Si substrate of the SOI was excluded by the SAD aperture and only diffraction from the InAs layer and the top thin Si layer is observed. Some Si oxide of the SOI and the amorphous Pt overcoating from focus ion beam are also included by the aperture, and they produce only faint diffused rings.

The lattice parameters of the InAs relative to the thin Si have been measured from the negatives of the diffraction patterns. The darker dots further away from the center are due to Si and the weaker dots closer are from InAs. The alignment of the diffraction pattern, Figure 2.16(b), shows that InAs takes on the crystal orientation of the (100) Si template and is both crystalline and epitaxial. The relative lattice mismatch can be
calculated from the distance ratio of the diffraction spots from same crystal plane, aa and bb in Figure 2.16(b). Without annealing the lattice mismatch calculated from Figure 2.16(b) is 11.2%, which is close to that between unstrained Si and InAs, 11.6%. The close agreement of the lattice mismatch indicates that the as-grown InAs islands are relaxed.

Figure 2.16 (a) TEM cross-sectional image of unannealed (17/5 nm)InAs/Si structure, and (b) selected-area TED pattern taken from the corresponding interfaces.
Figure 2.17 shows the TEM cross section, (a), and corresponding TED pattern, (b), at a corner of an InAs/Si island encapsulated in PECVD SiO$_2$ after a thermal anneal at 800 °C for 30 minutes. Transmission electron diffraction patterns taken from the cross-section, shows the lattice mismatch between the InAs and Si has reduced to 4.2%, Figure 2.17(b). A slight difference in camera constant between different patterns taken from the same grid is possible due to refocusing of the objective lens of the TEM. This would cause and error in comparing the lattice parameters determined from the diffraction patterns of the annealed and unannealed specimens. Neglecting this possible source of error, measurements made on the original negatives by Prof. Kuan shown that the lattice parameter of the Si is the same before and after annealing, but the lattice constant of InAs is reduced by a large amount, ~6%, after annealing, Figures 2.16 and 2.17.
Figure 2.17 (a) TEM cross-sectional image of 17/5 nm InAs/Si structure annealed at 800 °C for 30 minutes, and (b) selected-area TED pattern taken from the corresponding interfaces. The area in the dashed circle shows the twinning in both InAs and Si layers.

Thicker InAs films, ~45 nm (originally targeted for 30 nm) on SOI were also characterized by TED, after MOCVD growth, patterning, capping, and annealing. For these thicker films, the TED patterns do not show significant differences following
anneal, i.e. the lattice mismatch remains about the same as shown in Figure 2.18. Thicker InAs films are crystalline and do not appear to take on the lattice constant of the (100) Si template. Lattice mismatches calculated from 2.18 (a) and (b) are both ~11%, indicating both InAs and Si films retain their bulk lattice structure.

Figure 2.18 TED patterns of (a) unannealed and (b) annealed 45/5 nm InAs/Si structure.

In summary, a second approach for forming crystalline InAs on Si has been explored. In this approach blanket MOCVD InAs growth on SOI is followed by submicron mesa formation, dielectric encapsulation, and annealing. TEM and TED are performed to characterize the crystallinity of the InAs/Si. TED patterns confirms that MOCVD InAs forms crystal islands on the Si surface and takes on the crystal orientation of the (100) Si template. As-grown InAs films seem to remain relaxed, confirmed by the lattice mismatch calculated from TED patterns. Annealing at 800 °C for 30 minutes has significant effects on the InAs/Si structures when InAs film thickness is comparable to that of Si. When InAs and Si film thicknesses are 17 and 5 nm, respectively, annealing
causes InAs to reduce its lattice parameter and the misfit. However, when InAs is much thicker, 45 nm, the annealed structure retains the relaxed state.

The reduction of the misfit upon annealing of the 17/5 nm structure is surprising, because the relaxed state of the InAs is to be expected due to the large misfit. During the first few monolayers of growth, misfit dislocations should form, relaxing the elastic strain in the InAs as observed for both 17 and 45 nm InAs films. Since films form misfit dislocations because the energy associated with the array of dislocations is less than the elastic strain energy that would be present without them, it is difficult to understand why the dislocations would be rejected from the 17 nm film during annealing, increasing the strain energy of the InAs. The fact that the InAs is thicker than the Si after growth suggests that if the Si were not bonded to the BOX, the strain energy of the system in a pseudomorphic state would be reduced, possibly favoring a loss of dislocations and introducing some strain in the Si. However, the Si lattice parameter did not change upon annealing. Another possibility is that diffusion of Si into the InAs altered its lattice parameter, as observed from the diffraction patterns, but there is no direct evidence to support this mechanism.

2.4 Conclusion

Both MBE and MOCVD have been used to explore the deposition of InAs on Si. Depositing onto patterned SOI islands, both techniques have been observed to exhibit flat growth InAs structures at sufficiently submicron size and in a narrow growth temperature window. Deposited using MBE, planar InAs/Si structure can be as large as 500 × 500 nm² and 200 nm wide lines extend for several microns in length with planar
growth. MOCVD growth achieves planar structures only for sizes beginning at $100 \times 100 \text{ nm}^2$ and grows selectively relative to $\text{SiO}_2$ at temperature higher than $350 \, ^\circ\text{C}$. The relative lattice parameters between InAs and Si of comparable thickness can be change upon annealing. The lattice mismatch of 17/5 nm InAs/Si is changed from 11.2% to 4.2% after being annealed at 800 °C for 30 s.
Chapter 3
Formation and Characterization of Al\textsubscript{2}O\textsubscript{3} Gate Dielectrics

Two methods for Al\textsubscript{2}O\textsubscript{3} formation on InAs were explored: PVD using electron-beam (e-beam) evaporation of oxide source in an oxygen background, and ALD using trimethylalumini-num (TMA, Al\textsubscript{2}(CH\textsubscript{3})\textsubscript{6}). Variable-angle spectroscopic ellipsometer (VASE) and AFM were used to characterize the physical properties of Al\textsubscript{2}O\textsubscript{3} films. Metal-oxide-semiconductor (MOS) capacitors were formed on both Si and InAs substrates to characterize the electrical properties of these heterostructures.

3.1 Physical Vapor Deposition of Al\textsubscript{2}O\textsubscript{3}

E-beam assist PVD has been used to deposit a wide variety of dielectric films, including Al\textsubscript{2}O\textsubscript{3} [64] [65] [66]. Using an evaporation process in an oxygen background of 1 × 10\textsuperscript{-5} Torr, Sararie \textit{et al.} [64] deposited Al\textsubscript{2}O\textsubscript{3} on Si, reporting Al\textsubscript{2}O\textsubscript{3} films with low field resistivity of \(~1\times 10^{13}\) Ω-cm, breakdown fields of more than 3 MV/cm, and a dielectric constant of 7.5. Using an e-beam enabled PVD technique at an elevated substrate temperature of 200 °C Bhan \textit{et al.} deposited Al\textsubscript{2}O\textsubscript{3} films on a Si-doped n\textsuperscript{+} GaAs substrate, showing high resistivity of \(3.6\times 10^{11}\) Ω-cm and a dielectric constant of ~4.5 [66].

In this section, aluminum oxide was deposited in an AIRCO Temescal FC1800 e-beam evaporator at a base pressure of \(~4 \times 10^{7}\) Torr without substrate temperature control. Due to the lack of InAs at the time of the PVD experiments, bulk Si substrates
were used. Oxide film were deposited onto a 100-mm-diameter RCA cleaned and hydrogen-terminated Si (100) substrate (phosphorous-doped, 10 – 40 Ω cm, ~1 – 2 × 10^{14}/cm³) by e-beam evaporation of 99.99 % Al₂O₃ pellets, from Kurt J. Lesker Company, in an O₂ overpressure of 5 × 10⁻⁵ Torr at a rate of 1 ± 0.2 Å/s. For the electrical tests, Al dots, 150 μm in diameter, were deposited onto the oxide film through a Mo stencil mask. The back side of the wafer was evaporated with Al to provide an electrical contact to the back of the Si and a low resistance electrical connection to the probe station wafer chuck.

3.1.1 Physical Characterization of PVD Al₂O₃

Variable-angle spectroscopic ellipsometry measurements were made at four different illumination angles to the substrate and over the wavelength range from 260 to 900 nm. The VASE data was fitted to estimate the thickness and refractive index of the PVD Al₂O₃ using the Cauchy model. Table 3.1 shows three data point collected across the wafer diameter, showing uniformity of ± 2%. Points 1 and 3 are about 60 mm apart, point 2 is located between point 1 and 3.

<table>
<thead>
<tr>
<th></th>
<th>Position 1</th>
<th>Position 2</th>
<th>Position 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (Å)</td>
<td>303.8 ± 0.2</td>
<td>312.5 ± 0.2</td>
<td>312.7 ± 0.2</td>
</tr>
<tr>
<td>Refractive index @ 6300 Å</td>
<td>1.621 ± 0.001</td>
<td>1.620 ± 0.001</td>
<td>1.622 ± 0.001</td>
</tr>
</tbody>
</table>

Figure 3.1 compares the measured refractive index at point 2, which is about the center of a 100 mm diameter wafer and the reference from the data base of the VASE
across wavelengths from 300 to 860 nm. The measured values are approximately 8%, less than the reference values throughout the wavelength measured.

Figure 3.1 Comparison of the refractive index of Al₂O₃ obtained by fitting VASE measurement data with that from the J. A. Woollam Co., Inc. data base.

To characterize the etch rate of the PVD Al₂O₃ film, a 50-nm-thick Al₂O₃ film was deposited using the same surface preparation and deposition conditions through a Mo shadow mask, forming Al₂O₃ patterns directly. Three different etching solutions were tested: 1 HCl: 10 H₂O, 1 HCl: 1H₂O, and 1:10 BOE. Samples with Al₂O₃ patterns were dipped into both HCl solutions with agitation for as long as 2 minutes, which gave no reduction of the film thickness. The Al₂O₃ film etched in the 1:10 BOE solution with an etch rate of ~4.1 nm/s, as shown in Figure 3.2. The etch start-up delay, approximately 1.5 s, could not be understood at this stage and needs further investigation.
Figure 3.2 Etch depth vs. etch time for e-beam-deposited Al₂O₃ in 1:10 BOE. The etch rate is ~4.1 nm/s.

3.1.2 Electrical Characterization of PVD Al₂O₃

Current-voltage (I-V) measurements were acquired using an Agilent 4155 semiconductor parameter analyzer and on-wafer probing using a Cascade Microtech 11861 probe station. Figure 3.3 shows the top-to-back measurement of the leakage current through the Al₂O₃ film. The measurements were made in the dark. The semiconductor side of the Al/Al₂O₃/n-Si was connected to common through the wafer chuck. The voltage is swept from 0 to ±1 V. The leakage current at 1 V is in the order of 10⁻⁹ A/cm².
Figure 3.3 Current-voltage characteristics of Al/Al₂O₃/n-Si MOS diode measured in the dark.

To test the breakdown field, successive current ramps were applied to the Al/Al₂O₃/n-Si MOS diode to find the breakdown electric field. Figure 3.4 shows the breakdown field of the Al₂O₃ film is close to 6 MV/cm. The current sweeps from 0 to 1 μA, at a 0.01 μA increment, in each curve and the numbering indicates the sequence of the measurements. The destructive breakdown takes place on this scan on the 3rd sweep, and the resistance of the film decreased, 4th curve. Two more breakdown measurements were made on the same sample, also showing similar breakdown voltage close to 6 MV/cm.
Figure 3.4 Break down measurement of a PVD Al₂O₃ film on Si. Numbers 1 – 4 indicate the sequence of the measurement. Catastrophic breakdown happens at the 3ʳᵈ sweep when the electric field reaches ~6 MV/cm.

To estimate the Al₂O₃ dielectric constant in the MOS capacitor, capacitance-voltage (C-V) measurements were performed using an Agilent 4294A precision impedance analyzer on the Cascade Microtech 11861 probe station after an open-short-load calibration on a Cascade impedance standard substrate. The top-to-back C-V measurement was performed at four different frequencies, 1, 10, 100, and 1000 kHz, and from – 4 to 4 V with the Si substrate common, Figure 3.5. The solid C-V curve in Figure 3.5 is simulated C-V using Bandprof³. In the simulated C-V, parameters of Al₂O₃ are taken from Table 1.4, which shows a dielectric constant of 9 [40] and conduction offset to Si 2.6 eV [41]. The barrier height between Al contact and Al₂O₃ is taken to be 3.1 eV,

³ 1D Poisson simulator of William R. Frensley, University of Texas, Dallas.
which is the average between experimental value, 2.9 eV, from [67] and theoretical value 3.3 eV from [68].

![Figure 3.5 Capacitance-voltage measurements of Al/Al₂O₃/n-Si MOS capacitor with the Al₂O₃ deposited by electron-beam evaporation.](image)

In Figure 3.5, the large frequency dispersions in the C-V curves in the depletion and inversion regimes are due to the varying response of interface traps. The net capacitance increases at a given applied bias due to the increasing contribution of an interface-trap capacitance in parallel with the silicon space charge capacitance. Interface traps can dynamically be charged and discharged. At negative bias, most of the interface traps are not fast enough to respond to the 1 MHz signal, and more interface traps respond as the measurement frequency is lowered, resulting in a larger interface-trap capacitance at 1 and 10 kHz. To eliminate the capacitance contributed by the frequency response of interface traps, accumulation capacitance at 1 MHz is used for the calculation of dielectric constant of Al₂O₃. In Figure 3.5, 36 pF at 100 MHz, and the Al₂O₃ thickness
of 304 – 313 Å, from Table 3.1, the dielectric constant of can be estimated by fitting the simple parallel plate capacitance equation, \(C = \varepsilon_0kA/t_i\). The dielectric constant of PVD Al₂O₃ is 7.1 ± 0.1, which is lower than the bulk value, 9.

The effective barrier height of the MOS structure can be extracted from high field characteristics, Figure 3.4. In a MOS diode, carriers tunnel through only part of the insulator layer at high electric field, the triangular barrier of the oxide as shown in Figure 3.6.

![Energy band diagram of a Si/Al₂O₃ MOS dielectric.](image)

The tunneling current density is described by Fowler-Nordheim (F-N) for field-dependent tunneling through a triangular barrier [70].

\[
J = \frac{q^3E^2}{16\pi^2\hbar\Phi_B} \exp \left( -\frac{4\sqrt{2m^*\Phi_B^2}}{3\hbar qE} \right)
\]

(4.1)
where \( J \) is the tunneling current density, \( q \) single electron charge, \( \xi \) electric field across the insulator, \( \hbar \) reduced Plank constant, \( \phi_B \) effective barrier height between semiconductor and insulator, and \( m^* \) electron tunneling effective mass of the insulator.

The effective barrier height between the semiconductor and the insulator can be determined by plotting the \( \ln \left( \frac{J}{\xi^2} \right) \) vs. \( 1/\xi \). From the linear slope of this relation, the effective barrier height can be extracted. From Figure 3.7, the barrier height at the Si and Al\(_2\)O\(_3\) interface is calculated from Eq. (4.1) to be 2.4 eV, which is lower than the value shown in Table 1.4, 2.6 eV. This 0.2 eV discrepancy could be a result of image-force-lowering [70] [71]. The deviation from the linear region of F-N in the low-field region shows the transition from F-N field emission to thermionic emission [72] [73] [74]. The high field deviation mechanism is more complicated and has not been explained satisfactorily [73] [74].

![Figure 3.7 Fowler-Nordheim tunneling analysis of Al/Al\(_2\)O\(_3\)/Si MOS diode, 30 nm PVD Al\(_2\)O\(_3\) on n-Si.](image)

\[
\text{Slope} = -\frac{4\sqrt{2m^*(q\phi_B)^3}}{3\hbar q\xi}
\]
3.1.3 Conclusions on PVD Al$_2$O$_3$

Electron-beam enabled PVD Al$_2$O$_3$ film has been deposited onto an $n$-Si substrate at a rate of 1 Å/s, in an oxygen overpressure of $5 \times 10^{-5}$ Torr. The film has a refractive index of 1.62 and etches in 1:10 BOE at 4.1 nm/s. The leakage current at 0.33 MV/cm is in the order of $10^{-9}$ A/cm$^2$, ~10 times lower than that reported in [64] and in the same order to that in [66]. In [64] Saraie et al. deposited ~150 nm of Al$_2$O$_3$ in an oxygen pressure of $10^{-5}$ Torr on Si substrate, while in [66], ~150 nm of Al$_2$O$_3$ is e-beam evaporated onto GaAs substrate without oxygen background. Break down voltage of ~6 MV/cm is higher than ~3 MV/cm, reported in [64]. Dielectric constant extracted from $C$-$V$ measurement is $7.1 \pm 0.1$ which is comparable to [64], 7.5, and higher than [66], 4-4.5 and close to that of bulk material, 8 - 10. The dielectric constant of 7.1 is comparable to films deposited using ALD [52], varying between 5.3 to 8.5. By fitting the high-field I-V to F-N tunneling equation, barrier height at the Si and Al$_2$O$_3$ interface is calculated from be 2.4 eV, which is close to the theoretical value of 2.6 eV [41].

3.2 Atomic Layer Deposition of Al$_2$O$_3$

Atomic layer deposition systems alternately pulse the precursor gases and vapors onto the substrate surface and rely on subsequent chemisorption or surface reaction of the precursors [75]. An inert gas, used as a carrier, purges the reactor between the precursor pulses. The process can be adjusted to be saturative under properly-adjusted experimental conditions, and the thickness increase can be constant in each deposition cycle [75]. The growth of the conformal thin films is then self-limiting, resulting in an accurate deposition rate [75]. Atomic layer deposition is now a common approach for preparation.
of high-k dielectrics [39] [49] [52] [76] [77] [78] [79]. In this work, the ALD of Al₂O₃ films is realized in a Cambridge NanoTech Inc. ALD S100 system, which has a chamber pressure maintained at 0.4 Torr and carrier gas of N₂ with constant flow of 20 sccm. A substrate temperature of 200 °C is used. Before growth, a N₂ purge is performed for 5 minutes. A growth cycle starts 10 s after the purge with a 15 ms trimethylaluminum (TMA, Al₂(CH₃)₆) pulse followed by a 5 s purge delay, and a 15 ms H₂O vapor pulse. Between each pulse there is a purge delay of 5 s. The thickness of Al₂O₃ is controlled by programming the number of TMA and H₂O pulse cycles.

Films were deposited on two substrates: p-type B-doped Si and n-type S-doped InAs, of doping concentration ~10¹⁴ and 10¹₈ cm⁻³, respectively. The Si substrate is RCA cleaned and H-terminated in 1:10 BOE and InAs is soaked in NH₄OH (29%) solution for 3 minutes before transferring to the ALD growth chamber. Three growths of 18, 36, and 73 ALD cycles, were carried out to achieve film thicknesses of 2, 4, and 8 nm, respectively. Following the growth, wafers from each growth were subdivided into 3 pieces, and the 3 pieces were subsequently annealed in an RTP-600S at 250, 300 and 350 °C for 30 s in a N₂ ambient, resulting in 9 Al₂O₃ on InAs samples. For the electrical test, Al dots, 150 μm in diameter, were deposited onto the oxide film through a Mo stencil mask. The back side of the wafer was evaporated with Al to improve the electrical contact to the probe-station chuck.

3.2.1 Physical Characterization of ALD Al₂O₃

The thickness and index of refraction of the ALD Al₂O₃ films were measured using VASE and the RMS roughness of the films was obtained by scanning areas of 2 × 2
µm² and 0.4 × 0.4 µm², using an AFM. VASE measurements, using Cauchy model, for Si are collected along the radius of a 100-mm wafer quarter, and, for InAs, across approximately 2 × 2 cm² samples. The measured results are summarized in Table 3.2 and plotted in the figures following the Table.
Table 3.2

Characterization of growth and post-growth annealing of ALD Al₂O₃ deposited on InAs and Si substrates

| Substrate | Anticipated thickness | ALD cycle | Annealing T (°C) | Before annealing | | | After annealing | | |
|-----------|----------------------|-----------|------------------|-----------------|------------------|-----------------|-----------------|------------------|
|           |                      |           | Thickness (Å)    | n @ 6300 Å      | RMS (Å)          | Thickness (Å)   | n @ 6300 Å      | RMS (Å)          | |
|           |                      |           |                  |                 | 2 × 2 µm²       | 0.4 × 0.4 µm²   | 2 × 2 µm²       | 0.4 × 0.4 µm²   | |
| InAs      | 2 nm                 | 18        | 31.6 31.1 31.5  | 1.6925 1.5224 1.5304 | 1.66 1.32 1.66  | 31.8 29.1 29.9 | 1.786 1.5604 1.5847 | 3.3 2.00 1.90 | 1.73 1.60 1.38 |
|           | 4 nm                 | 36        | 51.3 49.3 49.8  | 1.568 1.6121 1.5912 | 1.98 1.56 1.98  | 49.2 46.8 50.9 | 1.6139 1.7017 1.6779 | 1.58 1.95 1.68 | 1.35 1.37 1.31 |
|           | 8 nm                 | 73        | 87.8 87.5 84.1  | 1.6030 1.5818 1.6320 | 2.42 2.54 2.42  | 90.5 86.5 82.6 | 1.6235 1.5992 1.6487 | 2.11 2.03 1.95 | 1.83 1.83 1.86 |
| Si        | 8 nm                 | 73        | 85.4 91.1 81.9  | 1.7982 1.7972 1.8454 | 2 nm 1.63 1.7 1.45 | 80.3 80.6 80.9 | 1.8511 1.869 1.8637 | 1.82 1.43 1.73 | 1.6 1.32 1.61 |

66
The dependence of ALD Al₂O₃ thickness deposited on InAs vs. ALD growth cycle is shown in Figure 3.8(a). The thickness is linearly related to the number of ALD cycles and intercepts the y-axis with an apparent no-cycle thickness. This indicates there might be an interfacial layer forming between the InAs and Al₂O₃. Native oxide interfacial layers have been observed and confirmed using TEM by Wheeler and Kosel [80] for ALD HfO₂ on InAs and by Groner et al. [52] depositing ALD Al₂O₃ on Si, Huang et al. [47] depositing ALD Al₂O₃ on InGaAs, and Hou et al. [46] depositing ALD Al₂O₃ on InSb. The thickness of the annealed Al₂O₃ films is plotted against the ALD cycle in Figure 3.8(b). Comparing Figure 3.8(a) and (b), no clear thickness change is observed. The uniformity of the film thickness in an area of 2 × 2 mm² is within 5 % for all films.

Figure 3.8 Thickness of ALD Al₂O₃ films as measured by VASE (a) grown at 200 °C and (b) after post-growth anneal at 250, 300, and 350 °C, vs. ALD growth cycle, indicating a growth rate of 1Å /cycle.
Refractive indices, at a wave length 630 nm, of as-grown and annealed ALD Al$_2$O$_3$ films are plotted in Figure 3.9. The refractive index of bulk Al$_2$O$_3$ is shown in the plots as dashed lines. Similar to the e-beam evaporated Al$_2$O$_3$ depositions, most of the measured refractive indices of thin film Al$_2$O$_3$ are less than the bulk value. Wang et al. points out in [81] the difficulties in accurately measuring refractive index and thickness for ultrathin film of less than 10 nm using ellipsometry: the accuracy of the measurement decreases as the thickness of the film decreases. Annealing may have increased the nonuniformity of the film, which is reflected by comparing Figure 3.9(a) and (b), but even the annealed 20 cycle film only has a deviation of less than ±8%.

![Figure 3.9 Refractive indices taken at 630 nm wave length of ALD Al$_2$O$_3$ films (a) grown at 200 °C, and (b) post-annealed at 250, 300 and 350 °C.](image)

All ALD Al$_2$O$_3$ films on InAs show good global, 2 × 2 cm$^2$, uniformity, less than ±4 Å thickness variation, measured by VASE, Table 3.2. Since the gate of an extremely scaled transistor is only tens of nanometers, the nanoscale uniformity of the films is important. The RMS roughness of the ALD films on InAs, measured using AFM across
areas of $2 \times 2$ and $0.4 \times 0.4 \ \mu m^2$, is summarized in Figure 3.10. The RMS roughness of most ALD Al$_2$O$_3$ films is comparable to that of the original InAs surface, ~2 Å over a $2 \times 2 \ \mu m^2$ area, indicated by the dash lines in Figure 3.10. The annealed films are typically smoother. This is contrary to the observation by Groner et al. [52] and Copel et al. [82]. Both Groner [52] and Copel [82] reported voids in the Al$_2$O$_3$ films after annealing. However in both cases, Al$_2$O$_3$ films were deposited on Si substrates and much higher annealing temperatures, > 800 °C, are executed.

Figure 3.10 Roughness of ALD Al$_2$O$_3$ films deposited on InAs with thickness of, (a) 18, (b) 36 and (c) 73 ALD cycles. The films were annealed at three temperatures, 250, 300 and 350 °C. Solid and empty squares represent measurements taken from surface areas of $2 \times 2$ and $0.4 \times 0.4 \ \mu m^2$, respectively. The dashed lines in the plots indicate the roughness of InAs roughness before growth.
3.2.2 Electrical Characterization of ALD Al₂O₃

3.2.2.1 I-V characteristics of Al/Al₂O₃/n-InAs MOS diodes

Only one report has been made of electrical characterization of ALD Al₂O₃ films on InAs substrates [51]. In [51], a relatively thick film, 30 nm, is deposited and only one I-V plot of this thick film is presented. This dissertation is the first to show the properties of ultra thin, < 10 nm, ALD Al₂O₃ on InAs substrate.

Low leakage current is one of the measures of an insulating film. Figure 3.11 shows the MOS diode current scales to the thickness of the Al₂O₃ film. The thickness of the three ALD films are taken as average values from Table 3.2; the 18, 36, and 73 ALD cycle films have average thicknesses of 3, 5 and 8.5 nm, respectively. The leakage current of these Al/Al₂O₃/n-InAs diodes can be compared to results on In₀.₁₅Ga₀.₈₅As [47] and InSb [46]. The leakage current density of the Al/Al₂O₃/n-InAs diode in this study measured at 1 V bias, from Figure 3.11(a) are approximately $1.5 \times 10^{-9}$, $0.9 \times 10^{-8}$, and $1 \times 10^{-6}$ A/cm² for Al₂O₃ thicknesses of 3, 5 and 8.6 nm. Huang et al. [77] reported current densities of $\sim 10^{-9}$ A/cm² through an Au/(8.5 nm) Al₂O₃/In₀.₁₅Ga₀.₈₅As MOS diode at the same bias. Hou et al. [46], reported current densities in Pt/(13 nm)Al₂O₃/InSb diode at same bias is almost 10 time higher, $\sim 10^{-8}$ A/cm². The almost symmetrical I-V in both bias directions in Figure 3.11(a) could be an indication of surface pinning at the Al₂O₃/InAs interface, which fixes the surface potential for varied gate bias.
Figure 3.11 I-V characteristics of (a) Al/Al₂O₃/n-InAs and (b) Al/Al₂O₃/p-Si MOS diodes. Three curves in each plot correspond to ALD Al₂O₃ film thickness of 3, 5 and 8.6 nm deposited at 200 °C.

Post growth annealing, optimized at 360 °C for 30 s, following ALD at 300 °C, is shown by Li [51] to improved the quality of ALD Al₂O₃ films deposited on p-InAs substrate. In this dissertation, post-growth annealing is performed to observe the effects, shown in Figure 3.12. Figure 3.12(a), (b) and (c) compare post-growth annealing effects on the leakage current through Al/Al₂O₃/n-InAs MOS diodes with Al₂O₃ of 3, 5, and 8.6 nm, respectively. All the annealing temperatures studied in this dissertation increase the leakage current through the Al/Al₂O₃/n-InAs MOS diodes. Since no significant thickness changes have been observed after the annealing, the increasing current cannot be explained by increased tunneling caused by decreasing film thickness. It is mentioned by Li [51] that damage of Al₂O₃/InAs interface, resulting in degradation of I-V performance, was observed when annealing temperature is more than 360 °C, which is 60 °C higher than growth temperature. It is possible that for 200 °C film, 250 °C annealing temperature is already too high and damages Al₂O₃/InAs interface.
Figure 3.12 Comparisons of I-V characteristics of Al/Al₂O₃/n-InAs MOS diodes with 200 °C ALD Al₂O₃ with thicknesses of (a) 3, (b) 5, and (c) 8.6 nm, as grown and annealed at 250, 300, and 350 °C.

Figure 3.13 compares leakage current of the Al₂O₃ films before and after annealing at an electric field of 1 MV/cm, obtained by dividing the bias voltage with the thickness of the film. An increase of leakage current upon annealing at all the annealing temperatures, 250, 300 and 350 °C is observed for all the ALD Al₂O₃ films grown at 200 °C. There is not a clear correlation between amount of leakage current increase and the annealing temperature, e.g. higher annealing temperature causes larger increment of leakage current. But the leakage current does increase more in the thinner film after
annealing at the same condition. The leakage current of the 5 and 8.6 nm films increase by about 1 order of magnitude, from $10^{-9}$ to $10^{-8}$ A/cm$^2$, while the leakage current of the 3 nm film jumps up 4 orders of magnitude, from $10^{-6}$ to $10^{-2}$ A/cm$^2$.

![Leakage current through ALD Al$_2$O$_3$ films at an electric field of 1 MV/cm changes with film thickness and annealing temperature.](image)

Figure 3.13 Leakage current through ALD Al$_2$O$_3$ films at an electric field of 1 MV/cm changes with film thickness and annealing temperature.

Catastrophic breakdown electric field is measured by ramping up the current through top Al contact of the MOS diode till observing an irreversible drop of resistance of the MOS device. The breakdown fields of as-grown and annealed films are presented in Figure 3.14. The break down field is similar for all the films, ~6 MV/cm, which is close to bulk value, ~7 – 8 MV/cm [44]. No clear correlation between breakdown strength and annealing temperature or film thickness can be drawn.
Figure 3.14 Breakdown field of ALD Al$_2$O$_3$ films vs. oxide thickness and post-growth annealing temperatures, ~6 MV/cm.

3.2.2.2 Quasi-static (QS) C-V of Al/Al$_2$O$_3$/n-InAs MOS capacitors

Quasi-static (QS) C-V measurements, with scan rate of 0.1 V/s, were made on the Al/Al$_2$O$_3$/n-InAs MOS capacitors, using the Agilent 4155C semiconductor parameter analyzer, to estimate the dielectric constant of the ALD Al$_2$O$_3$ films. All the measurements were made in dark and grounded back contact through the chuck of the probe station. Since post growth annealing increased the leakage current in the Al$_2$O$_3$/InAs structures, only nonannealed films were measured. Figure 3.15(a) and (b) show double-scan QS C-V measurements of 8.6 and 5 nm Al/Al$_2$O$_3$/n-InAs MOS capacitors, respectively, against computed C-V curves simulated using Bandprof.
In the simulated C-V, parameters of Al₂O₃ are taken from Table 1.4, which shows a dielectric constant of 9 [40] and conduction offset to InAs and Si of 3.6 and 2.6 eV [41], respectively. The barrier height between Al contact and Al₂O₃ is taken to be 3.1 eV, which is the average between experimental value, 2.9 eV, from [67] and theoretical value 3.3 eV from [68].

Dielectric constants estimated from measured electron accumulation capacitances are 6.0 and 6.1 for 8.6 nm and 5 nm films, respectively. The values are relatively low, which is noticeable when comparing the experimental C-V curves to the computed solid curves in Figure 3.15. Both QS C-V plots in Figure 3.15 fail to show the inversion of the n-InAs surface. This is an indication of high density of defects at the InAs/Al₂O₃ interface, or slow traps in the Al₂O₃ layer.

![Figure 3.15 Quasi-static double-scan C-V measurements of MOS diode formed by (a) 5 and (b) 8.6 nm ALD Al₂O₃ films on n-InAs, with 150 µm diameter Al contacts. The solid curves simulate ideal Al/Al₂O₃/nInAs MOS capacitor using BandProf³.](image)

However, one factor should be included into the estimation of Al₂O₃ film dielectric constant on an n-InAs substrate, which is that the maximum capacitance does
not happen in the electron accumulation region. The simulated ideal $C$-$V$ curves in Figure 3.15 show highest capacitance is reached in the hole inversion region. This is resulted from InAs has higher DOS of holes, $6.6 \times 10^9$/cm$^3$ in the valence band than that of electron in the conduction band, $8.7 \times 10^6$/cm$^3$. In Si, DOS of electrons and holes are close, $3.2 \times 10^{19}$/cm$^3$ and $1.8 \times 10^{19}$/cm$^3$, the simulated $C$-$V$ in Figure 3.16 shows better symmetry. Figure 3.16 shows the simulated and measured QS $C$-$V$ of the Al/(8 nm)Al$_2$O$_3$/p–Si MOS control capacitor. The measured $C$-$V$ shows clear electron inversion. Both the simulated and measured curves are more symmetric compared to those in Figure 3.15. Dielectric constant, calculated using the electron inversion capacitance, is 6.6, which is also lower than the bulk value $9 \ [40]$.

![Figure 3.16 Quasi-static double-scan C-V measurements of Al/(8.3 nm)Al$_2$O$_3$/p-Si MOS diode with Al$_2$O$_3$ film deposited using ALD. The solid curves simulate the ideal Al/Al$_2$O$_3$/p-Si MOS capacitor using BandProf$^3$.](image)

Since Figure 3.16 shows that the ALD Al$_2$O$_3$/p-Si can invert, the oxide alone is not the reason for the lack of inversion in the QS $C$-$V$ curves of the Al/Al$_2$O$_3$/n-InAs MOS capacitor in Figure 3.15. The reasons must originate from the InAs/Al$_2$O$_3$ interface.
Traps at the interface between the InAs and Al$_2$O$_3$ can hold the Fermi level pinned throughout the $\geq 3$ V bias and 0.1 V/s scan rate. The interface traps could be located in a native oxide of InAs, In$_2$O$_3$ and As$_2$O$_3$ which form in the 3 minutes between NH$_4$OH (29%) solution surface treatment followed by DI water rinsing clean and loading into the ALD chamber. It has been demonstrated by removing or reduce native oxides on the III–V material surface that the density of interface defects at insulator/III-V interface can be reduced and electrical performance, $I$-$V$ and $C$-$V$, enhanced [46] [47] [78] [83]. It should be pointed out that high interface defect density may also originate from defects, such as nonstoichiometry and antisite defects in the surface region of the semiconductor which are commonly seen in MOS on III–V's even after the removal of native oxides [46]. Although $p$-Si surface is able to invert, the $C$-$V$ curves still have less steep slope compared to the simulated curve, indicating the Al$_2$O$_3$ and Si interface are not free of interfacial traps.

3.2.3 Conclusions on ALD Al$_2$O$_3$

Atomic layer deposition of Al$_2$O$_3$ films have been carried out at a rate of $\sim$1 Å/cycle. Ultra thin films of 3, 5 and 8 nm, have been deposited onto $p$-Si and $n$-InAs substrates at 200 °C and subsequently annealed at 250, 300 and 350 °C. Annealing does not affect physical properties, thickness, surface roughness, and refractive index, of the ALD films. However, annealing does increase the leakage current of the ALD films by 10 times for 5 and 8.6 nm films and 4 orders of magnitude for 3 nm films, but does not appear effect breakdown voltage.
The lowest leakage current at 1 MV/cm of $\sim 10^{-9}$ A/cm$^2$, and highest breakdown electric field $\sim 10$ MV/cm, comparable to prior reports [52], are observed the 8.6 nm thick film. Dielectric constant obtained from QS C-V measurements is not lower than 6.1, comparable to previous measurements [52].

The $n$-InAs surface does not invert in QS C-V measurements of Al/Al$_2$O$_3/n$-InAs MOS capacitor, while the $p$-Si control surface did. The lack of inversion indicates high interface defects density between the InAs and Al$_2$O$_3$ despite the 3 minutes (29%) NH$_4$(OH)$_3$ surface treatment.

3.3 Summary

In this chapter, electron-beam-enabled PVD and ALD deposition of Al$_2$O$_3$ on InAs and Si were explored. Both PVD and ALD Al$_2$O$_3$ have been characterized physically and electrically. Both PVD and ALD films in Si MOS capacitors show inversion. Although no PVD films have been deposited on InAs substrates, ALD films on $n$-InAs have been characterized, however ALD Al/Al$_2$O$_3/n$-InAs did not invert, indicating further improvements are needed for the surface treatment at the interface. In the next chapter, PVD film were used in the formation of InAs-on-SOI extreme lattice mismatched MOSFETs.
Chapter 4

Characterization of InAs-on-SOI MOSFETs with Extreme Lattice Mismatch

Using PVD Al$_2$O$_3$ as the gate dielectric, MOSFETs with InAs-on-SOI extreme-lattice-mismatched channels were fabricated. Drain current characteristics and transconductance of the MOSFETs were measured. Gate recess etching was used to thin the InAs and improve gate control of the channel current.

4.1 InAs/Si MOSFETs Fabrication

The device fabrication process was outlined in Figure 1.11. Figure 4.1 shows the top view SEM images, from formation of submicron Si template to final completion of an InAs/Si MOSFET with source/drain and gate terminals. The fabrication of the InAs/Si MOSFET start with thinning of SOI from 50 nm to less than 10 nm and etching to form submicron Si islands as the template for the growth of InAs. Figure 4.1(a) is a Si island of size $0.4 \times 2 \mu m^2$ formed using RIE with FOx-12 as the etch mask. Figure 4.1(b) shows the growth results of MOCVD InAs on the patterned SOI substrate, which confirmed the observations that MOCVD growths result in InAs with granular structures on Si islands larger than $100 \times 100 \text{ nm}^2$. The InAs layer on Si appears to be coalesced InAs grains. The location of the Si island is indicated by the dashed lines in Figure 4.1(b) – (d), showing the InAs layer is $\sim 200 \text{ nm}$ wider. The thickness of the InAs film as measured using AFM is found to be $120 \pm 30 \text{ nm}$. After patterning, the source and drain contacts were
deposited, Figure 4.1(c). The final fabrication step was to deposit the Al₂O₃/Ti/Pt/Au gate stack in a single e-beam evaporation process, Figure 4.1(d).

(a) Si mesa on SOI, 0.4 × 2 µm

(b) MOCVD InAs grown on a 0.4 × 2 µm Si mesa

(c) InAs/Si MOSFETs with metal source and drain contacts

(d) A complete InAs/Si MOSFET with all three terminals

Figure 4.1 Construction of an InAs/Si on SOI MOSFET viewed by SEM. The boxes in (b), (c), and (d) outline the actual size of the Si mesa with InAs grown by MOCVD.
4.2 DC characteristics

Figure 4.2 shows common-source characteristics from three different devices with similar source and drain spacing, $\sim 0.7 \, \mu \text{m}$, at $0.5 \, V \, V_{DS}$ at zero gate-to-source bias. Measurements were performed using an Agilent 4155 semiconductor parameter analyzer on a Cascade Microtech 11861 probe station. These three devices were from the same substrate and within a $4.5 \times 6 \, \text{mm}^2$ area. The difference of the current densities in Figure 4.2 results from the nonuniform resistance of the InAs film on SOI.

![Figure 4.2 Drain current measured from three different devices with similar source and drain spacing, showing the nonuniform resistance of MOCVD InAs-on-SOI.](image)

4.2.1 Channel recess

Figure 4.3 shows the common source characteristics of an InAs/Si MOSFET. The SEM image shows the exact measured device, which has source-to-gate spacing of less than 25 nm. The measured device width is $\sim 600 \, \text{nm}$, gate length, $\sim 500 \, \text{nm}$, source to drain spacing, $\sim 700 \, \text{nm}$, which are measured from the SEM image. The drain current density is as high as 430 mA/mm at a drain bias, $V_{DS}$, of 0.5 V and gate bias, $V_{GS}$, 3 V.
However, the drain current cannot be completely turned off, even with $V_{GS} = -3$ V bias. The non-pinching off drain current of the device is not caused by the gate leakage current, which is much lower than the drain current at same bias conditions, Figure 4.3.

Figure 4.3 Common-source characteristics of an InAs/Si MOSFET with 15 nm PVD Al$_2$O$_3$ as the gate dielectric. The inset is the SEM image of the device measured, showing the dimension of the device. Notice the channel cannot be completely turned off.

The reason that the gate does not have much control over the channel conductance could result from the thick InAs layer, $\sim 120 \pm 30$ nm, which cannot be completely depleted. It has been reported that polycrystalline InAs grown by different methods has high carrier concentration, range from $10^{17}$ to even $10^{19}$ cm$^{-3}$ [84] [85] [86]. Assuming an InAs $n$-doping of $1 \times 10^{18}$ cm$^{-3}$, an Al$_2$O$_3$ dielectric constant of 8.1, a Ti/Al$_2$O$_3$ barrier of 3.3 eV,
and an $\text{Al}_2\text{O}_3$/InAs conduction offset of 3.6 eV, the band diagram of the device in Figure 4.4 (b) is simulated, using BandProf, plotted in Figure 4.4 (a).

![Band diagram of the device with Al$_2$O$_3$/InAs conduction offset of 3.6 eV.](image)

**Figure 4.4 (a)** Energy band diagram, simulated using BandProf, shows the thick, 120 nm, InAs channel. Drawing in (b) shows the corresponding layer structure simulated in (a), with all the layers under the gate drawn to scale.

It is apparent, from the band diagram simulated in Figure 4.4(a), that the channel current should be dominated by conduction in the InAs. Further simulations show that when Fermi level between $\text{Al}_2\text{O}_3$ and InAs is not pinned, device of thinner or less doped InAs channel can have better control of the channel charge, hence improved $I_{\text{ON}}/I_{\text{OFF}}$ ratio. Reducing InAs thickness from 120 to 20 nm, the channel sheet charge ratio increases, at $I_{\text{ON}}$ and $I_{\text{OFF}}$, from 2 to $5 \times 10^4$ for the InAs channel with electron concentration of $1 \times 10^{18}/\text{cm}^3$, Figure 4.5(a) and from 20 to $2 \times 10^6$ for $1 \times 10^{17}/\text{cm}^3$ Figure 4.5(b).
Figure 4.5 Simulated electron concentration in the InAs layer with changing gate bias and thickness and doping concentration (a) $1 \times 10^{18}$ cm$^{-3}$ and (b) $1 \times 10^{17}$ cm$^{-3}$ using BandProf, showing improve charge control of the channel when the InAs layer thickness or doping concentration is reduced.

The channel thickness can be reduced by channel recess etching before the gate stack deposition to improve gate control. This can be realized by a controlled etching before the gate deposition, Figure 4.6.

Figure 4.6 Schematic drawing of channel recess process, showing the exposed channel being thinned down.

Before the deposition of the top gate stack, the exposed InAs is etched in acetic-acid-based solution (1 acetic: 2 peroxide: 20 H$_2$O). Etch depth is controlled by probing through the resist covering source and drain contact and assuming the channel current
reduction is proportional to the thickness reduction. Figure 4.7(a) compares the common source characteristics of a device before and after 45 s etching. The measurement is realized by back-gate biasing using the substrate connection. Although the reduction of the drain current is achieved, the channel is not gated off. Figure 4.7(b) shows the common source measurement of the same device using the top gate. The device parameter of the recessed-channel device is: Al$_2$O$_3$ thickness, ~15 nm, gate length, ~500 nm, source and drain contacts spacing, ~700 nm.

Figure 4.7 Common source characteristics (a) through the SOI substrate backgate, showing the reduction of channel current due to gate recess etching of InAs, and (b) the same channel-recessed InAs/Si MOSFET controlled with 15 nm PVD Al$_2$O$_3$ as gate dielectric.

Comparing the drain current at 50 V and -50 V gate bias, in Figure 4.7(a), the drain current density at 0 back gate bias reduced from 275 to 80 mA/mm, and the ratio, $I_D(V_{GS} = 50 \, \text{V})/I_D(V_{GS} = -50 \, \text{V})$, improved from 1.45 to 2.36. But showing in Figure 4.7,
both back-gated and top-gated measurements, even with channel recessed to about 25% of original current density, the InAs/Si channel still cannot be turned off. It indicates more mechanisms are involved in generating drain current other than charge the channel. One of the mechanisms for lack of gate control could be that the Fermi level at the InAs/Al$_2$O$_3$ interface is pinned. The surface Fermi level of air exposed or metal-contacted InAs is pinned ~0.15 eV above conduction band of InAs [87], which can contribute about $10^{18}$ cm$^{-3}$ of carriers under the InAs surfaces.

The PVD MOS capacitor, 30 nm Al$_2$O$_3$ on n-Si, presented in Chapter 3 shows constant capacitance through -4 to 4 V bias, indicating the lack of charge control at the oxide and semiconductor interface resulted from high density of interface traps. It is intriguing that the channel conductance can be modulated through PVD oxide as shown in Figure 4.7(b). The control of channel charge can be regained if the interface traps are filled by the gate leakage current. However, following Passlack [88], the effect of the gate leakage current is shown to be insufficient on filling interface traps. Mechanisms other than gate leakage, involved in filling the interface trap, are required for explaining the channel charge control through the PVD Al$_2$O$_3$.

4.2.2 Gate leakage current

Figure 4.8 shows gate leakage current of two different thicknesses Al$_2$O$_3$, 7.5 and 15 nm. Both of them have higher leakage current than the film characterized in the previous chapter, which is in the order of $10^{-8}$ A/cm$^2$ at an electric field of 0.33 MV/cm. The increase of the leakage current could be caused by the deposition of Al$_2$O$_3$ onto grainy structures of InAs surfaces, which have been observed regularly in the SEM. The
uneven surfaces of InAs layer might cause the Al₂O₃ coated unevenly, which could become a leakage path under bias. The interesting observation is that the thicker oxide seems to have higher leakage current, Figure 4.8 (b), than film half of its thickness, Figure 4.8 (a), for these two particular devices. However, the gate leakage current of device in Figure 4.8 (b) is still close to three orders of magnitude lower than the drain current measured, \( I_G = 0.27 \mu A \) compared to \( I_D = 242 \mu A \) at \( V_{DS} = 0.5 \) and \( V_{GS} = -2 \) V. For the device in Figure 4.8 (a), the drain current is 71 \( \mu A \), and gate leakage \( 5.2 \times 10^{-4} \) \( \mu A \) at \( V_{DS} = 0.5 \) and \( V_{GS} = -2 \) V, which gives a more than five orders of magnitude difference between \( I_D \) and \( I_G \). The gate leakage current is small enough not to contribute to drain current in the transistor common source and transconductance characteristics.

![Figure 4.8 Gate leakage current of two devices with (a) 7.5 and (b) 15 nm Al₂O₃.](image)

4.3 Conclusions

MOSFETs with MOCVD grown InAs-on-SOI were fabricated. High-\( k \) dielectric, Al₂O₃, is incorporated as a gate dielectric. Due to the thick InAs, 120 ± 30 nm, layer, the pinch-off of the drain current could not be demonstrated in the common source device
characteristics. By recessing the channel area before the gate stack deposition, the drain current ratio, $I_D(V_{GS} = 3V)/I_D(V_{GS} = -3 V)$, improved from 1.45 to 2.36, but pinch-off still could not be reached.
Chapter 5

Conclusions and Recommendations for Further Study

This dissertation shows the results of an exploration of the growth and characterization of highly-mismatched InAs-on-Si thin films on SOI for MOSFET applications. Planar InAs, as observed by SEM, has been formed using both MBE and MOCVD on patterned submicron SOI islands. High-\(k\) dielectric Al\(_2\)O\(_3\) films, deposited using both PVD and ALD, have been characterized physically and electrically. MOSFETs with MOCVD InAs-on-SOI channels have been fabricated with PVD Al\(_2\)O\(_3\) as the gate dielectric and characterized by \(I-V\) measurements. This chapter summarizes the work presented and suggests the directions for future research.

5.1 Summary

Both MBE and MOCVD have been used to grow InAs in the thickness range from 100 – 10 nm, onto patterned SOI substrates. Silicon pattern size and growth temperature have been investigated and shown to effect the growth of the InAs. Despite 11.6\% lattice mismatch, planar InAs structures have been obtained using MBE at 250 °C on Si island sizes as large as 500 × 500 nm\(^2\) and lines of width 100 nm and lengths of microns. MOCVD growth of InAs has been observed to generate single grain structures on Si island sizes of 100 × 100 nm\(^2\) at 450 °C. With SOI as the growth template, selective growth is achieved by MOCVD at both 400 and 450 °C.
A post-growth pattern-then-anneal process was explored on MOCVD InAs-on-SOI. In encapsulated InAs-on-SOI structures, the lattice parameters of InAs are changed upon annealing. The relative thickness between InAs and Si is shown to be a factor in the annealing results. Transmission electron diffraction patterns shows a relative lattice mismatch change from 11.2% to 4.2% on a 17/5 nm InAs/Si structure after being annealed at 800 °C for 30 minutes. High-$k$ dielectrics Al$_2$O$_3$ have been deposited with both e-beam enabled PVD and ALD processes. MOS capacitors were fabricated for the electrical characterization of the Al$_2$O$_3$ films. Both PVD and ALD methods have been found to produce Al$_2$O$_3$ films with leakage current in the order of $10^{-9}$ A/cm$^2$ at 1 MV/cm, breakdown field $\sim$6 MV/cm, and dielectric constant 7.1 ± 0.1 (PVD) and 6.3 ± 0.3 (ALD). Both PVD and ALD Al$_2$O$_3$–Si MOS capacitors show inversion of Si in low frequency, quasi-static (ALD) to 1 - 10 kHz (PVD), C-V measurements, while ALD Al$_2$O$_3$-InAs MOS capacitors fail to invert. The lack of inversion at the ALD Al$_2$O$_3$-InAs interface indicates a high density of interfacial states.

Ultrathin ALD Al$_2$O$_3$ films, less than 10 nm, on InAs have been deposited and characterized for the first time. Post growth annealing at temperatures higher than the growth temperature has been studied. Annealing does not affect the thickness, surface morphology and refractive index of ALD Al$_2$O$_3$ films. Annealing also does not affect the breakdown field of the film, but does increase the leakage current of the ALD films by 10 times for 5 and 8.6 nm films and 4 orders of magnitude for 3 nm films Al$_2$O$_3$ films.

MOSFETs with InAs-on-SOI channels are made by integrating MOCVD InAs with PVD Al$_2$O$_3$. However characterization shows devices cannot be pinched off due to the thickness of the InAs layer, 120 ± 30 nm.
5.2 Suggestions for future studies

The growth results shown in the dissertation have been performed on (100) SOI, however, a (211) crystal orientation is preferred for growing polargroup III-V compounds, on non-polar ones, group IV [26] to avoid the formation of antiphase domains [24]. Prada’s simulation of InAs-Si composite material reports the possibility of engineering electronic properties, energy bandgap and DOS effective mass, of (211) InAs-Si structures [22]. Future material growth should be explored on (211) orientation.

As shown by Prada [22], combining two ultra thin layers of group IV and III-V compounds, new materials with new properties could be created and have possible superior electronic properties. More new composite material systems, e.g. InAs/Ge, InSb/Si, and InSb/Ge, can be the candidates under investigation. The lower lattice mismatch, 7.1%, between InAs and Ge will make epitaxial growth of InAs on less challenging compared to growth on Si. Although the lattice mismatches of InSb/Si and InSb/Ge are 19.3% and 14.5%, the electron mobility in InSb is 77,000 cm²/V·s compared to 30,000 cm²/V·s. Using InSb as the group III-V component in the III-V/IV structures could form composite channels superior to InAs-based ones.
APPENDIX A

Processing Procedure for MOCVD InAs-on-Si MOSFET with extreme lattice mismatch

Device Fabrication Outline:

1. thin down SOI Si layer to less than 10 nm by oxidation and BOE etching
2. deposit Ti/Pt/Si EBL alignment marks
3. form sub micron Si structures
4. grow InAs using MOCVD
5. deposit Ti/Au source and drain bonding pads to form S/D contacts
6. etch away poly InAs on the BOX if electrical data suggests necessary
7. deposit top gate stack, AlOx/Ti/Pt/Au

1. Thin Down SOI Si Layer to 10 nm by Oxidation and BHF Etching
   - RCA clean BOX1
   - RCA1 (DI: NH₄OH: H₂O₂=40-50:1:1) bath, 70 ºC, 10 min, Spray dunk rinse
   - RCA2 (HCl: H₂O₂:DI=40-50:1:1) bath, 70 ºC, 10 min, Spray dunk rinse
   - Etch in 1HF: 50DI for 30 s
   - Rinse in DI for 20 s
   - Load the substrate to Tube 2 and dry oxidize at 1000 ºC for 90 min
   - The final Si layer thickness measured by VASE⁴ is 10 ± 2 nm

2. Ti/Pt/Si EBL Alignment Marks Deposition

Solvent Clean
   - Soak in hot acetone (boiling point 56.5 ºC) hot plate 60 ºC, 2 min
   - Soak in hot methanol (flash point 64.7 ºC) hot plate 60 ºC, 2 min
   - Rinse in DI 2 min and blow dry with N₂
   - UV Ozone⁵, 10 psi, 60 s

⁴ Variable-angle spectral ellipsometry, J. A. Woolam Co., Inc. VB-250 (spectral range: 240 – 1700 nm)
⁵ Jelight UV Ozone Model 144AX with 99.999% O₂ purity
MicroChem MMA/PMMA Positive Resist

- Note expiration dates to make sure resists are up to date
  - MMA(8.5) MAA EL6
  - 950 PMMA C2
- Set hotplate temps. to 150 °C and 180 °C
- Load sample on spinner
- Using a glass pipette and dispense MMA onto wafer to coat surface
- Spin 1000 rpm, 90 s (expect ~2500 Å thick layer)
- Hot plate bake 150 °C, 75 s on Al lollypop
- Load sample back on spinner
- Using a glass pipette, dispense PMMA onto wafer to coat surface
- Spin 4000 rpm, 45 s (expect ~1250 Å thick layer)
- Bake 180 °C, 75 s
- Expect total resist thickness of 3750 Å

Electron-Beam Lithography Elionix ELS-7700, 75 keV

- Compute e-beam write time using Excel workbook below
  - Aperture 2, Spot size 8 nm

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<thead>
<tr>
<th>Settings</th>
<th>Calculations</th>
</tr>
</thead>
<tbody>
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<td>B</td>
<td>12</td>
</tr>
<tr>
<td>C</td>
<td>12</td>
</tr>
<tr>
<td>D</td>
<td>12</td>
</tr>
</tbody>
</table>

- Expose each piece separately
- Record actual write time ____ min
- Record CON filenames:
- Record SCH filename:
- Develop wafers in AZ MIF 917⁷, 30 s
- Rinse in DI, 60 s and blow dry in N₂
- Microscope inspect to determine if more develop time is needed
- Develop as needed, record total develop time for each piece

Ti/Pt/Si Alignment Marks Deposition and Lift-off

- Pump chamber to < 2 x 10⁻⁶ Torr, record final pressure Torr
- Deposit Ti/Pt/Si (200 Å /850/250 Å) at ~ 5/8/5 Å/s

---

⁶ PMMA, polymethyl methacrylate, C₃H₆O₂; MMA, methyl mannose, C₇H₁₄O₆; MAA, methylarsonic acid, CH₅AsO₃; ⁷ metal ion free, AZ 917 MIF
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<td>Density (g/cm$^3$)</td>
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<tr>
<td>Z-ratio</td>
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<td>Rate (Å/s)</td>
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</table>

- Prepare hot acetone (boiling point 56.5 ºC) hot plate 60 ºC
- Vent and unload wafers
- Soak in hot acetone (boiling point 56.5 ºC) hot plate 60 ºC, 2 min
- Acetone spray ___ min to complete lift-off
- Bottle rinse methanol, 20 s
- Blow dry N$_2$
- Microscope inspect and note cleanliness and alignment marks definition

3. **Submicron Si Island Formation**

Solvent Clean SOI wafers (if left over night)

- Soak in hot acetone (boiling point 56.5 ºC) hot plate 60 ºC, 2 min
- Soak in hot methanol (flash point 64.7 ºC) hot plate 60 ºC, 2 min
- Rinse in DI 2 min and blow dry with N$_2$
- UV Ozone, 10 psi, 60 s

**Negative Resist process using Dow Corning FOX-12**

- Ensure FOX-12 has reached room temperature
- Using a plastic pipette to dispense FOX-12 onto sample
- Spin 4000 rpm, 30 s Record time to color change ____ s
  - Expect ~1400 Å thickness
- Bake samples at 200 ºC for 4 min

**Electron-Beam Lithography Elionix ELS-7700, 75 keV**

- Compute e-beam write time using Excel workbook below
  Aperture 2, Spot size 8 nm

---

8 flowable oxide containing HSQ, hydrogensilsesquioxane, HSiO$_{3/2}$
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<thead>
<tr>
<th>Settings</th>
<th>Calculations</th>
</tr>
</thead>
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<tr>
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<tr>
<td>B 9 157 500 800 300 60000 5 0.4 0.4</td>
<td></td>
</tr>
<tr>
<td>C 9 157 500 800 300 60000 5 0.4 0.4</td>
<td></td>
</tr>
<tr>
<td>D 9 157 500 800 300 60000 5 0.4 0.4</td>
<td></td>
</tr>
</tbody>
</table>

- Expose each piece separately
- Record actual write time ____ min
- Record CON filenames:
- Record SCH filename:
- Develop wafers in AZ MIF 917⁹, 30 s
- Rinse in DI, 60 s and blow dry in N₂
- Microscope inspect to determine if more develop time is needed
- Develop as needed, record total develop time for each piece

SOI Island Etching in Alcatel 601E Inductively-Coupled Plasma (ICP) Etcher

Solvent Clean (if left overnight)

- Soak in hot acetone (boiling point 56.5 °C) hot plate 60 °C, 3 min
- Soak in hot methanol (boiling point 64.7 °C) hot plate 60 °C, 3 min
- Rinse in DI 2 min

Etching

- Mount samples on 4” wafer with painted photoresist
- Bake 120 °C, 2 min
- Load into Alcatel without delay
  - Settings: SF₆:O₂, 40:5 sccm, RF1: 100 W, RF2: 80-100 W, 100 mTorr, 120 °C
  - DC bias: 70-80 V
  - Etch rate 100-120 nm/min, 1:20 selectivity (PECVD¹⁰ SiO₂:Si)
- Compute etch time for an overetch factor of 150% for 10 nm of Si (include 10 s of delay), estimated etch time 22 s
- ICP etch ____ s
- Record DC bias ____ V
- Microscope inspect – is there visible evidence of etching?

4. InAs Growth Using MOCVD

Package samples out to Wisconsin

---

⁹ metal ion free, AZ 917 MIF
¹⁰ Plasma-enhanced chemical vapor deposition
Growth Conditions:

Remove Fox-12 from control sample

- Take SEM images of islands before HSQ removal
- Keep BOE\textsuperscript{11} etch time under 50 s to avoid SOI undercut
  \((\text{SiO}_2\text{ etch rate } 1 \text{ nm/s})\) \((\text{HSQ etch rate } > 15 \text{ nm/s})\)
- Rinse in DI 1 min
- Etch in BOE 15 s
- Rinse in DI 1 min
- Take SEM images of islands after HSQ removal to ensure all HSQ has been removed

**Alpha-Step SOI mesa after FOX-12 removal**

- Record height and surface roughness

Physical Characterization of Pilot Sample BSOI\textsubscript{10}

- SEM\textsuperscript{12} inspect and document SOI morphology and surface cleanliness prior to growth
- AFM\textsuperscript{13} characterize islands prior to MBE growth

**5. Ti/Au Source/Drain Contacts Deposition**

Physical Characterization Prior to S/D Deposition

- SEM inspect and document morphology of samples
- AFM characterize islands
- Cleave an edge of each sample for TEM characterization

Solvent Clean

- Soak in hot acetone (boiling point 56.5 °C) hot plate 60 °C, 3 min
- Soak in hot methanol (boiling point 64.7 °C) hot plate 60 °C, 3 min
- Rinse in DI 2 min

MicroChem MMA/PMMA Positive Resist

- Note expiration dates to make sure resists are up to date
  - MMA(8.5) MAA EL6

\textsuperscript{11} J. T. Baker buffered oxide etch (10:1), product code 5175
\textsuperscript{12} Hitachi S-4500
\textsuperscript{13} Nanoscope IV AFM/MFM
950 PMMA C2
- Set hotplate temps. to 150 °C and 180 °C
- Using glass pipettes
- Spin on MMA at 1000 rpm for 90 s (expect ~2500 Å thick layer)
- Bake at 150 °C for 75 s
- Spin on PMMA at 4000 rpm for 45 s (expect ~1250 Å thick layer)
- Bake at 180 °C for 75 s

Electron-Beam Lithography Elionix ELS-7700, 75 keV
- Use aperture 3
- Write the Si pilot BSOI7 as a control
- Compute e-beam write time using Excel workbook below

Aperture 3, Spot size __ nm

<table>
<thead>
<tr>
<th>Settings</th>
<th>Calculations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer Loc.</td>
<td># of Die</td>
</tr>
<tr>
<td>9</td>
<td>40000</td>
</tr>
<tr>
<td>9</td>
<td>40000</td>
</tr>
<tr>
<td>9</td>
<td>40000</td>
</tr>
</tbody>
</table>

- Record actual write time ____ min
- Record CON filename:
- Develop wafers separately in 1MIBK: 3IPA: 1.5% MEK solution for 30 s
- Bottle rinse in IPA 20 s
- Blow dry in nitrogen
- Microscope inspect to determine if more develop time is needed
- Develop as needed, record total develop time for each piece
- Ready evaporator
- UV Ozone clean 60 s, inlet O₂ pressure ____ psi

Ti/Au S/D Contacts Deposition and Lift-off
- Pump chamber to < 2 x 10⁻⁶ Torr, record final pressure ____ Torr
• Deposit Ti/Au (150 Å / 1700 Å) at ~ 5/8 (Å) / s

<table>
<thead>
<tr>
<th>Evaporation parameters</th>
<th>Beam parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal</td>
<td>Ti</td>
</tr>
<tr>
<td>Tooling (U-bar)</td>
<td>Density (g/cm³)</td>
</tr>
<tr>
<td></td>
<td>Z-ratio</td>
</tr>
<tr>
<td></td>
<td>Rate (Å/s)</td>
</tr>
<tr>
<td></td>
<td>Thickness (Å)</td>
</tr>
</tbody>
</table>

• Transfer wafers into hot acetone
• Soak in acetone 5 min (actual soak time _____ min)
• Acetone spray ___ min to complete lift-off
• Bottle rinse IPA, 20 s
• Blow dry N₂
• Inspect under microscope

Measurements Before Further Processing

• Test the isolation between adjacent pads to decide if InAs isolation etch is required
• Test the back gated transistor I-V
• Using test structures to measure InAs/Si composite layer resistivity and contact resistance.

6. Top Gate Stack, Al₂O₃/Ti/Pt/Au, Deposition

Solvent Clean

• Soak in hot acetone (boiling point 56.5 º C) hot plate 60 º C, 3 min
• Soak in hot methanol (boiling point 64.7 º C) hot plate 60 º C, 3 min
• Rinse in DI 2 min

MicroChem MMA/PMMA Positive Resist

• Note expiration dates to make sure resists are up to date
  o MMA(8.5) MAA EL6
  o 950 PMMA C2
• Set hotplate temps. to 150 º C and 180 º C
• Using glass pipettes
• Spin on MMA at 1000 rpm for 90 s (expect ~2500 Å thick layer)
• Bake at 150 º C for 75 s
• Spin on PMMA at 4000 rpm for 45 s (expect ~1250 Å thick layer)
• Bake at 180 º C for 75 s
Electron-Beam Lithography Elionix ELS-7700, 75 keV

- Use aperture 3
- Write the Si pilot BSOI7 as a control
- Compute e-beam write time using Excel workbook below
  Aperture 3, Spot size ___ nm

<table>
<thead>
<tr>
<th>Wafer Loc.</th>
<th>Die</th>
<th>Pattern Area (μm²)</th>
<th>Beam I (pA)</th>
<th>Dose μC/cm²</th>
<th>Chip Size (μm)</th>
<th>Dot space</th>
<th>Time (μs/dot)</th>
<th>Write (min.)</th>
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</thead>
<tbody>
<tr>
<td>9</td>
<td>20000</td>
<td>2500 400</td>
<td>300</td>
<td>240000</td>
<td>1.25</td>
<td>0.003</td>
<td>4.8</td>
<td></td>
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<tr>
<td>9</td>
<td>20000</td>
<td>2500 400</td>
<td>300</td>
<td>240000</td>
<td>1.25</td>
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<tr>
<td>9</td>
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<td>240000</td>
<td>1.25</td>
<td>0.003</td>
<td>4.8</td>
<td></td>
</tr>
</tbody>
</table>

- Record actual write time ____ min
- Record CON filename:
- Develop wafers separately in 1MIBK: 3IPA: 1.5%MEK solution for 30 s
- Bottle rinse in IPA 20 s
- Blow dry in nitrogen
- Microscope inspect to determine if more develop time is needed
- Develop as needed, record total develop time for each piece
- Ready evaporator
- UV Ozone clean 60 s, inlet O₂ pressure ____ psi

Top Gate Stack, Al₂O₃/Ti/Pt/Au, Deposition and Lift-off

- Pump chamber to about 5 x 10⁻⁷ Torr, record final base pressure ____ Torr
- Open the valves to through O₂, set pressure to be 5 x 10⁻⁵ Torr
- Deposit 8 nm Al₂O₃ using (deposition rate 1 Å/s)
  Record actual chamber pressure ____ Torr
- Deposit Ti/Pt/Au 15/20/150 nm

<table>
<thead>
<tr>
<th>Metal</th>
<th>Al₂O₃</th>
<th>Ti</th>
<th>Pt</th>
<th>Au</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tooling</td>
<td>82</td>
<td>82</td>
<td>82</td>
<td>82</td>
</tr>
<tr>
<td>Density (g/cm³)</td>
<td>3.97</td>
<td>4.5</td>
<td>21.4</td>
<td>19.3</td>
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<tr>
<td>Z-ratio</td>
<td>0.336</td>
<td>0.628</td>
<td>0.245</td>
<td>0.381</td>
</tr>
<tr>
<td>Rate (Å/s)</td>
<td>1</td>
<td>5</td>
<td>7</td>
<td>8</td>
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<tr>
<td>Thickness (Å)</td>
<td>100</td>
<td>700</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Beam parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃</td>
</tr>
<tr>
<td>V (kV)</td>
</tr>
<tr>
<td>2.45/3.6</td>
</tr>
</tbody>
</table>

- Soak in acetone 5 min (actual soak time ____ min)
- Acetone spray ____ min to complete lift-off
- Bottle rinse IPA, 20 s
- Blow dry N₂
- Inspect under microscope
APPENDIX B

Conference abstracts

Abstracts from the following conference poster and presentation are presented in this appendix:

“Current-Voltage Measurements and Photoconductance Spectroscopy of Ultrathin InAs Grown on (211) Si,” 2007 Material Research Society Spring Meeting, Poster;

“InAs Growth On Submicron (100) SOI Islands for InAs-Si Composite Channel MOSFETs,” 2007 International Semiconductor Device Research Symposium, Presentation.
Current-Voltage Measurements and Photoconductance Spectroscopy of Ultrathin InAs Grown on (211) Si

Bin Wu\textsuperscript{1}, Dane Wheeler\textsuperscript{1}, Qin Zhang\textsuperscript{1}, Patrick Fay\textsuperscript{1}, Alan Seabaugh\textsuperscript{1}, Changhyun Yi\textsuperscript{2}, Inho Yoon\textsuperscript{2}, April Brown\textsuperscript{2}, Thomas Kuech\textsuperscript{3}

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\textsuperscript{2}Department of Electrical and Computer Engineering, Duke University, Durham, NC.
\textsuperscript{3}Department of Chemical and Biological Engineering, University of Wisconsin, Madison, WI.

ABSTRACT

An approach for forming InAs-channel MOSFETs is being explored in which sub-10-nm thick InAs is grown directly on Si (211) and (100) substrates. These thin channels are capped with a high-k dielectric consisting of evaporated aluminum oxide. The (211) orientation is selected to provide a charge neutral growth plane and circumvent the formation of antiphase domains. The growth is by molecular beam epitaxy (MBE) using growth temperatures at 300 °C. Post-growth annealing is being explored to improve the crystallinity. Four probe device structure has been designed to explore transport in InAs on Si channels. Current-voltage measurements, normal to the growth plane, of Al/Ti/10 nm InAs/p-Si devices show diode characteristics, consistent with the formation of n-InAs/p-Si diodes. Scanning electron microscopy of these first films reveal the formation of islands with an island size ranging from 5 to 25 nm in extent. Current-voltage measurements in the plane is also explored to understand the transport in the 10 nm InAs film. Photoconductance measurements are being used to further unravel the transport in these films.

INTRODUCTION

The debate on transferring III-V compound semiconductors onto Si substrate has attracted lots of attention. The reason to integrate III-V materials with Si is to provide FETs with high-electron-mobility channels. Among all the binary III-V semiconductor materials, InAs, with a room temperature high electron mobility of 33,000 cm\textsuperscript{2}/Vs at 300 K is particularly attractive as a channel material for field-effect transistors (FETs). This electron mobility is almost three times higher than in GaAs, and more than twenty times higher than in Si. The electron peak velocity of $4.3 \times 10^7$ cm/s at 77 K [1] in InAs is twice that of GaAs and four times the electron saturation velocity of Si. Moreover this peak velocity in InAs appears at an electric field of 2 kV/cm, amongst the lowest of any semiconductor [1] [2].

InAs [3] and In\textsubscript{0.53}Ga\textsubscript{0.47}As [4] on Si has been explored with some success using thick buffer layers to relieve the strain caused by the high lattice mismatch. High room temperature electron mobility of 18,000 cm\textsuperscript{2}/V·s for InAs (4 to 7 μm layer thicknesses) has been demonstrated by Kalem et al. [3].

In this paper ultra thin InAs (~ 10 nm) films have been grown on silicon substrate using MBE. Electrical and photo response measurements have been performed to characterize the transport properties of the thin film and the diode formed by n-InAs/p-Si.
EXPERIMENT

Ten nanometer InAs films have been grown on three different substrates: p-Si (211), p-Si (100) and SiO₂ using MBE at Duke University. The sample numbering and the corresponding growth conditions are shown in Table I.

**Table I. List of 10 nm InAs films grown at different conditions and substrates.**

<table>
<thead>
<tr>
<th>sample</th>
<th>substrate</th>
<th>orientation</th>
<th>$T_{AN}$ (°C)</th>
<th>$t_{AN}$ (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P306</td>
<td>SiO₂/p-Si</td>
<td>(100)</td>
<td>420</td>
<td>5</td>
</tr>
<tr>
<td>P309</td>
<td>p-Si</td>
<td>(100)</td>
<td>n</td>
<td>0</td>
</tr>
<tr>
<td>P313</td>
<td>p-Si</td>
<td>(211)</td>
<td>n</td>
<td>0</td>
</tr>
</tbody>
</table>

$T_{AN}$: annealing temperature;  
$t_{AN}$: annealing time.

High-k dielectric Al₂O₃ is evaporated in an AIRCO TEMESCAL FC1800 electron beam system at a rate of 1 ˚s⁻¹ and oxygen background of 5 × 10⁻⁵ Torr to cap the InAs surfaces, offering the insulation between bonding pads. The sub-micron Al/Ti (120/20 nm) contacts to the InAs films are formed by etching through the Al₂O₃ using BHF and following with lift-off process and making contact between the bonding pads and InAs film. Two controlled samples C1 and C2, p-Si (100) and p-Si (211), respectively, are also processed as the reference devices. Figure 1 is the scaled drawing of the device cross section which shows two adjacent contacts, P1 and P2.

![Device cross section](image)

**Figure 1.** Device cross section in (a) is shown next to (b) the computed energy band diagram for the InAs on Si heterostructure, drawn normal to the wafer at the center of the device. P1 and P2 are the contacts formed to the InAs film.

The representative device structure has been shown in figure 1 (a). The n-InAs/p-Si diode characteristics and the transport through InAs films are both tested. All the measurements are performed using Agilent 4155C system. The diode characteristic is tested by
grounded the p-Si substrate and biasing the one of the contacts, P1 or P2. Transport in InAs film is studies by taking the I-Vs between two adjacent contacts.

Figure 2 (a) and (b) are SEM images of two fabricated four-probe devices.

![SEM images of four-probe devices](image)

Figure 2. SEM images of four-probe devices fabricated on (a) P313, 10 nm InAs/p-Si (211) and (b) C2, p-Si (211).

**DISCUSSION**

From the SEM images in figure 2, the InAs films on Si substrates appear to be poly-crystalline, which is not observed in the Si reference sample. The grain size is in the range of 5 – 25 nm. In order to interpret the electrical measurements of n-InAs/p-Si diodes, Schottky diodes are fabricated on the Si substrates, C1 and C2, with same doping type and orientation match that of the corresponding InAs/Si n-p diodes.

**n-InAs/p-Si diode characteristics**

Figure 3 (a) shows the diode characteristics of InAs/Si n-p diode fabricated on P313 (InAs on p-Si (211)) together with the reference Schottky diode fabricated on p-Si (211) and (b), of InAs/Si n-p diode on P306 (InAs on p-Si (100)) with p-Si (100) Schottky.
Compared to p-Si Schottky diodes, both InAs/Si n-p diodes give higher current densities, more than two orders improvement for InAs/Si (211) and about two orders for InAs/Si (100). This increase of current density is caused by more generations happening at the InAs/Si n-p junction area due to narrower band gap, 0.36 eV, of InAs.

**Transport in poly-crystalline InAs films**

To remove the effect of Si substrate, 10 nm InAs is deposited onto a 130 nm SiO<sub>2</sub>/p-Si structure, P306. Figure 5 is the I-V characteristics of two adjacent contacts on sample P306, InAs/SiO<sub>2</sub>, under the condition of with and without microscope illumination.

Figure 5. I-V characteristics between two adjacent contacts of four-probe device on P306, InAs/SiO<sub>2</sub>. The inset is the SEM image of the two contacts area, showing a spacing of 32 nm. The solid curve is obtained in dark, while the dashed curve is the response to the illumination from the probe station light source.
From SEM image of the device, InAs appears to be poly-crystalline. The I-V appears to be almost linear. The resistance between the two 32 nm spaced contacts is about 500 MΩ in the dark. The contact resistivities to the poly-crystalline InAs range from 0.5 to 80 µm² [6], hence can be neglected compared to the film resistance. A crude estimate for the 2-probe spreading resistance in the InAs is \( R = \rho / t \), where \( \rho \) is the InAs sheet resistivity and \( t \) is the thickness of the InAs film. The sheet resistivity of a film is the product of the unit charge \( q \), carrier density \( n \) or \( p \), and mobility \( \mu \). Assuming an electron density of \( 10^{19} / \text{cm}^3 \) [7] and for a 32 nm probe spacing, the electron mobility in the poly-crystalline 10 nm InAs film is estimated to be 310 cm²/Vs. This mobility is higher than those of 75 – 320 nm poly InAs films in [7]. Since the InAs film is deposited on 130 nm thick SiO₂ film, the photo current from the Si substrate can be eliminated. So, the photo current observed in figure 5 is the really photo response from InAs film.

Figure 6 shows the I-V characteristics of two adjacent contacts on sample P313, n-InAs/p-Si (211), under the condition of with and without microscope illumination.

![Figure 6. I-V characteristics between two adjacent contacts of four-probe device on P313, n-InAs/p-Si (211). The inset is the SEM image of the two contacts area, showing a spacing of 340 nm. The solid curve is obtained in dark, while the dashed curve is the response to the illumination from the probe station light source. Compared to device characteristics shown in figure 5, the I-V curves in figure 6 show similar resistance between contacts in dark, ~ 460 MΩ, with ten times increase in the device spacing. The unchanged resistance between adjacent contacts with one order larger spacing indicates that the transport happen mostly in Si substrate instead of in the 10 nm InAs film.

CONCLUSIONS

This study shows for the first time InAs/Si n-p diodes formed on Si substrates with different orientations, (211) and (100). Compared to Si Schottky diodes, the presence of the thin InAs films increases the current densities for more than 2 orders of magnitude.
This increase indicates the Fermi level at the InAs surface has been pinned. Photo currents have been observed on the InAs film deposited on SiO$_2$ and p-Si (211).

ACKNOWLEDGMENTS

This work is supported by the National Science Foundation (contract ECS05-06950), the National Institute of Standards and Technology, and the Semiconductor Research Corporation through a NIST/SRC Graduate Research Fellowship.

REFERENCES

Student Paper

InAs Growth On Submicron (100) SOI Islands for InAs-Si Composite Channel MOSFETs

Bin Wu\textsuperscript{a}, Dana Wheeler\textsuperscript{a}, Changhyun Yi\textsuperscript{b}, Inho Yoon\textsuperscript{b}, Smita Jha\textsuperscript{c}, April Brown\textsuperscript{b}, Thomas Kuech\textsuperscript{c}, Patrick Fay\textsuperscript{b}, and Alan Seabaugh\textsuperscript{a}

\textsuperscript{a}Dept. of Electrical Engineering, University of Notre Dame, \texttt{bwu@nd.edu}
\textsuperscript{b}Department of Electrical and Computer Engineering, Duke University
\textsuperscript{c}Department of Chemical and Biological Engineering, University of Wisconsin-Madison

A thick transition layer (often exceeding 100 nm) is commonly used to grow III-V semiconductors on Si. In this study, we explore the growth of ultra thin and highly-mismatched InAs directly on SOI islands. SOI islands allow the termination of misfit dislocations at the island edges to relieve the strain. For MOSFETs, the ability to tailor the ratio of InAs to Si in an ultrathin (~3 nm) channel allows optimization of both the channel density-of-states effective mass and the bandgap [1], for achieving high channel current at low voltage. We show that flat, planar, growth of InAs can be achieved, despite the 11.6% lattice mismatch, on submicron SOI islands by molecular beam epitaxy (MBE) toward realization of MOSFETs. Furthermore, metalorganic chemical vapor deposition is shown to nucleate InAs selectively on SOI islands and first back-gated transistor results are presented.

Wafers of 100-mm-diameter (100) SOI are thinned using a Logitech CDP (chemical delayering and planarization) system to approximately 500 nm, using an experimental slurry from Cabot Microelectronics, EXP-0012. Thermal oxidation followed by oxide removal in buffered HF is used to thin the Si to a layer thickness as small as 10 nm. After this process the wafer has a surface flatness within ±1 nm when measured over a 1 µm length.

Dow Corning FOx-12 flowable oxide, containing hydrogen silsesquioxane (HSQ) as the primary component, is coated on the wafer and used as a negative electron-beam-lithography (EBL) resist to pattern submicron islands for definition by reactive ion etching (RIE). An Alcatel 601e RIE is used to etch the Si using SF\textsubscript{6} and O\textsubscript{2} at -120 °C. The Si etch rate is approximately 150 nm/min with a 1:4:1 etch selectivity between Si and FOx-12.

Prior to loading for MBE, the wafer surface with the HSQ islands was characterized by x-ray photoelectron spectroscopy (XPS) which showed that the surface is clean. The FOx-12 was next removed in a 15 s buffered-HF dip and the wafer was loaded directly into the MBE system. The native oxide on the Si islands was blown off at high temperatures, ranging from 710 to 750 °C, as determined by monitoring the RHEED pattern (reflection high-energy electron diffraction). As much as 40 nm of InAs was then deposited by MBE at temperatures of 110, 200, and 250 °C using a V:III flux ratio of 33:1. These low growth temperatures were used to prevent the islanding of InAs that is common at higher growth temperatures [2]. Scanning electron microscopy (SEM) shows that approximately 1 in 4 islands grown at 250 °C achieve a flat growth.

Flat, planar growth occurred only for the MBE samples grown at 250 °C; growths at 110 °C and 150 °C yielded only polycrystalline InAs. Growth of InAs on large Si islands (tens to hundreds of square microns) as well as growth on SiO\textsubscript{2} yielded polycrystalline InAs at all three growth temperatures. Patterned SOI lines of width 200 nm also nucleated smooth, flat InAs at 250 °C, while growth on 500-nm-width lines and all lines grown at lower growth temperatures were polycrystalline.

This work was supported by the National Science Foundation (contract ECS05-06950), and the National Institute of Standards and Technology and Semiconductor Research Corporation through a NIST/SRC Graduate Research Fellowship.

References


Fig. 1. Energy band diagram of the InAs-on-SOI composite channel MOSFET.

Fig. 2. SEM cross-section of a (100) SMOX-SOI wafer after CMP and thermal oxidation thinning.

Fig. 3. SEM image of SOI islands after FOx-12 removal and before growth on InAs. SEM and AFM show the island heights ranges from 150 to 400 nm in a 10 μm field.

Fig. 4 (right). SEM images of the 250 °C MBE InAs growth (a) on a 100-μm-scale Si island and (b) on an adjacent SiO₂ surface. Note the growths on these surfaces appear to be polycrystalline.

Fig. 5. SEM images of 250 °C MBE InAs growths on (100) 500 x 500 nm² SOI islands: (a) approximately one-in-four are flat and planar, (b) some show a coalesced network.

Fig. 6 SEM images of the 250 °C MBE InAs growth on SOI lines: (a) 200 nm and (b) 500 nm width. Only on the 200-nm-width lines is smooth, flat growth of InAs observed.

Fig. 7. (a) SEM of Ti/Al source/drain contacts to InAs on (100) SOI island, grown selectively by MOCVD at 450 °C. The island size is 0.2 x 2 μm². (b) Common-source back-gated transistor characteristic showing weak gate control due to the thick InAs layer and thick oxide ($I_D \approx 60 \, mA/\mu m^2$ at 600 μA).
REFERENCES


