INDIUM-GALLIUM-ARSENIDE AND GERMANIUM TUNNEL JUNCTIONS

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Abstract

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$In_{0.53}Ga_{0.47}As$ tunnel junctions were fabricated towards use in tunneling field effect transistors which have shown promise as low-subthreshold-swing transistors. Tunnel junctions were fabricated with doping densities ranging from 10^{19} cm^{-3} to 10^{20} cm^{-3}. Reverse tunneling current, the regime of operation in TFETs, was measured and modeled as function of doping density and electric field. Reverse current was measured up to a current density of 1.5 $mA/\mu m^2$. High current density tunnel junctions are demonstrated as evidenced by forward bias peak current densities in the range 0.06 to 0.94 $mA/\mu m^2$, the latter comparable to the best reported results for $In_{0.53}Ga_{0.47}As$ junctions.

Tunnel junctions were also explored in Ge motivated by tunnel diode oscillator sensors. Germanium tunnel junctions were fabricated using two approaches: (1) rapid melt regrowth of Al-doped *p*+ Ge from an Al metal source into *n*+ Ge and (2) *p*+ Ga doping by diffusion from a Ga metal source into *n*+ Ge. The *n*-type dopant was P, introduced either via ion implantation or diffusion from spin-on diffusants. In the rapid melt regrown junctions, negative differential resistance characteristic was obtained with

peak current density of up to 0.27 mA/μm^2 and peak to valley ratios of 1.1-1.23. In the diffusion based approach, *p*-type doping by Ga diffusion from a molecular beam epitaxy source was characterized as function of Ga flux and deposition time. Diodes fabricated using Ga as *p*-type, and P as *n*-type dopant, exhibited a backward diode behavior.

INDIUM-GALLIUM-ARSENIDE AND GERMANIUM TUNNEL JUNCTIONS

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CHAPTER 1. INTRODUCTION AND MOTIVATION

1.1 Introduction

Improving complementary metal-oxide-semiconductor (CMOS) based technology by introducing new materials and devices that add functionality is cited by the International Technology Roadmap for Semiconductors [1] as a way to extend Moore's Law [2]. Tunnel diodes (TDs) with their negative differential resistance (NDR), bistability, and high intrinsic switching speed have shown capability to enhance circuit performance by reducing power consumption, device count, and delay [3-7].

The *N*-shaped current-voltage (*I-V*) characteristic arising from interband tunneling in a heavily-doped $p+n+$ junction was first observed and analyzed in 1957 by Leo Esaki [8]. Within a few years of the discovery, the Esaki diode was showing considerable promise across a wide range of applications [9]. By 1961, the TD was being incorporated into oscillators [10], amplifiers [11], pulse generators [12], memory, and flip flops [13]. However, the Esaki diode had a limitation of lack of isolation between the input and output [9]. The emergence of the integrated circuit (IC) and the discrete nature of the device brought the early commercial activity to an end [9]. Even though batch processing

for the Esaki diode was demonstrated in 1967 [14] and explorations have continued to produce IC-compatible TDs on Si [15-18], foundry processes are currently not available for IC development incorporating TDs. The discovery of resonant tunneling in III-V heterostructures led to a rejuvenation of interest in TDs [3, 19, 20] in the 1980s and 1990s. Growth techniques such as molecular beam epitaxy (MBE) made it possible to develop ICs with III-V TDs and transistors [5, 21]. Tunnel diodes were proposed to extend the exponential growth in functional density of the Si IC industry, before limits of CMOS scaling were reached [20], and with CMOS scaling continuing it is not clear that this will happen.

Currently, however, interband tunnel junctions are attracting much attention for use beyond the CMOS scaling limits in low-subthreshold-swing tunneling field-effect transistors (TFETs) [22-25]. In TFETs, an electric field is used to control the reverse current of a p+n+ tunnel junction which can result in subthreshold swings less than 60 mV/decade, the theoretical limit of a MOSFET. This is attractive because with scaling down of MOSFETs, power dissipation has become the main concern, and the power supply cannot be reduced further due to the subthreshold slope limit.

In TFETs, tunnel junctions are required with current densities comparable to channel current densities in high performance MOSFETs. The ITRS roadmap shows drain-source currents of 1 mA/μm [1] at a drain-source bias of 1 V in high performance 2008 MOSFETs. In fabricated Si TFETs channel currents have been low, 0.02 mA/μm [25], limited by the high energy bandgap (1.1 eV) and high carrier effective masses ($0.19m_o$ for transverse electrons and $0.16m_o$ for light holes). The tunneling current in a

pn junction is increased by choosing or engineering a material with a low bandgap and carrier effective mass or by maximizing the junction electric field by increasing the dopant density and junction abruptness. Using $Si_{0.7}Ge_{0.3}$ tunnel junctions in TFETS led to an improvement in channel current to 0.12 mA/μm from 0.02 mA/μm [25].

In this work, tunnel junctions for TFETs were explored in $In_{0.53}Ga_{0.47}As$ which has bandgap and carrier masses that are much lower than in Si, Table 1.1. While low bandgap materials such as InSb and InAs are possible candidates for TFET tunnel junctions, $In_{0.53}Ga_{0.47}As$ has the advantage of being lattice matched to InP and the MBE growth in this system is more mature.

Table 1.1

Basic parameters of $In_{0.53}Ga_{0.47}As$ and Si at 300 K [26]

Parameter	$In_{0.53}Ga_{0.47}As$	Si
Bandgap (eV)	0.74	1.12
Electron effective mass	$0.041m_o$	$0.19m_o$ (light mass)
Light hole effective mass	$0.052m_o$	$0.16m_o$
Dielectric constant	13.9	11.9

m_o is the electron mass

In TFETs, the on-state of the transistor corresponds to the Zener tunneling regime of interband tunnel junctions. Zener tunneling in $In_{0.53}Ga_{0.47}As$ junctions has received some attention in the development of avalanche photodiodes [27, 28] for fiber receivers. In avalanche photodiodes it is important to keep the junction doping low to circumvent interband tunneling; however near breakdown Takanashi *et al*. [27] found that Zener

tunneling is still responsible for the dark current. Both Takanashi [27] and Pearsall [28] showed that the Kane-Sze formula [29, 30], used later, provides an accurate description of the Zener tunneling current. Blanco *et al*. [31] studied conduction mechanisms in *n*+*p* diodes made by ion implantation of *n*-type dopants (Si, 10^{19} cm^{-3} or Si and P co-implanted) into a *p*-type (Zn-doped, 10^{16} cm^{-3}) $In_{0.53}Ga_{0.47}As$ epitaxial layer. They used *I-V* measurements and admittance spectroscopy and determined that reverse current in these implanted junctions could be described by different tunneling mechanisms depending on the bias. While at low bias thermally assisted tunneling explained observed data, at higher biases the data was fit using additional trap assisted tunneling currents. The traps were believed to originate from either Zn doping in the Si implanted junctions or from P implantation damage in the co-implanted junctions.

In TFETs where high on-state currents are required to compete with MOSFETs, doping densities can be pushed to solid solubility limits, generally near 10^{20} cm^{-3} for dopants of interest. Measurements of reverse tunneling current in $In_{0.53}Ga_{0.47}As$ junctions at such doping densities is lacking in the literature.

In this work, $In_{0.53}Ga_{0.47}As$ tunnel junctions were fabricated with *p* and *n*-type doping densities from 10^{19} cm^{-3} to ~10^{20} cm^{-3} enabling measurement of reverse current density relevant to high current density TFETs. Since the material system was chosen to be $In_{0.53}Ga_{0.47}As$, the effective mass and bandgap was decided and the design variable was electric field. For a given material, the electric field is a function of the doping density and doping gradient. Dopant profiles were obtained using secondary ion mass spectroscopy (SIMS), while the electrically-active dopant concentrations were determined from Hall measurements and zero-bias capacitance measurements. The

measured impurity profiles were used to calculate the maximum junction electric field using the one-dimensional Poisson solver BandProf [32]. Reverse tunneling current in $In_{0.53}Ga_{0.47}As$ as a function of field and doping density was then modeled using the tunneling Kane-Sze formula assuming a uniform field [29, 30]. The forward bias direction of the tunnel junction is of interest as the dependence of the peak current density on doping density yields reduced tunneling masses [29] and dependence of peak and valley voltage on doping density provides an estimate of the sum of degeneracies on the *n*- and *p*-side of the junctions [29].

Another motivating interest in tunnel junctions is in sensors. Tunnel diode oscillators (TDO) consisting of a TD and an LC tank circuit have been used for the measurement of various phenomena, e.g. pressure [33], temperature [34], and magnetic field strength [35]. The TDO as a sensor changes its resonant frequency in response to changes in capacitance, inductance, or losses induced by the physical stimulus, e.g. charge, temperature, pressure, or changes in local electromagnetic medium.

In published TDO sensors, the frequency of operation ranges from a few kHz to few tens of MHz [33-35]. A simple approach for forming Ge tunnel junctions developed at the University of Notre Dame uses a rapid melt regrowth (RMR) process [36]. In RMR, phosphorus-doped Ge is melted back into an Al contact and then regrown back on cooling to grow an epitaxial Al-doped Ge layer and form an $n+p+$ tunnel junction. This approach uses a spin-on dopant (SOD) diffusion for the P $n+$ doping. Zhang *et al*. [22-25] showed by transmission electron microscopy (TEM) that the junctions regrown by this method showed excellent crystallinity but that the melt-back is not planar.

Experiments shown here examine ion implantation in place of the phosphorus spin-on diffusant to provide a cleaner starting surface for RMR. Ion implantation does away with the need for cleaning of SOD residue after diffusion. This experiment extends the doctoral research of Yan Yan [37] on Si and Jialin Zhao [38] on Si and Ge.

Tunnel diodes were also fabricated in the SiGe system, using ultrahigh vacuum chemical vapor deposition (UHV-CVD) to grow *n*+ doped SiGe layers, followed by rapid thermal processing (RTP) of SODs to obtain the *p*+ doping and the *p*+*n*+ junction. In these junctions a peak tunneling current density of 1.8 $\mu A/\mu m^2$ was demonstrated and reported in two papers co-authored with Lars-Erik Wernersson, Lund University, Sweden, titled "SiGe Esaki tunnel diodes fabricated by UHV-CVD growth and proximity rapid thermal diffusion" [39] and "A combined chemical vapor deposition and rapid thermal diffusion process for SiGe Esaki diodes by ultra-shallow junction formation" [40]. These papers are included as Appendices I and II respectively.

1.2 Accomplishments and organization of dissertation

In Chapter 2 the physics of tunneling is described and the origin of the *N*-shaped behavior of the *I-V* characteristic of the tunnel diode is detailed. The Kane-Sze tunneling current formula based on tunneling through a triangular barrier is introduced..

Chapter 3 details the research performed on $In_{0.53}Ga_{0.47}As$ *p*+*n*+ junctions. The junctions were fabricated by MBE using C and Si as the *p* and *n* type dopants. A self-aligned collector process for the *p*+*n*+ diode was demonstrated. Measurement and

modeling of reverse current densities is shown up to 2 mA/μm^2, the highest reported for InGaAs junctions. In the forward bias region peak current densities in the range 0.06-0.94 mA/μm^2, with 0.94 mA/μm^2 being comparable to the highest reported for $In_{0.53}Ga_{0.47}As$ junctions [41]. Peak-to-valley current ratios (PVR) of ~17, also comparable to the best in literature, are obtained.

Ge *p*+*n*+ tunnel junctions were fabricated using RMR of Al on Ge for the *p*-type doping, and ion implantation of P for the *n*-type doping. A current density of 0.27 mA/μm^2 is demonstrated in these Ge junctions while the PVRs obtained are in the range 1.10-1.23. The experimental work done on Ge *p*+*n*+ junctions is presented in Chapter 4.

Accomplishments and new findings are summarized in chapter 5. Suggestions for future work and possibilities for improving the current density in $In_{0.53}Ga_{0.47}As$ and Ge tunnel junctions are also given.

CHAPTER 2. TUNNEL DIODE PHYSICS

Interband TDs are *p*+*n*+ junctions with degenerate doping densities. In degenerately-doped *pn* junctions, electric fields on the order of 10^6 V/cm lead to depletion widths of a few nanometers, enabling electrons to quantum-mechanically tunnel between bands across the semiconductor bandgap. The measured *I-V* characteristic of a Si TD is shown in Fig. 2.1. The bias dependence of the interband tunneling produces a negative differential resistance (NDR) in the *I-V* characteristic, arising from a disruption of the tunneling channel as the diode is forward biased.

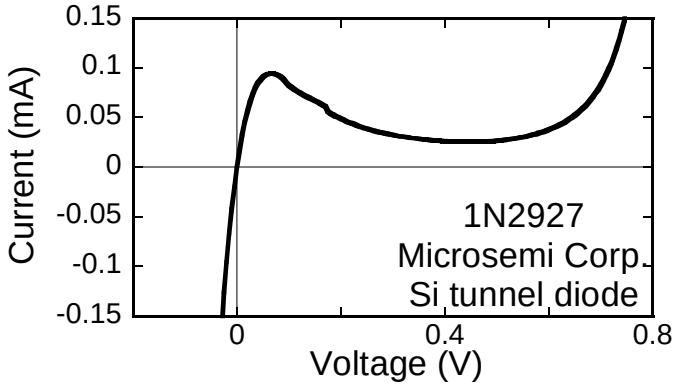


Figure 2.1 Current-voltage characteristic of a commercial Si TD [42], no longer available.

2.1 Physics of current-voltage characteristic

The *I-V* characteristic of a TD can be qualitatively explained using the band diagram and characteristics shown in Fig. 2.2. When a reverse bias is applied, Fig. 2.2(a), current flows by electrons tunneling from occupied states on the *p*-side valence band into unoccupied states on the *n*-side conduction band. In equilibrium, with no applied bias, Fig. 2.2(b), when the Fermi level on each side is aligned, the net tunneling current is zero. When a forward bias is applied, current flow occurs by electrons tunneling from occupied states in the *n*-side conduction band into unoccupied states in the *p*-side valence band. Maximum alignment between electrons on the *n* side and holes on the *p* side gives the peak current, I_p, at voltage V_p as in Fig. 2.2(c). When the conduction band minimum on the *n* side is raised just above the valence band on the *p* side, Fig. 2.2(d), the valley current, I_v, is obtained, as indicated at the voltage V_v in Fig. 2.2(a). With further increase in the voltage, the current increases due to tunneling through defect states in the depletion layer and thermionic emission over the diode internal barrier, Fig. 2.2(e). Tunneling between the conduction band and valence band can be direct or indirect depending on the band structure of the semiconductor. In direct bandgap semiconductors such as InGaAs, the conduction band minimum and valence band maxima occur at the same value of momentum in the band structure, while in indirect bandgap semiconductors like Si, they occur at different points in the momentum space. Momentum is conserved in the tunneling process facilitated by phonons.

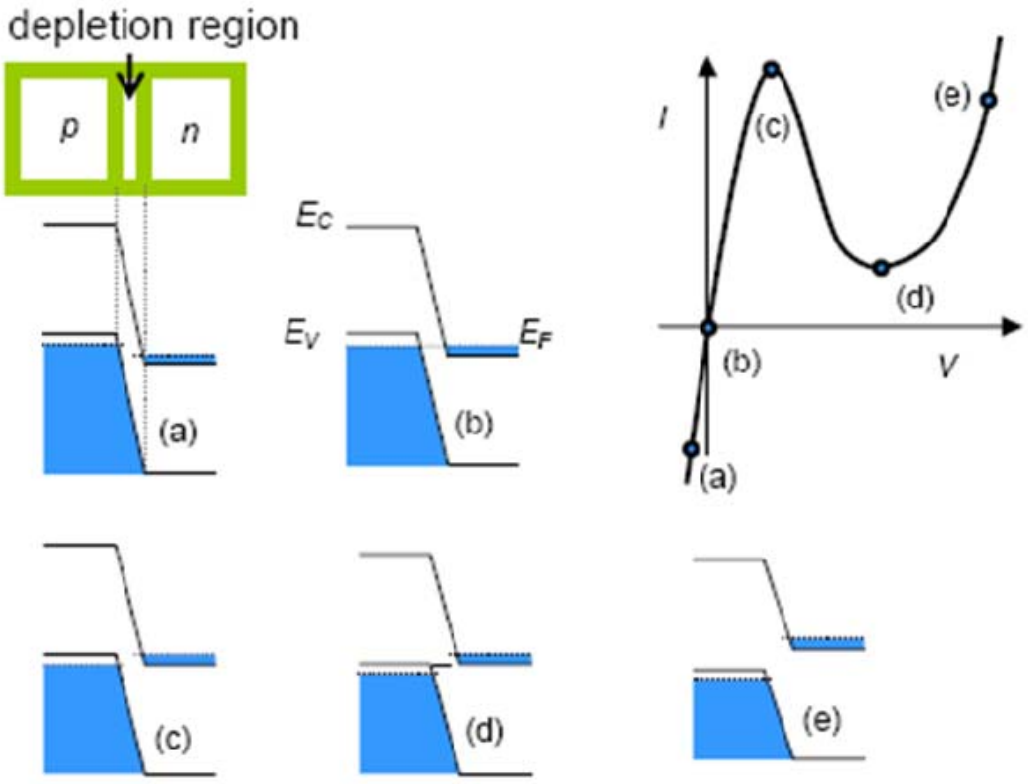


Figure 2.2 Schematic current-voltage characteristic and energy band diagram and of an Esaki TD adapted from reference [38].

The current density of a TD is a function of the tunneling probability of carriers through the potential barrier presented by the bandgap. Figure 2.3 shows the calculated energy band diagram of an abrupt $In_{0.53}Ga_{0.47}As$ $p+n+$ junction with a symmetric doping density of 5 x 10^{19} cm^{-3}, and also shows the potential barrier for tunneling carriers. It can be seen that the tunneling barrier for conduction band electrons and valence band holes can be approximated by a triangular barrier of height E_g as indicated for electrons in Fig. 2.3.

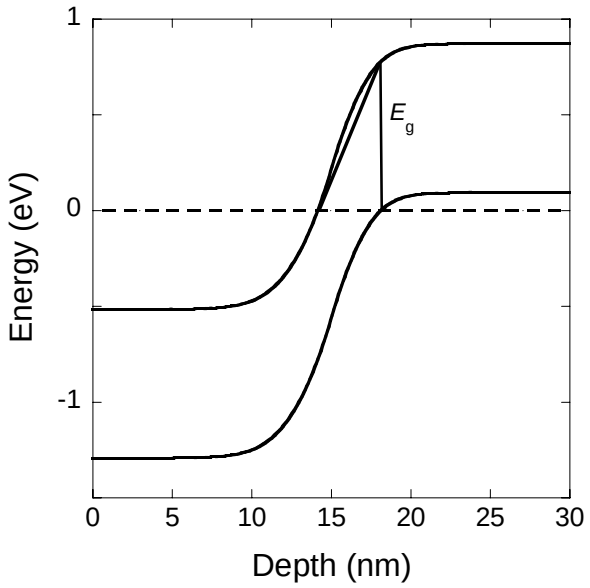


Figure 2.3 Energy band diagram of an abrupt $In_{0.53}Ga_{0.47}As$ $p+n+$ junction with a symmetric doping density of 5 x 10^{19} cm^{-3}, calculated using BandProf [32]. Also shown is the triangular barrier approximation for the tunneling barrier for conduction band electrons.

The Kane-Sze formula [29, 30] for reverse tunneling current density through a triangular barrier has been recently derived with a factor 1/2 correction by Zhang [30, 43]

$$J = \frac{\sqrt{2m_r^*}q^3\xi V_R}{8\pi^2\hbar^2 E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m_r^*}E_g^{\frac{3}{2}}}{3q\xi\hbar}\right), \tag{2.1}$$

where q is the electron charge, $\hbar = h/2\pi$ is Planck's constant, ξ is the field, V_R is the applied reverse voltage, and m_r^* is the reduced effective mass in the direction of tunneling. The reduced mass is given by [29],

$$m_r^* = \frac{m_c^* m_v^*}{m_c^* + m_v^*}, \tag{2.2}$$

where m_c^* is the effective mass of electrons, and m_v^* is the hole effective mass in the direction of tunneling.

For a given material, current density is improved by increasing the electric field in the junction. The field used in the triangular barrier approximation is assumed to be the maximum electric field in the *pn* junction, given by [44],

$$\xi = \sqrt{\frac{2qN(V_{bi} - 2kT/q)}{\varepsilon_s}}, \tag{2.3}$$

where k is Boltzmann's constant, T is the temperature, ε_s is the permittivity, V_{bi} is the built-in voltage, and N is the effective doping density of the p+n+ junction with net donor concentration N_d and net acceptor concentration N_a [44],

$$N = \frac{N_a N_d}{N_a + N_d}. \tag{2.4}$$

The built-in voltage is given by, $V_{bi} = E_g + \zeta_n + \zeta_p$, where ζ_n and ζ_p are the n-side and p-side degeneracies, defined as the difference between the conduction band and Fermi level, and the Fermi level and valence band, respectively.

The tunneling current density in Si, Ge and $In_{0.53}Ga_{0.47}As$ is plotted in Fig. 2.4 as a function of the electric field in an abrupt *pn* junction. The effective masses and bandgaps used for the calculation are shown in the inset. The effective masses are calculated using Eq. 2.2, where the light hole mass was used for the hole mass, and the transverse electron mass was used for electron mass in Si. For Ge, the electron mass used was calculated for

transport in the (100) direction via the (111) conduction band minima. As an estimate, the conductivity electron mass is used, given by $\frac{1}{m_c^*} = (\frac{1}{3m_l^*} + \frac{2}{3m_t^*})$. From Fig. 2.4 it can be seen that Ge and $In_{0.53}Ga_{0.47}As$ offer a significant improvement in current density compared to Si. The exploration of low bandgap tunnel junctions in materials such as Ge for use in TFETs is already under way [24].

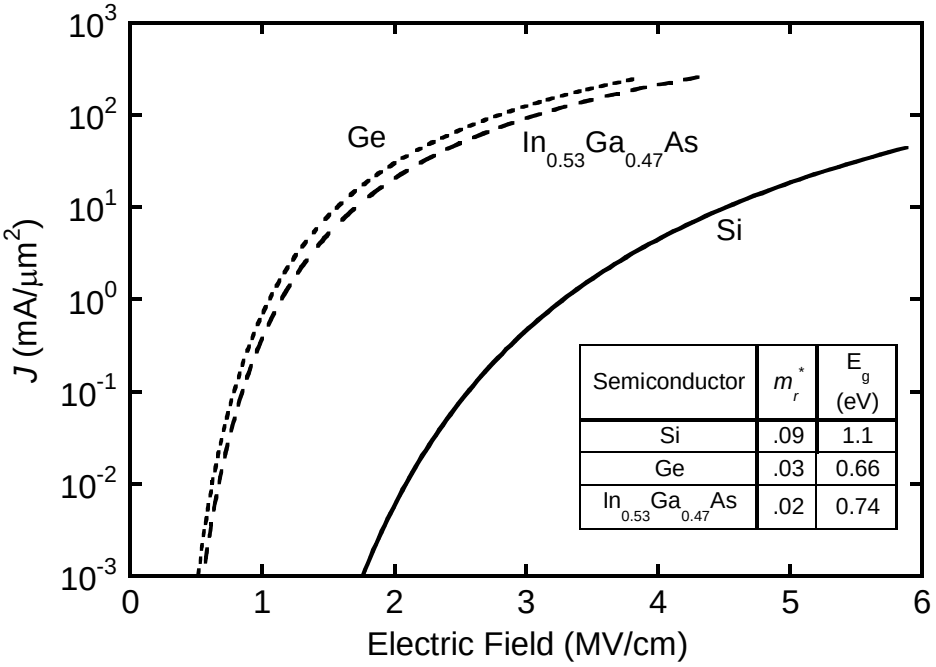


Figure 2.4 Tunneling current density in Si, Ge and $In_{0.53}Ga_{0.47}As$ tunnel junctions as a function of maximum electric field in the junction for a reverse bias of 1 V. Material parameters are obtained from reference [26]. The reduced mass is evaluated using Eq. (2.2).

The above plot predicts tunneling current densities that are achievable in $In_{0.53}Ga_{0.47}As$ tunnel junctions and can be used for comparison with current densities that are achieved in present day MOSFET technology. The ITRS roadmap shows drain-source currents of 1 mA/μm [1] at a drain-source bias of 1 V in high performance 2008

MOSFETs (29 nm gate length). If one assumes a channel doping density of 10^{18} cm^{-3}, and a gate oxide thickness of 1 nm, and a gate bias of 1 V, most of the carriers in the inversion layer are confined to a thickness of approximately 3 nm, as simulated from BandProf. This translates to a current density of approximately 333 $mA/\mu m^2$ in high performance MOSFETs, at a channel current of 1 mA/μm. It can be seen from Fig. 2.4 that tunnel junctions in $In_{0.53}Ga_{0.47}As$ are capable of producing current densities of approximately 300 $mA/\mu m^2$ at a reverse bias of 1 V, comparable to high performance MOSFETs.

In this chapter the Kane-Sze formula for interband tunneling has been presented based on tunneling through a triangular barrier. Tunneling is a strong function of bandgap, effective mass and junction doping density. The Kane-Sze formula predicts that InGaAs tunnel junctions should yield current densities that are comparable to high performance MOSFETs.

CHAPTER 3. INDIUM GALLIUM ARSENIDE TUNNEL JUNCTIONS

In this chapter, experimental results are presented on fabrication and electrical characterization of $In_{0.53}Ga_{0.47}As$ tunnel junctions grown by MBE using C and Si as the *p*- and *n*-type dopants. In these junctions impurity densities near the limits of solid solubility were explored, ranging from 10^{19} to 10^{20} cm^{-3}. The impurity profiles were measured using SIMS. Junction fields were computed from band diagram simulations using the measured SIMS dopant profiles. In *I-V* measurements of the tunnel junctions, reverse current measurements were measured to compare with the Kane-Sze formula [29, 30]. The forward peak current densities, up to 0.94 $mA/\mu m^2$ are comparable to the highest previously reported.

3.1 Carbon and silicon doping of InGaAs

Carbon being a group IV element can incorporate in III-V compound semiconductors either on the group V site as an acceptor or on the group III site as a donor. In (100) GaAs, C incorporates as an acceptor and high hole densities of up to 1.5×10^{21} cm^{-3} have been achieved [45] as measured by Hall effect. The case of $In_{1-x}Ga_xAs$ however is different with the hole concentration being dependent on the In content. This is attributed to a weaker In-C bond compared to the Ga-C bond [46].

Lubyshev *et al*. [47] observed that the hole concentration decreases as the In content increases beyond 0.7 and changes to *n*-type at around 0.8 in C doped $In_{1-x}Ga_xAs$ using MBE and CBr_4 as the source. The acceptor densities achieved in InGaAs are significantly lower compared to GaAs. The best reported results for C doping in $In_{0.53}Ga_{0.47}As$ are shown in Table 3.1, with the highest being 2.1 x 10^{20} cm^{-3} [48].

Carbon has low diffusivity in InGaAs compared to other *p*-type dopants such as Be and Zn [49] although quantitative data on C diffusivity in $In_{0.53}Ga_{0.47}As$ is sparse. Pearton [49] estimates a diffusivity from SIMs of less than 3 x 10^{-14} cm^2/s at 800 ºC for implanted C in $In_{0.53}Ga_{0.47}As$. The low diffusivity of C makes it an attractive choice for obtaining abrupt dopant profiles.

Like C, Si is a group IV element, and exhibits amphotericity in GaAs depending on the orientation of the substrate [50, 51]. It shows *n*-type behavior for (100) GaAs and (111)B faces of GaAs, but is amphoteric on the (111)A face [50]. It is observed that on the (111)A face, Si behaves as a donor when incorporated by MBE under high V/III ratio and as an acceptor under low V/III ratio [50]. In the case of $In_{0.53}Ga_{0.47}As$, Schneider *et al*. [51] reports that for a Si density of 7 x 10^{17} cm^{-3} Si is a donor on both (100) and (111) surfaces. In Si-doped $In_{0.53}Ga_{0.47}As$, electron concentrations as high as 6.1 x 10^{19} cm^{-3} have been reported, Table 3.1.

In this thesis research, C densities of up to 10^{20} cm^{-3} were examined and since the In content was less than 0.7 amphoteric behavior is not expected. In the case of Si, amphotericity is also not expected based on the above discussion. An effort was made to push Si densities beyond the best reported value of 6.1 x 10^{19} cm^{-3}. A δ-doping technique

was used obtain Si densities higher than 10^{20} cm^{-3}. The results of C and Si doping are discussed in the next section.

Table 3.1

Carrier concentrations achieved in $In_{0.53}Ga_{0.47}As$ using C and Si by other researchers obtained using Hall effect

Dopant	Growth	Source	Carrier density (cm^{-3})	Reference
C	MBE	CBr_4	2.1×10^{20}	Cai [48]
C	CBE	CBr_4	2.0×10^{20}	Han [52]
Si	GSMBE	$SiBr_4$	3×10^{19}	Jackson [53]
Si	MBE	Si	6.1×10^{19}	Fujii [54]

CBE: Chemical beam epitaxy, GSMBE: Gas source MBE

3.2 $In_{0.53}Ga_{0.47}As$ *p*+ on *n*+ tunnel structure

The $In_{0.53}Ga_{0.47}As$ *p*+*n*+ structures in this work were grown by MBE using solid sources of In, Ga, and As at a substrate temperature of 450 ºC. The *p*-type dopant, C, was incorporated from a carbon-tetrabromide source, while the *n*-type dopant source was Si. All MBE $In_{0.53}Ga_{0.47}As$ growths were performed by Intelligent Epitaxy Technology (IntelliEpi) of Richardson, Texas. The Ga source purity was 99.99999%, with K < 110 parts per billion (ppb), Ag < 65 ppb, and Ge < 20 ppb. The In source purity was 99.99995%, with all impurities < 0.1 ppm. The As source purity was 99.99999%, with Si 15 ppb, and Fe 11 ppb.

The carrier concentrations in C-doped and Si-doped InGaAs wafers were measured by IntelliEpi using Hall effect. In the C-doped wafer (305C), a hole concentration of ~10^{20} cm^{-3} was measured in a uniformly doped wafer. The *n*+ wafer

(329C) had a 100 nm thick InGaAs layer grown with a flux to achieve 5 x 10^{19} cm^{-3}; every 5 nm the growth was interrupted and was delta doped to obtain twenty doping spikes at the 10^{13} cm^{-2} level, for a total target concentration of 1.5 x 10^{20} cm^{-3}. The measured electron concentration was however lower, at 5.8 x 10^{19} cm^{-3} which incidentally is similar to the highest reported electron concentration obtained using Si [54].

In the first tunnel structure grown, a *p*+ on *n*+ structure was chosen because the electron mobility in InGaAs is much higher than the hole mobility, and hence sheet resistance would be lower in the bottom layer for an *n*+ layer. The structural details of the first growth run, wafer 338C, are listed in Table 3.2. A high Si doping density of 1.5 x 10^{20} cm^{-3} was targeted using delta doping. To reach this density, the 10 nm *n*+ side of the junction was grown with a flux to achieve 5 x 10^{19} cm^{-3}; every 1 nm the growth was interrupted to obtain ten delta doping spikes at the 10^{13} cm^{-2} level.

Table 3.2

Structural of $In_{0.53}Ga_{0.47}As$ tunnel-structure 338C

nm	type	dopant	density (cm^{-3})
50	*p+*	C	1 x 10^{19}
10	*p+*	C	1 x 10^{20}
3	*i*		
10	*n+*	Si	1.5 x 10^{20}
300	*n+*	Si	1 x 10^{19}
Semi-insulating InP substrate			

The C and Si profiles in this structure were measured by SIMS, courtesy S. Corcoran of Intel Corporation, Fig. 3.1(a). A peak concentration of 1.6 x 10^{20} cm^{-3} was

achieved for C, while ~10^{20} cm^{-3} was obtained for Si, close to the solid solubility for both C and Si.

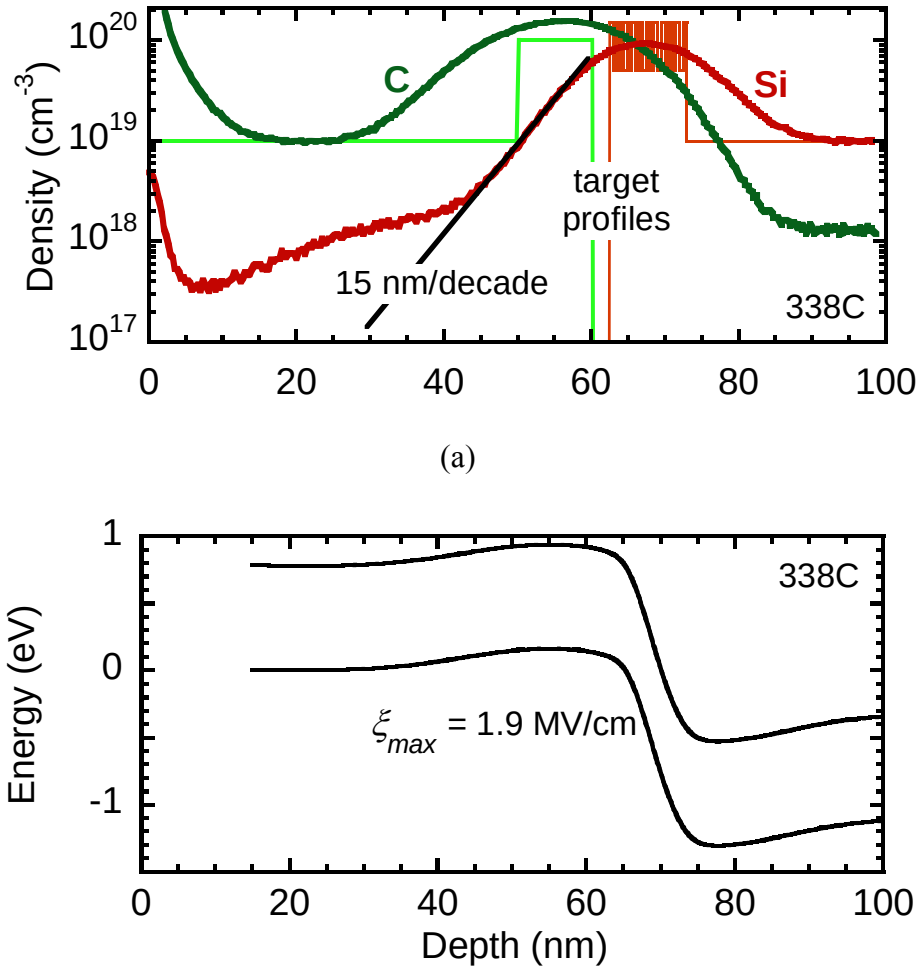


Figure 3.1 (a) SIMS measurements of C and Si in $In_{0.53}Ga_{0.47}As$ tunneling structure 338C, and (b) the simulated band-diagram of structure 338C using the measured SIMS profiles, calculated using BandProf. The Fermi-level is located at zero energy. The first 15 nm of the SIMS data was ignored for the simulation since the high C density in this region is likely a SIMS artifact.

The first 10-15 nm of the SIMS data shows dopant densities that are much higher than the designed densities. This is likely an artifact of the SIMS measurement, since a

steady-state sputter rate may not have been attained in this shallow region. The data shows that the dopants have diffused at the junction resulting in profile slopes that are poorer than prior reported results (Mensa at UCSB [55]). The maximum dopant slope seen for the Si profile is 15 nm/decade compared to ~5 nm/decade observed by Mensa. An unexpectedly high concentration of C is measured in the Si-doped region, which is generally not observed. Origins of the anomalous C concentration could be a C memory effect in MBE, an increase in C solubility in heavily *n*-doped InGaAs, a SIMS artifact due to crater roughness in heavily doped InGaAs, or diffusion of C into the Si-doped layer.

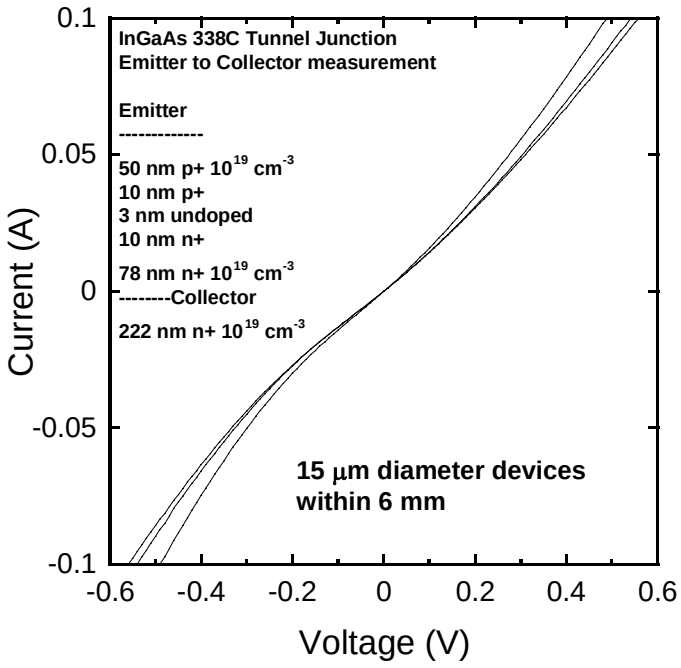
Band diagram simulation of structure 338C using the SIMS C and Si profiles shows that a tunnel junction is expected in this wafer, with a maximum field of 1.9 MV/cm, Fig. 3.1(b). The first 15 nm has been ignored for the simulation since the high C density is likely a SIMS artifact and the conclusions are not affected if this data is excluded. Due to the dopant diffusion which occurred in wafer 338C, the expected junction field is much lower than the field calculated for an abrupt junction, 2.9 MV/cm, obtained using BandProf for the designed structure.

3.3 $In_{0.53}Ga_{0.47}As$ *p*+ on *n*+ TD fabrication and characterization

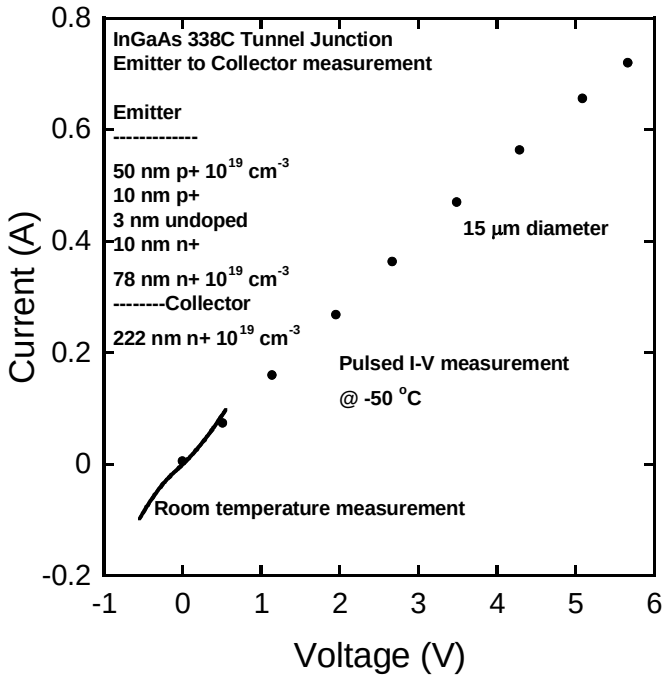
Diodes were fabricated on structure 338C, Table 3.2, using a two-mask process with nonalloyed ohmic contacts deposited on the top *p*+ emitter layer ($p = 10^{19}$ cm^{-3}) and the bottom *n*+ collector layer ($n = 10^{19}$ cm^{-3}). The emitter contact was formed using a lift-off process using electron-beam evaporation of a Pd/Ti/Pd/Au (10/40/40/240 nm) layer.

The Pd/Ti/Pd/Au metallization has been shown by Chor *et al*. [56] to be preferable to Ti/Pt/Au contacts for *p*+ InGaAs owing to lower contact resistivity. A mesa of approximately 150 nm was formed by wet etch in 1 H_2SO_4: 8 H_2O_2: 160 H_2O which etches InGaAs at 5 nm/s. Finally a Ti/Pt/Au 10/10/200 nm collector contact was formed using lift-process and e-beam evaporation. The process traveler is given in Appendix III.

The measured *I-V* characteristics of this heavily-doped InGaAs tunnel junction are shown in Fig. 3.2(a), where three 15 μm diameter devices spanning a 6 mm length were measured to the current limit of the Agilent 4155C semiconductor parameter analyzer (SPA) corresponding to a current density of 0.6 mA/μm^2 at a voltage of approximately 0.5 V. A symmetric *I-V* characteristic is observed without any indication of NDR in the positive bias region, which is the forward bias region of the diodes. To look for NDR at higher current densities without causing junction burn-out, pulsed *I-V* measurements were made using the Tektronix 370A curve tracer, at −50 ºC. Shown in Fig. 3.2(b) is the *I-V* characteristic of a 15 μm diameter device where voltage pulses were applied and the current measured. No NDR was observed up to a current density of 4 mA/μm^2 at a voltage of 5.7 V. A possibility for absence of NDR is the presence of high density of traps in the junction depletion layer leading to excess current, which occurs via tunneling through these states.



(a)

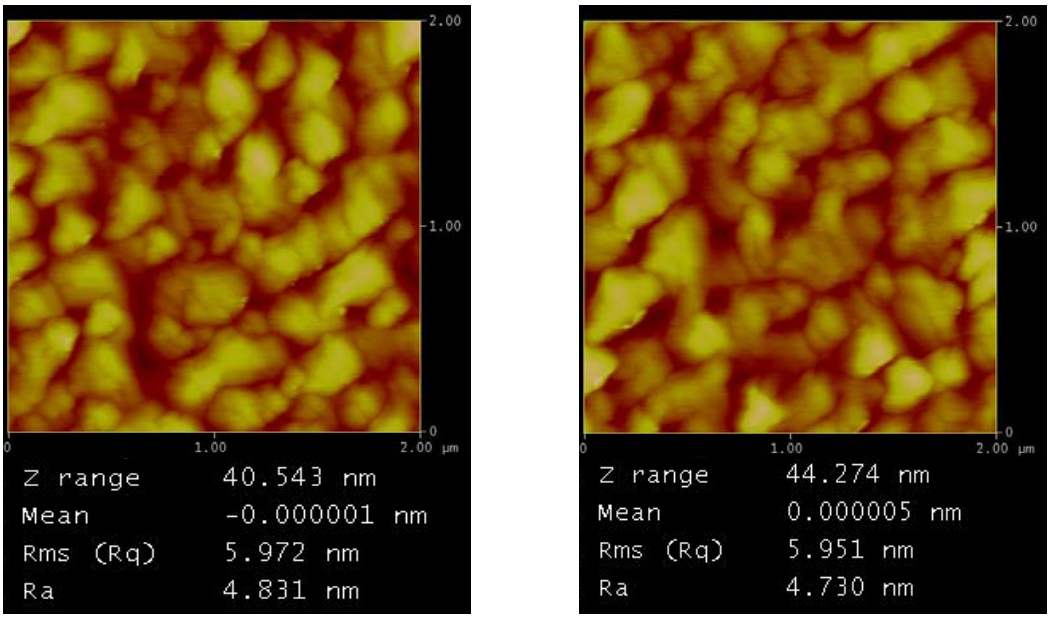


(b)

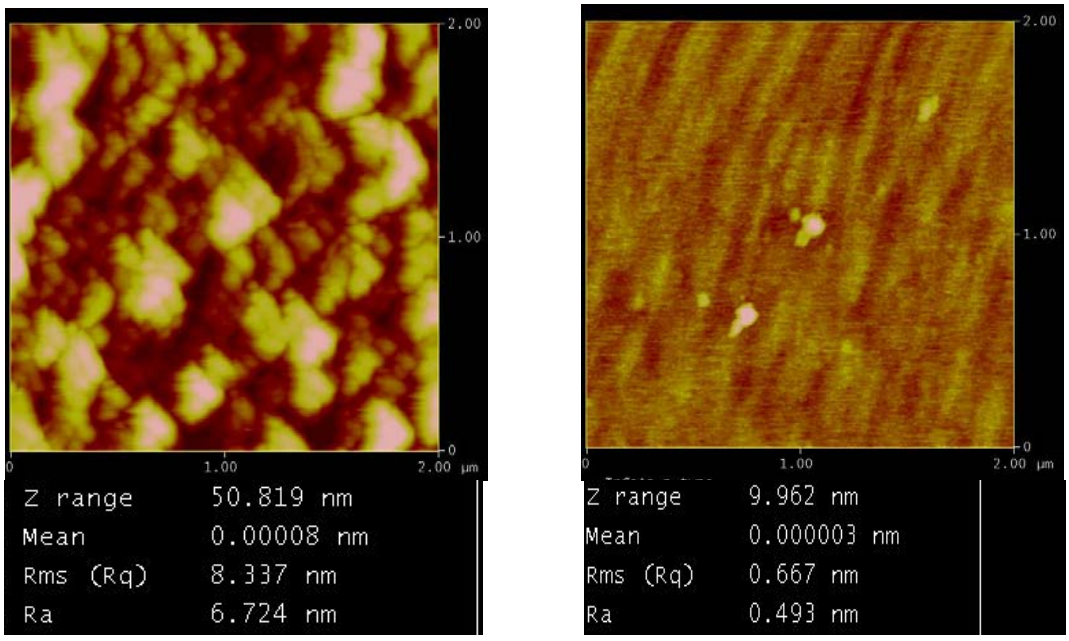
Figure 3.2 Measured *I-V* characteristic of $In_{0.53}Ga_{0.47}As$ tunnel structure 338C, (a) measured at room temperature to a current of 100 mA and (b) pulsed *I-V* measurements of the same junction at -50 ºC compared against the SPA measurements.

Structure 338C, has an rms surface roughness of ~6 nm, measured using atomic force microscopy (AFM), Fig. 3.3(a). To understand whether this roughness arises from the heavy *n*-doping or from the *p*-doping, AFM scans were taken of doping calibration wafers: *n*+ Si-doped InGaAs wafer 329C and C-doped InGaAs wafer 305C, Fig. 3.3 (b) and (c), respectively. The AFM scans reveal that the Si-doped InGaAs has the higher average surface roughness of 6.7 nm, while the C-doped $In_{0.53}Ga_{0.47}As$ has a roughness of only 0.5 nm. These results suggest that the surface roughness seen in 338C originates from the heavy Si doping.

Freundlich *et al*. [57] comment that $In_{0.53}Ga_{0.47}As$ tunnel junctions grown with either the *pn* or *np* configuration gave similar results. In their work the maximum Si concentration used was 1-2 x 10^{19} cm^{-3} and the maximum peak current density observed was 0.01 $mA/\mu m^2$. Ono *et al*. [58] obtained tunnel junctions growing a Si doped *n*+ layer first and obtained a peak current density of 0.08 $mA/\mu m^2$ and a PVR of 8 using a Si density of 10^{19} cm^{-3}. Neither Freundlich *et al*., nor Ono *et al*. report the surface roughness of their structures. Therefore, in *p* on *n* structures, Si densities of up to 1-2 x 10^{19} cm^{-3} are known to exhibit NDR. In growth 338C, doping densities were nearly ten times higher.



(a)



(b) (c)

Figure 3.3 Atomic force microscopy images of (a) the *p*+ surface of $In_{0.53}Ga_{0.47}As$ wafer 338C taken at two spots 20 µm apart, (b) *n*+ Si-doped $In_{0.53}Ga_{0.47}As$ wafer 329C, and (c) *p*+ C-doped $In_{0.53}Ga_{0.47}As$ wafer 305C.

In summary, an InGaAs *p*+ on *n*+ tunnel diode (structure 338C) was grown with dopants approaching the solubility limits on both sides of the junction. Measured atomic profiles by SIMS show C and Si dopant slopes of 10 and 15 nm/decade, and higher background concentrations for C and Si than are typical for dopant profiles in InGaAs grown by MBE [55]. The simulated band profiles show junction fields should be less than 1.9 MV/cm and tunneling width of approximately 4.8 nm compared to the designed values of 2.9 MV/cm and 3 nm assuming abrupt doping profiles. The absence of NDR and the weak temperature dependence between 300 and 250 K could result from a large trap-assisted excess current in the junction, but might also result from other causes like interface roughness, or nonuniformities in the electrical activation giving rise to a spatially-dependent junction field, or dopant spikes which might manifest themselves by a high apparent background concentration.

3.4 $In_{0.53}Ga_{0.47}As$ *n*+ on *p*+ tunnel structures

In the next set of structures grown, it was of interest to determine if steeper C and Si profiles were possible at dopant densities lower than that used in 338C (~10^{20} cm^{-3}). Junctions with lower C and Si densities would also confirm the formation of a tunnel junction via observation of an NDR. In these growths, the doping order was reversed so that the smoother *p*+ layer growth would take place first followed by *n*+ and a smoother junction interface might be obtained.

A set of six structures with C densities of 5 and 10 x 10^{19} cm^{-3} and Si densities of 1 to 15 x 10^{19} cm^{-3}, see Table 3.3, were grown. In growths 480C and 483C, the high Si

concentration was obtained by using 10 delta-doping spikes of 10^{13} cm^{-2} with 1 nanometer separation between spikes, all with a background flux which yields a Si concentration of 5 x 10^{19} cm^{-3}.

Table 3.3

Layer description for a set of six $In_{0.53}Ga_{0.47}As$ tunnel junctions: (a) layer thicknesses and common dopings and (b) C and Si doping variations vs. growth number.

nm	type	dopant	density (cm^{-3})
40	*n+*	Si	1 x 10^{19}
10	*n+*	Si	N_D
3			
10	*p+*	C	N_A
10	*p+*	C	1 x 10^{19}
500	*p+*	Be	1 x 10^{19}
Semi-insulating InP substrate			

(a)

	x10^{19} cm^{-3}		
Growth	N_a	N_d	N_{eff}
477	5	1	0.83
479	5	5	2.50
480*	5	15	3.75
481	10	2	1.67
482	10	5	3.33
483*	10	15	6.00

(b)

*Si doping density: 5 x 10^{19} cm^{-3} plus a δ-doping of approximately 10^{13} cm^{-2} every 1 nm for 10 nm for an integrated doping density of 15 x 10^{19} cm^{-3}

3.5 SIMS characterization of C and Si in heavily doped $In_{0.53}Ga_{0.47}As$ structures

The C and Si profiles in the *n*+*p*+ structures of Table 3.3 were measured by SIMS [59]. Figure 3.4 shows the target locations of C and Si profiles in each wafer, and the corresponding SIMS profiles. Maximum C dopant slopes of 2.1-6.2 nm/decade were observed in the SIMS profiles, comparable to the slopes seen by Mensa, ~5 nm/decade [55].

Wafer 477C broke during the SIMS preparation at Intel and was held together by a C-containing glue for SIMS analysis. The elevated background C levels in this wafer

may result from this glue. The minimum background C level in 477C is ~3.5 x 10^{18} cm^{-3} compared to 4-5 x 10^{17} cm^{-3} in the other wafers.

As is the case in wafer 338C, the C concentration in the Si-doped regions is higher than expected, generally not observed in heterojunction bipolar transistors, where the overlying *n*-InGaAs layer is lightly doped. This could indicate that the solubility of C is increased in heavily-doped InGaAs, or an enhanced diffusion of C in heavily Si-doped InGaAs, however other factors may be responsible e.g. residual C in the growth system or a SIMS artifact e.g. roughness of the etch crater or anomalous change in etch rate during profiling.

3.6 Band-diagram simulations of $In_{0.53}Ga_{0.47}As$ tunneling structures

The current density is a function of the junction field, which in structures 477C-483C were obtained from band diagram simulations performed using BandProf utilizing the exact SIMS profiles of C and S, Figs. 3.5 (a) and (b). The simulation results show that junction electric fields in range 1.1 to 2.4 MV/cm can be expected. Tunneling-current densities in the range 1 mA/μm^2 to 50 mA/μm^2 are predicted for these fields for a reverse bias of 1 V, see Fig 2.4.

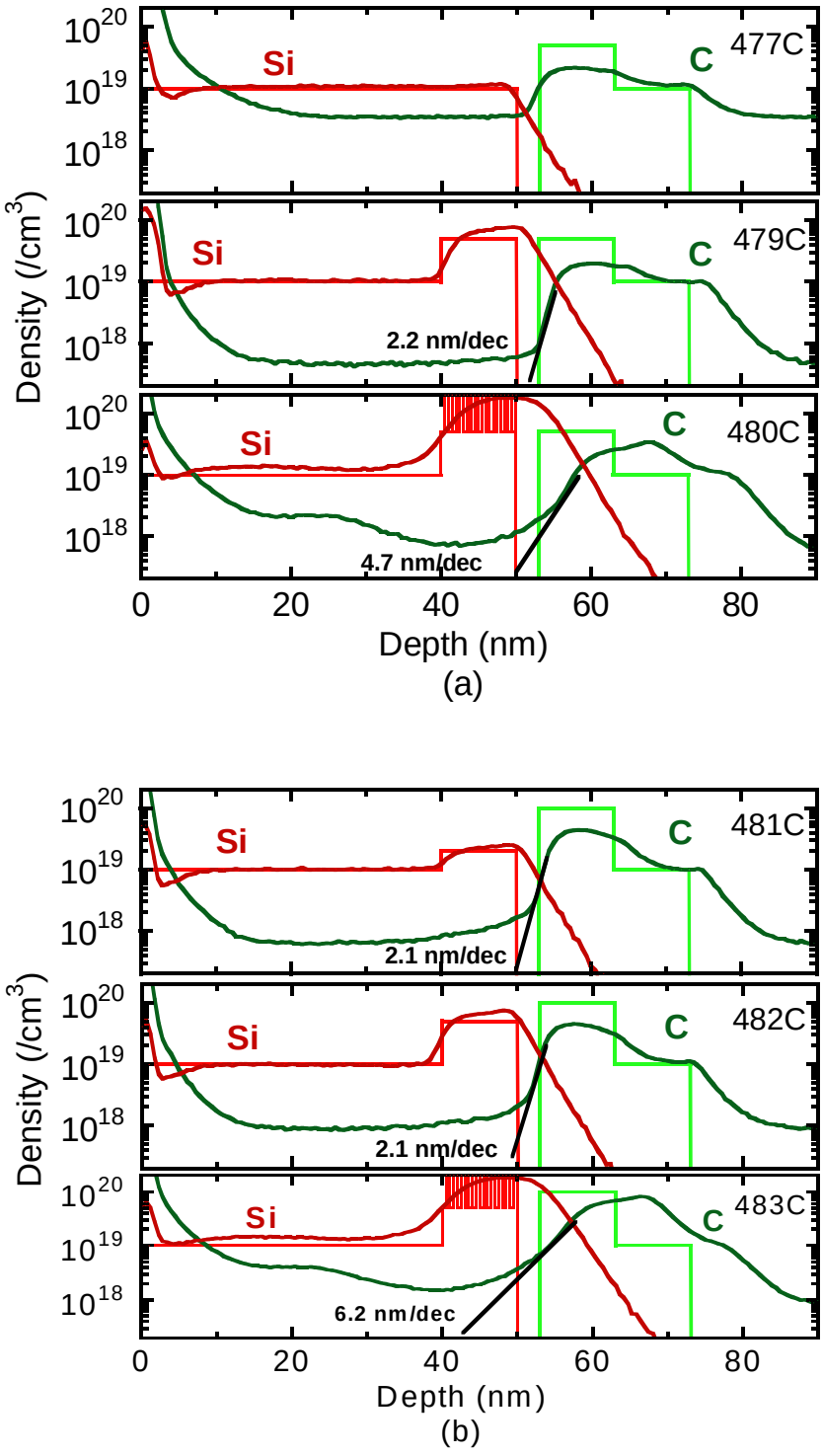


Figure 3.4 Dopant profiles of C and Si in $In_{0.53}Ga_{0.47}As$ tunnel structures (a) 477C-480C and, (b) 481C-483C, overlaid on the target dopant profiles.

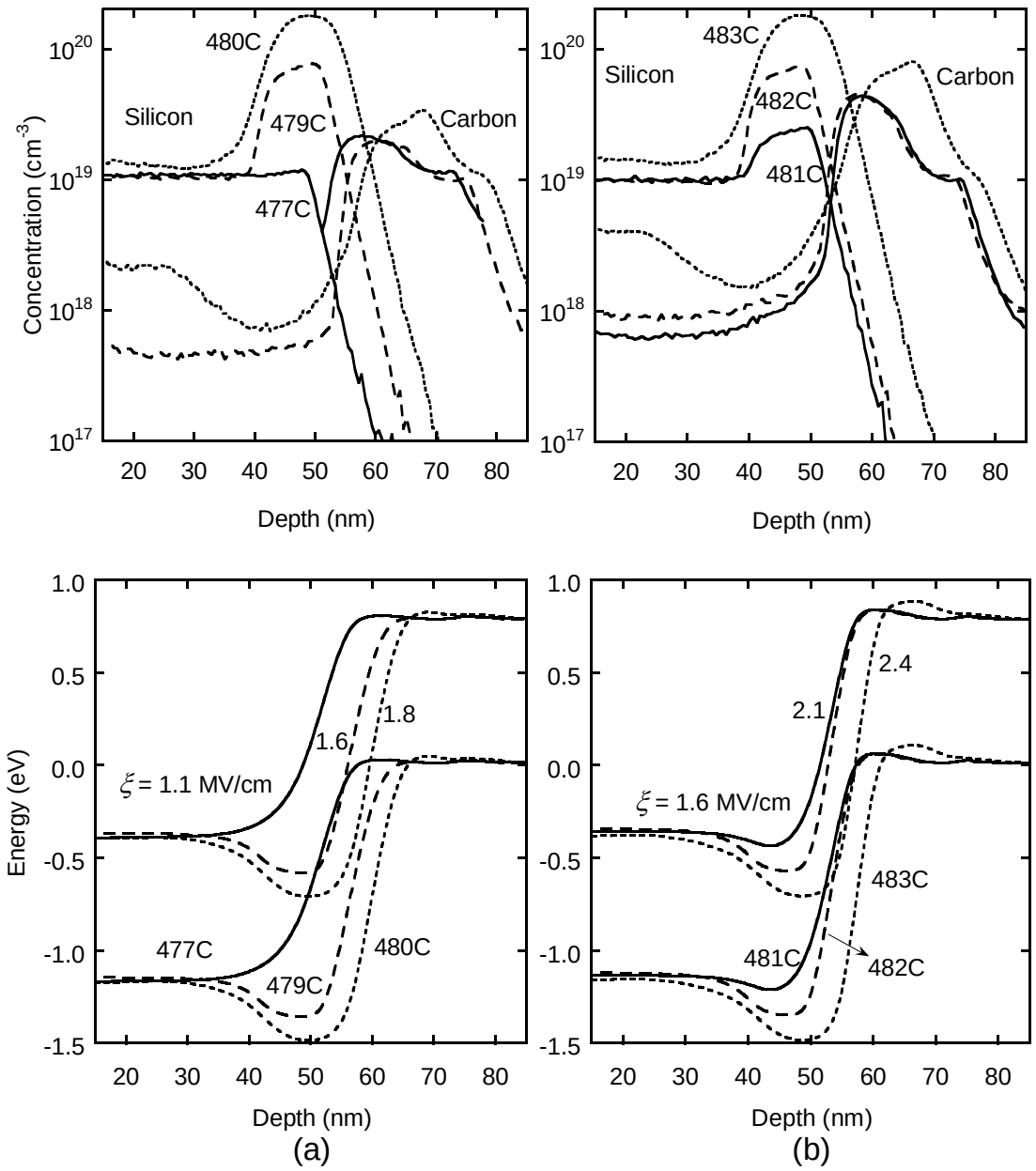
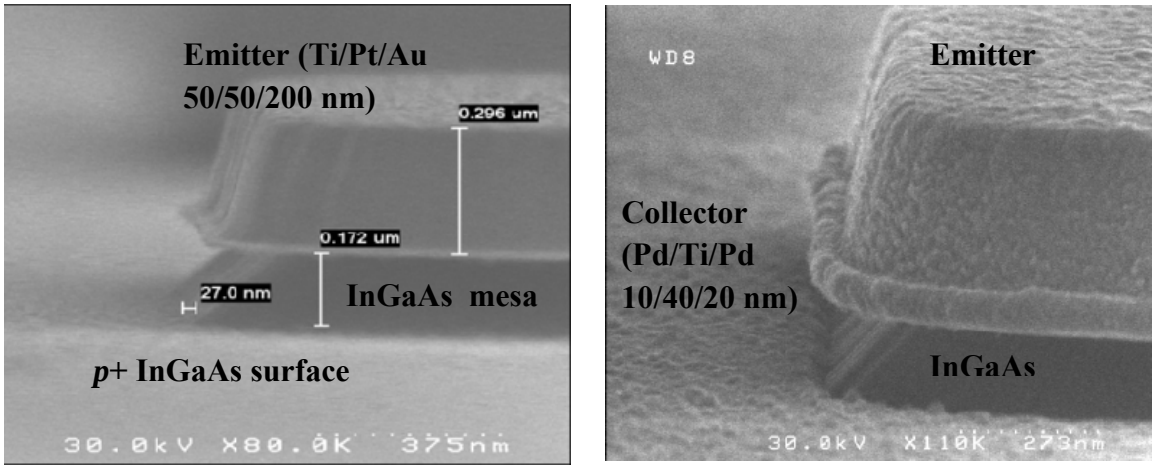


Figure 3.5 Simulated band diagrams of $In_{0.53}Ga_{0.47}As$ tunneling structures (a) 477C-480C, and (b) 481C-483C, calculated using SIMS profiles of C and Si shown above the respective band diagrams. The band diagrams are simulated using BandProf [32]. The maximum field, ξ, in each wafer is listed alongside the band diagram.

3.7 $In_{0.53}Ga_{0.47}As$ *n*+ on *p*+ TD fabrication and characterization

In the *n*+ on *p*+ structures, the collector layer is formed on the bottom *p*+ layer which has a low hole mobility of 30-50 cm^2/Vs [52] at the concentrations used in this work. To minimize access resistance in the device arising from the collector layer, a self-aligned collector contact process was used. In short, an electron-beam evaporated Ti/Pt/Au (50/50/200 nm) emitter contact was formed by a lift-off process followed by a wet etch of $In_{0.53}Ga_{0.47}As$ in $1H_2SO_4$: $8H_2O_2$: $160H_2O$ to form a 170 nm high mesa. The collector contact was then formed by e-beam evaporation of Pd/Ti/Pd (20/40/20 nm) at normal incidence. Scanning electron microscope (SEM) images of the diode structure prior to deposition of the collector, and after deposition, are shown in Fig. 3.6(a) and Fig. 3.6(b). The images show the self-alignment of collector and emitter metallization. The full process description is given in Appendix IV.



(a) (b)

Figure 3.6 Scanning electron microscope images of the self-aligned $In_{0.53}Ga_{0.47}As$ tunnel diode mesas, (a) before, and (b) after collector metal evaporation.

The *I-V* characteristics of the InGaAs junctions were measured using an HP4155 semiconductor parameter analyzer (SPA), Fig. 3.7, using a double voltage sweep, where the voltage was swept from -1 V in the reverse bias to forward bias, and back. In the reverse direction, a current density of up to 1.5 mA/μm^2 has been measured in these junctions. In the forward direction, the wafers 477C, 479C, 480C, and 481C show an NDR. A hysteresis is observed in the *I-V* characteristic of 481C in forward bias when using the double voltage sweep. This occurs because the series resistance in 481C results in bistability, which causes different *I-V* paths to be traced in the forward and reverse sweep directions. In wafer 480C, increasing the Si doping in 480C by 10 x 10^{19} cm^{-3} did not result in a higher peak current density. This suggests that the active Si density in 480C and 479C are similar. The current density did not increase in wafer 483C as well, compared to 482C, when the Si density was increased by 10 x 10^{19} cm^{-3}. Possibly as the Si concentration as increased, formation of Si clusters, Si-defect complexes, or Si being incorporated as an acceptor result in lowered *n*-type density.

One can estimate the upper limit on the series resistance from the *I-V* characteristics by assuming that the post-valley current is exponential, since the thermionic current and excess current are known to be exponential in nature. The maximum resistances thus obtained from the *I-V* characteristics of 5 x 5 μm^2 devices is 12 Ω in 477C, 9 Ω in 479C-481C, of which the contribution of probe resistance was 2-3 Ω. Now a calculation is made for the expected resistance in these devices after accounting for the contact resistance and probe resistance. The contact resistance of Ti/Pt/Au contacts on *n*+ $In_{0.53}Ga_{0.47}As$ was measured using the transmission line method. The *n*+ layer had a concentration of 10^{19} cm^{-3} and a thickness of 220 nm, with

semi-insulating InP below. A contact resistivity of 1.3 x 10^{-6} Ωcm^2 and sheet resistance of 3.8 Ω was measured. Based on these results, the contact resistance for a 5 x 5 μm^2 device is ~5 Ω. After accounting for a probe resistance of 2-3 Ω, the expected resistance is therefore 7-8 Ω, which indicates that the series resistance seen in the measurements is essentially due to the contact resistance.

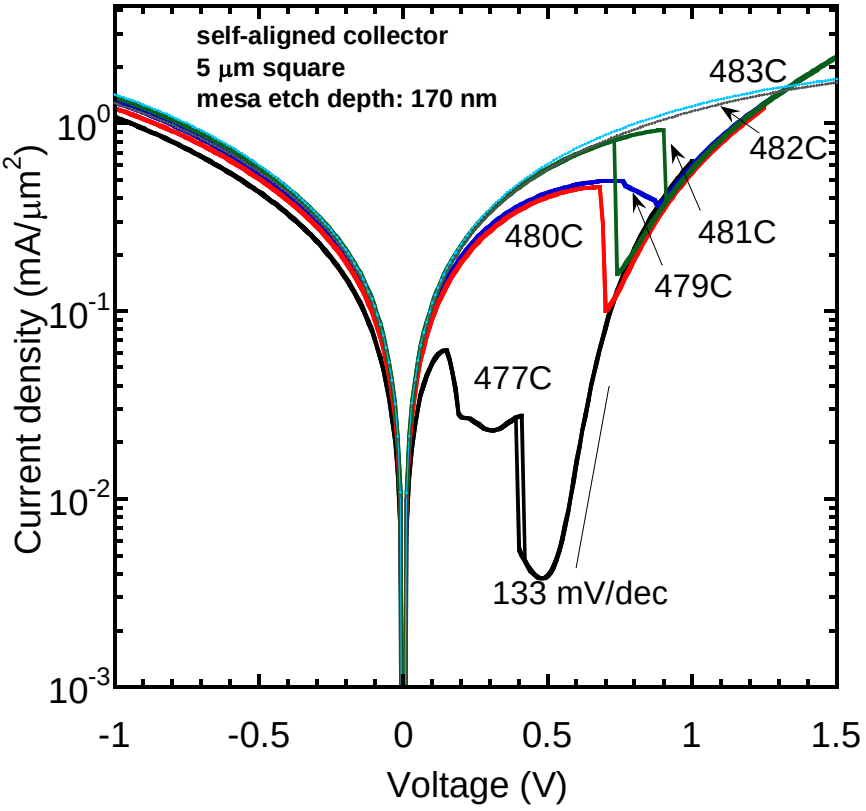


Figure 3.7 Measured *I-V* characteristics of 5 x 5 μm^2 square devices in $In_{0.53}Ga_{0.47}As$ tunnel structures 477C-483C.

An NDR region is not observed in the wafers with the highest doping densities, 482C and 483C. The absence of NDR in these samples could be due to excess current through states in the bandgap rising from defects at the junction. Another possible reason is that a variation in tunneling width occurs across the junction interface, causing the

local *I-V* characteristic to vary across the junction. This could cause the NDR to disappear when the sum of these varied local *I-V* is measured. The reasons for varying tunneling widths could be a rough junction, or lateral nonuniformity in the doping density or impurity activation. Low temperature *I-V* measurements of wafer 483C reveal an NDR at 4.2 K, Fig. 3.8, which is believed to be due to tightening of the Fermi distribution of carriers at lower temperature which increase the current density.

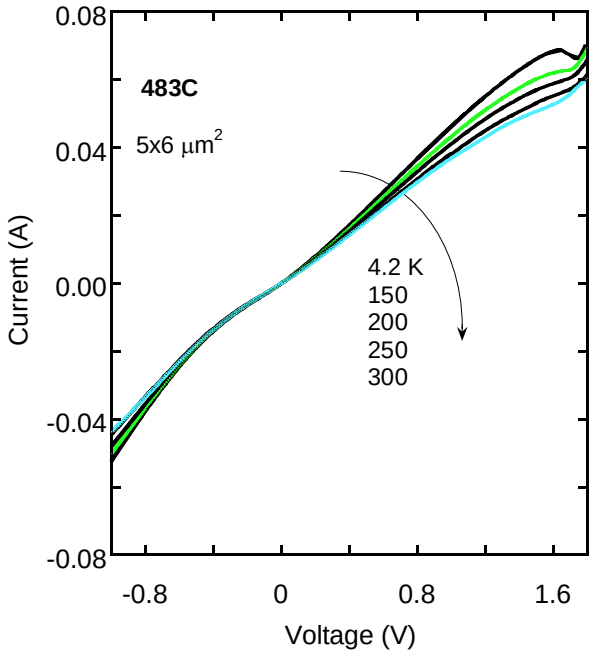


Figure 3.8 Temperature dependence of the *I-V* characteristics of $In_{0.53}Ga_{0.47}As$ tunnel diode wafer 483C showing NDR at 4.2 K.

3.8 Reverse current behavior as function of tunneling barrier width

Tunneling current can be expressed as an exponential function of the tunneling width, $J_o \exp(-w/\lambda)$ [60], where J_o is the extrapolated current at zero tunneling width, and λ is an attenuation length, and w is the tunneling width. Solomon, *et al.* [60]

determined the parameters J_o and λ for reverse-biased Si *pn* junctions (J_o = 5.3 x 10^7 A/cm^2, and λ = 0.38 nm), by obtaining tunneling widths from band diagrams calculated using dopant profiles measured by SIMS and consistent with *C-V* measurements. For InGaAs tunnel junctions, the prefactor J_o and attenuation length were determined from band diagrams calculated using dopant profiles measured by SIMS assuming complete dopant activation.

Since the band diagram is curved, the tunneling width for a given reverse bias is not the same over the entire tunneling window. Solomon calculates an effective tunneling width, w, for a given reverse bias to account for this fact. The current density is then plotted against the effective width to determine the parameters J_o and λ. The tunneling probability is proportional to the exponential of the spatial integral of the k vector, $e^{-2\int kx}$. Solomon defines the term $\int kx$ as the action integral, ϕ. To determine an effective width for a given reverse bias, the minimum tunneling width w_T at that bias is multiplied by a correction factor which is the ratio of the action integral of the real band diagram, and that of the uniform field case, ϕ_F. The effective width is therefore given by,

$$w = w_T(\phi/\phi_F) \tag{3.1}$$

For a given reverse bias, the potential corresponding to the minimum barrier width in the junction is called V_i, the position corresponding to this potential on the conduction band is x_c, and on the valence band is x_v, Fig. 3.9. Tunneling is assumed to

occur by electron tunneling from point x_c to a point x_p, assumed to be the mid-gap position, and recombining with a hole which tunnels from x_v to x_p.

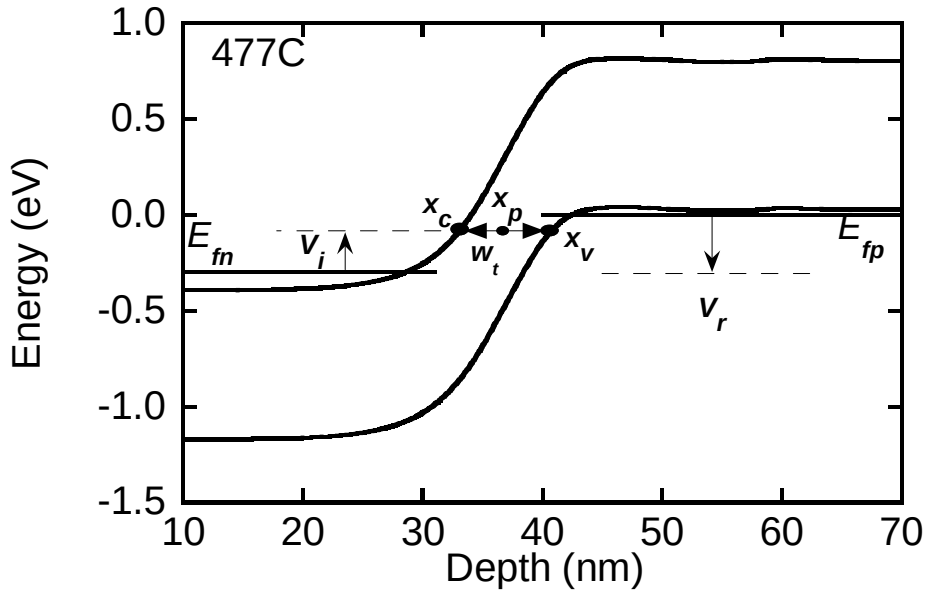


Figure 3.9 Band diagram of InGaAs tunnel junction 477C, calculated at a reverse bias of 300 mV. For the reverse bias V_r, shown is the minimum barrier width w_t, between the tunneling points x_c and x_v, the voltage corresponding to this minimum width, V_i, and the position corresponding to mid-bandgap point along the tunneling path, x_p.

The action integral for a potential distribution $V(x)$ is then given by [60],

$$\phi = \frac{1}{\hbar}\left\{\int_{x_c}^{x_p} \sqrt{2qm_e^*(V(x)-V_i)}dx + \int_{x_p}^{x_v} \sqrt{2qm_h^*(E_g+V_i-V(x))}dx\right\} \tag{3.2}$$

where m_e^* and m_h^* are the electron and hole mass respectively. The action integral for a uniform field is given by [60],

$$\phi_F = \frac{2}{3\hbar}\sqrt{qm^* E_g} w_T \tag{3.3}$$

where w_T is the minimum tunneling barrier width for a given reverse bias, and m^* is the effective mass of electrons or holes, assumed to be equal by Solomon, and here as well, since the electron and hole masses are similar in InGaAs, 0.041 and 0.052, respectively [26].

For the InGaAs tunnel junctions, the correction factor for a given reverse bias was obtained by determining the action integrals from band diagrams calculated using the measured SIMS profiles, assuming complete activation. The correction factors thus obtained for wafers 477C-481C are shown in Fig. 3.10, which shows that in these wafers, the correction factor is nearly one at all reverse biases.

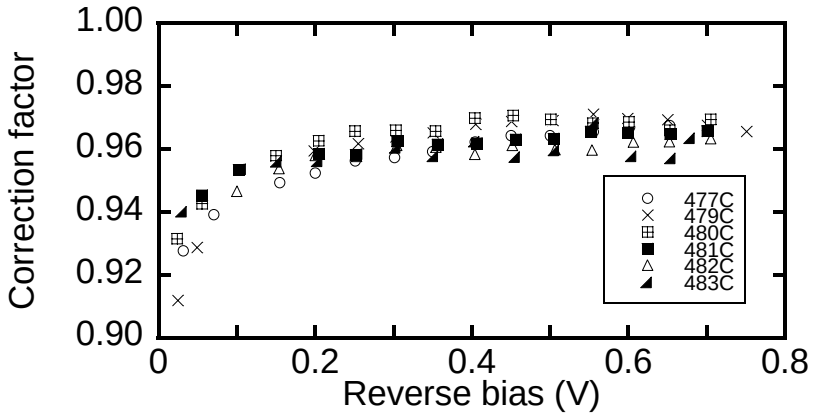


Figure 3.10 Correction factor for the calculation of effective tunneling barrier width, as a function of reverse bias for junctions 477C-483C. The effective barrier width in the case of curved bands is obtained by reducing the tunneling width in the case of uniform field by the correction factor.

It is now useful to consider what theory predicts for current density vs barrier width for the InGaAs tunnel junctions fabricated in this work. Tunneling current density can be expressed as a function of the tunneling barrier width by assuming that the maximum electric field in the junction is approximately $\xi_{max} = E_g/w$ in Eq. (2.1).

$$J = \frac{\sqrt{2m_r^*}q^3(E_g/w)V_R}{8\pi^2\hbar^2 E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m_r^*}E_g^{\frac{3}{2}}}{3q(E_g/w)\hbar}\right). \tag{3.4}$$

The electric field can be calculated from the doping densities in the junction, Eq. (2.3), and the barrier width can be found from the electric field as listed above, $w = E_g/\xi_{max}$. If one assumes constant electric field over the tunneling window, then w is constant over the tunneling window as well. The current density is plotted against the barrier width w, in Fig. 3.11. However, a deviation from the exponential behavior is seen at certain widths. Also, the current density vs barrier width relation is not unified for all the wafers as Solomon observed for Si. This is because there is a voltage term in the prefactor which differs across the wafers for the same tunneling width. Depending on the doping densities used, different reverse biases must be applied in the different wafers, to obtain the same tunneling width. Solomon does note that one should see voltage dependence in the current density versus barrier thickness, but that it was not observed in their work. If one examines J/V_R vs tunneling width, however, it is seen that all the wafers have the same exponential dependence on tunneling width (at low biases), Fig. 3.12.

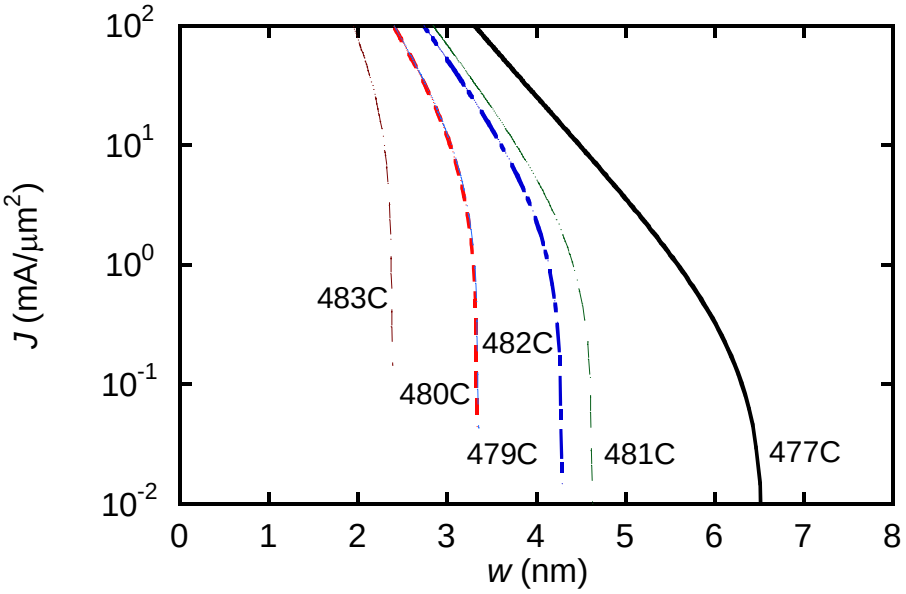


Figure 3.11 Current density as a function of tunneling barrier width as predicted theoretically for InGaAs wafers 477C-481C. The calculations are made using the expression for reverse current density given by Eq. (3.4).

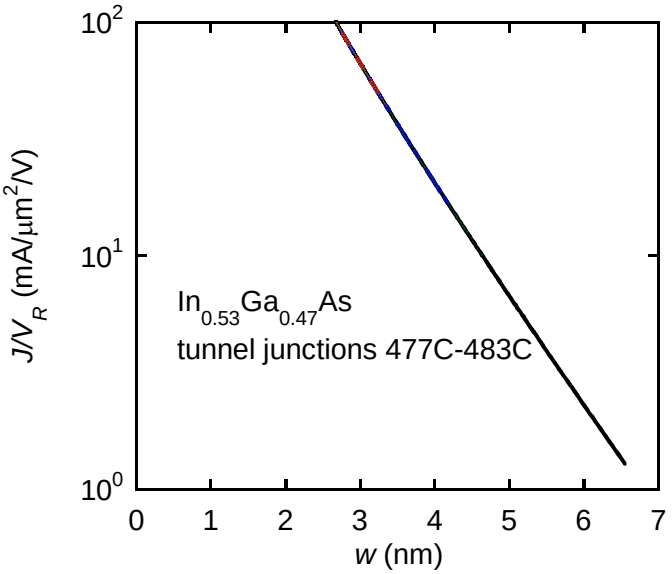


Figure 3.12 Current density per unit reverse bias voltage as a function of tunneling barrier width as predicted theoretically for InGaAs wafers 477C-481C showing a unified tunneling behavior. The calculations are made using the expression for reverse current density given by Eq. (3.4).

The current density for different reverse biases is plotted against the corresponding effective tunneling width for InGaAs wafers 477C-483C, Fig. 3.13. The series resistance is taken into account for this calculation as 12 Ω in 477C and 9 Ω in the remaining wafers, as explained in section 3.7. From Fig. 3.13, it is observed that in wafers 477C-481C, current density has an exponential dependence on w over a range of barrier widths. Extraction of J_o for zero tunneling barrier width gives 0.7 to 7 x 10^7 A/cm^2. An attenuation length of 0.41 to 0.86 nm is observed. At higher widths, or low reverse biases, the current density deviates from the exponential dependence, as predicted by theory. Also, the exponential dependence is not the same for all the wafers as was observed for Si by Solomon, but agrees with the theoretical analysis of InGaAs junctions presented previously.

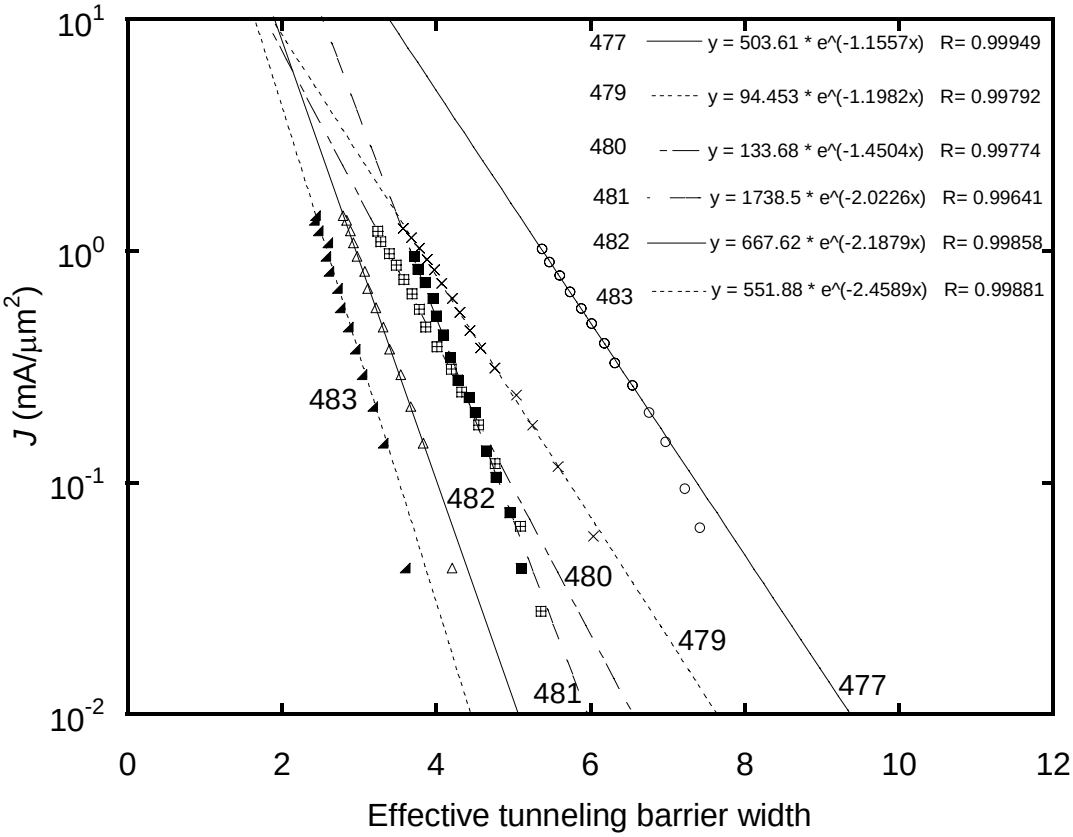


Figure 3.13 Current density as a function of effective tunneling barrier width in InGaAs wafers 477C-481C.

From theory one expects a unified behavior for J/V_R versus tunneling width. All wafers show an exponential region with a value of J_o/V_R of 4.8 to 12.71 mA/μm^2. An attenuation length of 2.5 to 3.3 nm is seen wafers 477C-481C. In fact the attenuation length in wafers 477C, 480C and 481C is in the range 2.5 to 2.6 nm, with only 479C having a higher value of 3.3 nm. In wafers 482C and 483C, the attenuation lengths of 1.6 and 1.5 nm seen are significantly lower than in 477C-481C, which suggests an increased effective mass or band gap in 482C and 483C. Since one expects the band gap to

decrease with increasing doping density, an increased effective mass is the more likely reason.

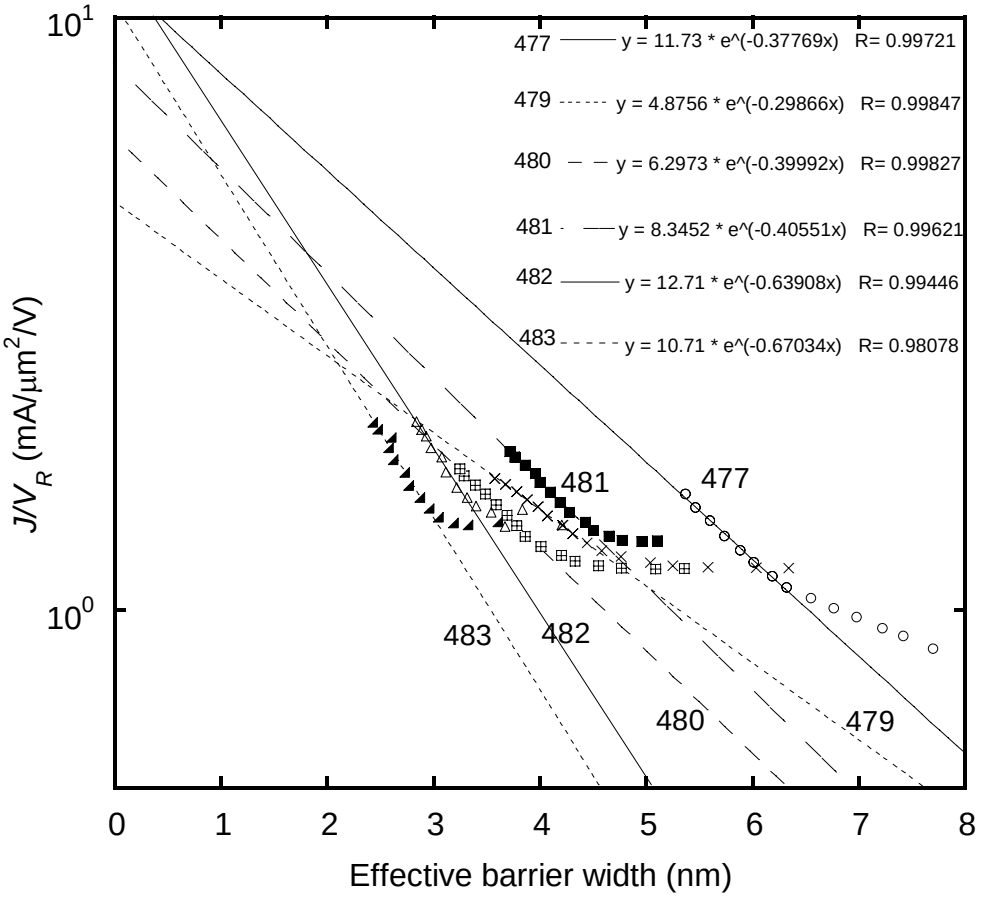


Figure 3.14 Current density per unit reverse bias as a function of tunneling barrier width for InGaAs wafers 477C-481C.

At low biases, or high barrier widths, J/V_R does not have an exponential dependence on tunneling width, and higher current than predicted by the tunneling equation is seen. The reason for this could be that at low reverse bias, an additional path of current such as trap-assisted current may exist in these junctions. Hurkx *et al*. [61]

notes that in the case of Si, tunneling dominates at high reverse biases while trap-assisted tunneling dominates at lower reverse biases.

In this chapter, the effect of C and Si doping density on the electrical behavior on InGaAs $p+n+$ junctions has been investigated. Carbon profiles with ~2 nm/decade slopes are achieved, comparable to the best seen in literature. In the forward direction, the highest peak current density observed was 0.94 mA/μm^2 at room temperature, while a peak current density of 2.3 mA/μm^2 was measured at 4.2 K in the heaviest doped junction. In the reverse direction, tunneling behavior was examined using the tunneling width as a parameter, and the exponential dependence of J_o/V_R on width was determined for the wafers used in this work.

CHAPTER 4. GERMANIUM TUNNEL JUNCTIONS

Germanium tunnel junctions were fabricated using two approaches: (1) rapid melt regrowth of Al-doped *p*+ Ge from an Al metal source into *n*+ Ge and (2) *p*+ Ga doping by diffusion from a Ga metal source into *n*+ Ge. In the first approach the junction is formed by melting back Ge from under a deposited Al contact followed by cooling down to regrow a *p*+ Ge layer doped with Al. The *n*+ side Ge was formed using P implantation at high doses of 0.5 x 10^{16} and 1 x 10^{16} cm^{-2}. In this chapter, the effects of implantation depth and activation anneal on junction *I-V* characteristics are discussed. A peak tunneling current density of 0.27 $mA/\mu m^2$ and PVR of 1.23 is demonstrated in these junctions.

In the second diffusion-based approach, Ga was used as the *p*-type dopant. The *n*+ surface was formed via P implantation, or P diffusion from the spin-on dopant Phosphorosilicafilm 10^{21} from Emulsitone, while the Ga diffusion was performed in Veeco Gen 930 GaN MBE system. The study on Ga diffusion was initiated because the RMR process using the Al-Ge system produces a nonplanar interface with low PVR [22]. Ga with its high solid solubility of 5 x 10^{20} cm^{-3} in Ge is an attractive *p*-type dopant for high current density tunnel junctions.

4.1 *n*+ doping of Ge by P implantation

In recent years there has been interest in implantation doping of Ge [62-65] due to the potential of Ge as high mobility substrate for MOSFETs. The *n*-type dopants that have been studied for Ge are P, As, and Sb [65], of which P has the highest solid solubility of 5 x 10^{20} cm^{-3} [66]. Recently an *n*+ concentration of 4 x 10^{20} cm^{-3} (measured via sheet resistance) was demonstrated using P implantation by Satta *et al*. [63]. The concentration was achieved using a high dose implant of 5 x 10^{15} cm^{-2}, followed by a rapid thermal activation anneal at 500 ºC for 1 s. The *n*+ doping of Ge for the experiments described here also use P implantation and are based on the best-case implant and anneal conditions used by Satta *et al*. [63].

The activation anneal for the P implant was accomplished by RMR for Al doping of Ge. In this process, the *p*+ junction formation and *n*+ implant activation are achieved simultaneously. Four RTA temperatures of 550, 600, 650 and 700 ºC were used for the Al doping of Ge. No cap layer was used for these implants following the implant conditions used by Satta [63]. In this experiment, a Ge wafer was implanted with P and split into pieces that then received the activation anneals. On these wafers no RMR process was performed.

The P profiles expected after anneals at these temperatures were characterized using SIMS, measured by Sean Corcoran of Intel Corporation. From the SIMS data it can be seen that the peak P concentration decreases with temperature after anneal, Fig. 4.1. This is expected since the diffusivity of dopants increases with temperature, causing deeper diffusions at higher temperatures, and a corresponding decrease in the surface

concentration. However, the depth of diffusion after the 600 ºC anneal is lower than the depth after the 500 ºC, the reason for which is presently unknown.

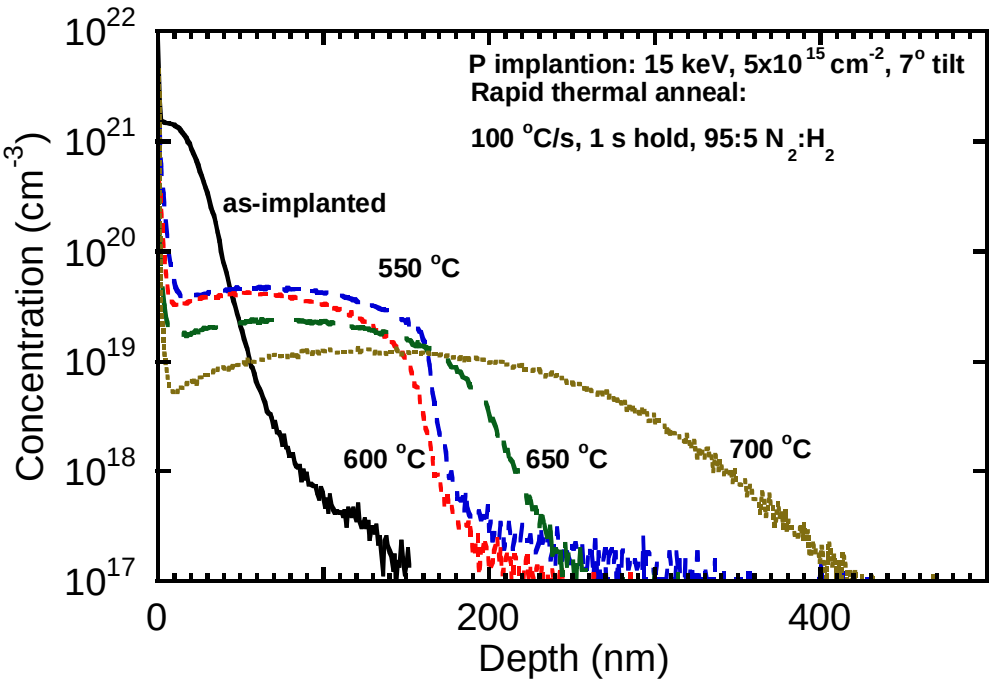


Figure 4.1 SIMS profile of P implants in Ge before and after implant activation anneals.

From the SIMS measurement it was noted that after the P activation anneal a loss of P dose is observed in all the wafers. Figure 4.2 compares the integrated P density of the as-implanted and annealed Ge against the implantation dose. Significantly less P is present than expected. An apparent dose loss of more than 60% results even after the lowest anneal temperature of 500 ºC, and up to 90% loss occurs after the 650 ºC anneal. Dopant loss has been observed after anneals of implants of P in Ge [62, 67], both in capped and uncapped implants [62, 67], using similar anneal temperature ranges of 500 to 800 ºC, anneal times of 1 [62, 67] and 60 s [62, 67] and anneal ambient of N_2. The loss of P is believed to occur by P evaporation at the surface [62, 67].

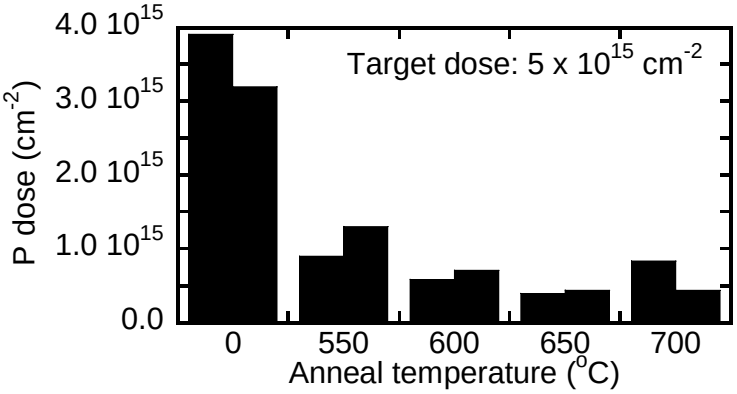


Figure 4.2 Comparison of the integrated P dose from SIMS measurements against the target dose obtained after implantation into Ge at 15 keV, 5 x 10^{15} cm^{-2} and following an activation anneal at temperatures 550, 600, 650 and 750 ºC. Two SIMS profiles were measured on each wafer.

4.2 *n*+ doping of Ge by Phosphorus diffusion from spin-on dopant

In this work, another *n*+ doping approach used was diffusion from the spin-on dopant Phosphorosilicafilm 10^{21} from Emulsitone. In this approach, a Ge substrate was coated with the SOD, and then annealed in an RTP to diffuse the P into the Ge surface.

It is important to know the depths of P diffusion for determining how deep the *p*-type dopant can be incorporated for the formation of the *p*+*n*+ junction. Also, sheet resistance measurements on SOD diffused layers require knowing the depth of the *n*+ layer for estimating concentrations. The junction depth obtained after the P diffusion was determined by differential etch and *I-V* measurements. The P was first diffused into a *p*-substrate following which mesas were etched into the *n*+ layer. The current between two Ge mesas was then measured as a function of mesa etch-depth into the *n*+ layer. The current decreases with increasing etch-depth as the thickness of the *n*+ layer shunting

layer decreases. The current reaches a minimum when the etch depth surpasses the *n*+*p*- junction; this depth is junction depth.

Three wafers were processed with P diffusion times of 3 s, 10 s, and 30 s, which were chosen to determine the dependence of the depth of the P profile, and surface concentration on the diffusion time. A *p*- Ge substrate (10^{17} cm^{-3}) was coated with the SOD and annealed in an RTP600S at 800 ºC, 30 ºC/s, in 95:5 N_2:H_2 flowing at 10 slpm. Ge mesas were fabricated by depositing and patterning Al, followed by RIE in CF_4 etch to form mesas of 150 μm diameter. The results of the differential etch *I-V* measurement are shown in Fig. 4.3. The depth of diffusion after 3 s, 10 s and 30 s was found to be 467, 605 and 700 nm respectively.

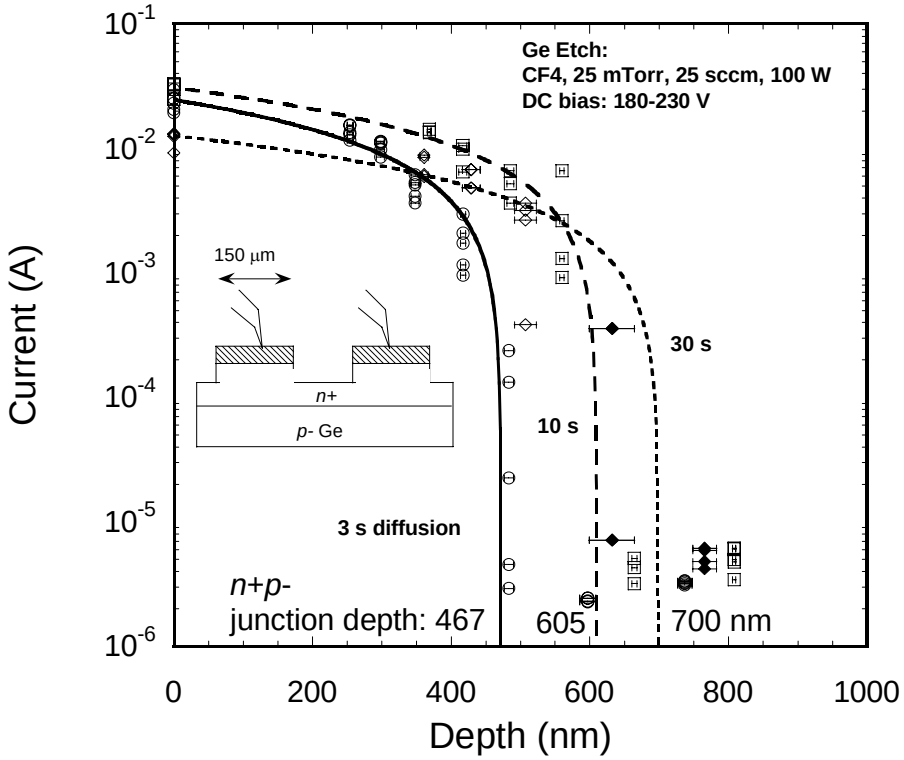


Figure 4.3 Differential etching to estimate junction depth of P-diffused Ge *n*+*p*- junctions. Measured current (at 0.5 V) between two Al contacts (150 μm diameter) vs. etch depth for three different rapid thermal anneal hold times at 800 °C: (a) 3 s, (b) 10 s, and (c) 30 s.

The concentration level obtained after the diffusion was investigated using SIMS, which was also used to confirm the junction depths obtained using the electrical measurements, Fig. 4.4. The *n*+*p*- junction occurs at the substrate concentration of 10^{17} cm^{-3}. The SIMS data is noisy near this concentration level, but extrapolating from the smooth part of the curve, yields junction depths of 410, 515 and 620 nm. The junction depths obtained using electrical characterization is within 18 % of the depths observed from the SIMS measurement.

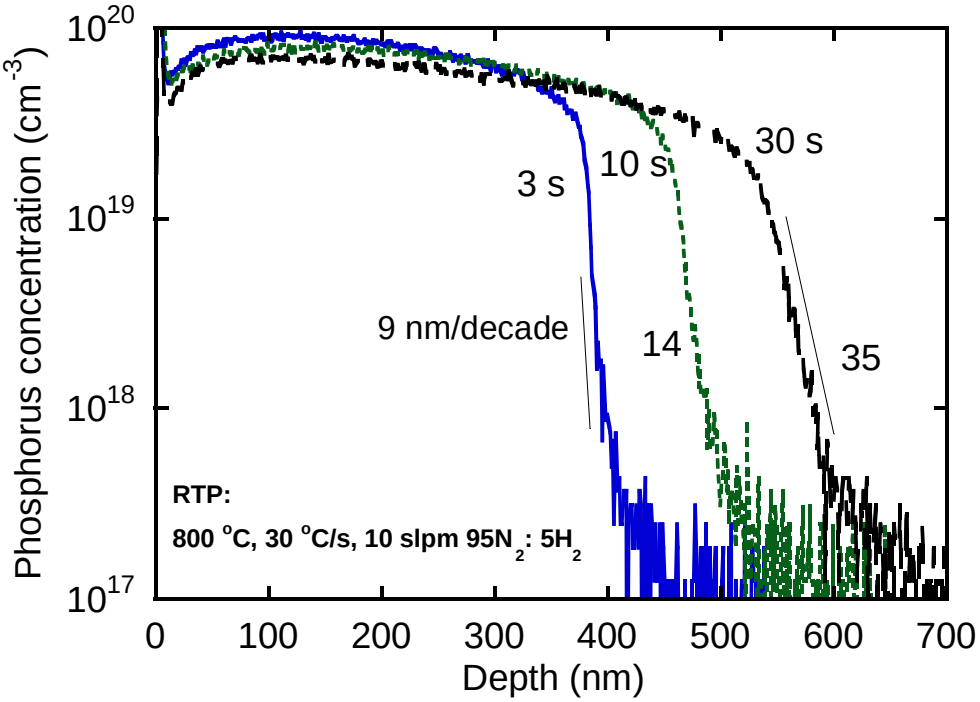


Figure 4.4 SIMS results of P diffused from Emulsitone's spin-on dopant Phosphorosilicafilm 10^{21} cm^{-3}. Shown are the results for three diffusion times of 3 s, 10 s and 30 s. SIMS data courtesy of Brian Doyle and Intel Corporation.

4.3 *p*+ doping by rapid melt regrowth of Al-doped Ge

In RMR, an Al layer is deposited on to an *n*+ Ge surface and then encapsulated in a plasma-deposited SiN_x microcrucible [36]. The SiN_x holds the Al-Ge liquid in place during the rapid melt process, and also suppresses the pooling of Al into islands [36]. By melting and cooling, an Al-doped *p*+ crystalline Ge layer is formed. In this work, the RMR process was used for forming *p*+ layers on top of *n*+ layers formed via ion implantation (II).

During regrowth, a certain thickness of Ge at the surface is melted and doped with Al. The *n*+ layer remaining after regrowth must be thick enough to accommodate the *n*-side depletion width to form the *p*+*n*+ junction. The Ge melt-back thickness consumed for the *p*+ layer formation can be calculated from the Al-Ge phase diagram for a given Al thickness [36]. At the peak anneal temperature the melt-back depth, x, for a given deposited Al thickness, t_{Al}, is determined from the Al-Ge binary phase diagram according to the relation [36],

$$\frac{x}{t_{Al}} = \frac{\rho_{Al}}{\rho_{Ge}} \frac{W_{Ge}}{1 - W_{Ge}}, \tag{4.1}$$

where ρ_{Al} and ρ_{Ge} are the densities of Al and Ge respectively, and W_{Ge} is the weight percent of Ge in the Al melt, given by the point on the liquidus line of the phase diagram at the peak anneal temperature. In this work, the as-implanted P profile was expected to have a depth of ~55 nm at 10^{19} cm^{-3}, which is the conduction band effective density of states for Ge, see Fig. 4.1. Based on this, an Al layer of 25 nm thickness was chosen. At the highest regrowth temperature, 700 ºC, a 25 nm thick Al layer results in a melt-back of 42 nm which leaves enough *n*+ layer thickness to accommodate the *n*-side depletion width of ~10 nm.

4.4 *p*+ doping by Gallium doping of Ge

To form Ge tunnel junctions with lower nonuniformity than observed in RMR junctions using Al [22], an alternate approach was explored using the *p*-type dopant, Ga.

The Al-Ge system has an Al-rich phase and a Ge-rich phase, leading to formation of both these phases after the regrowth, which results in non-planar junctions in this system. The phase diagram of Ga-Ge is simpler than that of Al-Ge, in that only a single Ge-rich phase nucleates on cooling from the Ga-Ge liquidus. Also, Ga has a high solubility in Ge with a peak solubility of 5 x 10^{20} cm^{-3} in the range 650 to 700 ºC [66]. A GaN MBE system was used for the doping of Ge with Ga. The growths were performed at the University of Notre Dame by Kejia Wang, John Simon and Yu Cao.

In this approach, the Ge is doped *p*-type by depositing Ga on the surface and driving it into the surface at the substrate temperature. In these experiments, (100) oriented *p*-Ge wafers (0.13-0.15 Ωcm) and of area approximately 1x1 cm^2 were Indium-mounted onto a Si wafer. Before mounting the wafers, the surface oxide was etched in BHF. The choice of substrate temperature and deposition time sets the diffusion depth of Ga into Ge. The depth of the *p*+ layer is estimated to be the diffusion length of Ga using $\sqrt{D_{Ga}t}$, where D_{Ga} is the Ga diffusivity [68] at the deposition temperature, and t is the deposition time. A box profile was assumed for the incorporated Ga with all the Ga being incorporated substitutionally at the solid solubility, assuming a unity sticking coefficient.

The flux of atoms hitting a surface in an ambient with n atoms per unit volume, is given by [69], $F = n\bar{c}/4$, where $\bar{c}$ is the average velocity of the atoms. The atomic density n at a pressure P is given by $n = P/kT$, where k is Boltzmann's constant, and T is the temperature. The average velocity of atoms in an ideal gas having a Maxwell-Boltzmann velocity distribution is given by [70], $\bar{c} = \sqrt{8kT/\pi m}$, where m is the atomic mass. The flux can then be expressed as,

$$F = (2\pi mkT)^{-\frac{1}{2}}P. \quad (3.5)$$

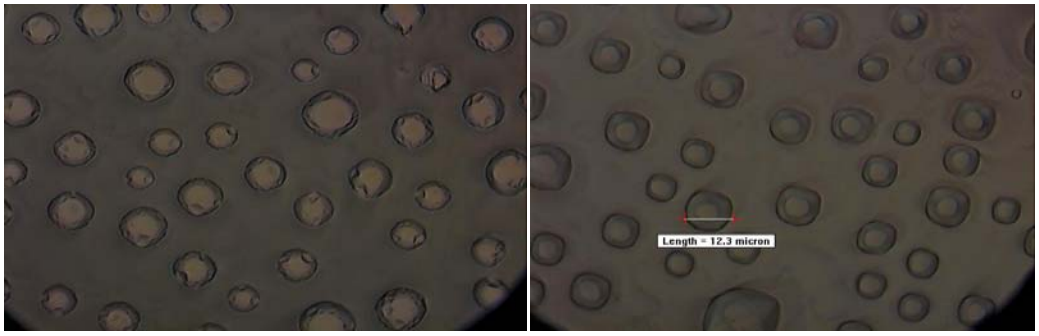
Gallium doping of Ge was explored as a function of Ga flux and deposition times. In a first series of three depositions, K102-K104, the Ga flux was varied and characterized by measuring the chamber pressure, 0.06, 0.6 and 1.8 x 10^{-6} Torr, with a fixed deposition time of 10 minutes at a substrate temperature of 800 ºC.

Table 4.1 MBE deposition parameters for Ga deposition on Ge at a substrate temperature of 800 ºC, and time of 10 minutes. The $\sqrt{D_{Ga}t}$ diffusion depth is calculated to be 65 nm.

Sample	Growth Pressure (10^{-6} Torr)	Ga Flux (10^{14} /cm^{2}s)	Deposited Ga thickness (nm)
K102	0.06	0.08	0.91
K103	0.6	0.77	9.07
K104	1.8	2.31	27.02

After the deposition, Ga droplets were observed on the surface of K103 and K104. The droplets vary in size from 2 to 4 μm in K103, and 7 to 15 μm in K104. The Ga droplets were removed by a 10 minute soak in HCl. After the HCl soak, craters were observed in the Ge surface where the Ga droplets were observed, Fig. 4.5(b). The depth of the craters was measured using a step profiler, and a depth of up to 0.2 μm in K103, and 2 μm in K104 was measured. Since the eutectic temperature of the Ga-Ge system is as low as 29.8 ºC, it is likely that Ge was drawn in from the surface by Ga droplets, thereby leaving craters. These droplets were not observed in optical micrographs of

K102. One reason could be that for the low deposition thickness in this sample, all the Ga deposited was incorporated into the Ga surface. Another possibility is a decrease of Ga sticking coefficient with pressure, causing lesser Ga to be deposited at the lower pressure used in K102, and hence an absence of the Ga pooling that was observed in K103 and K104.

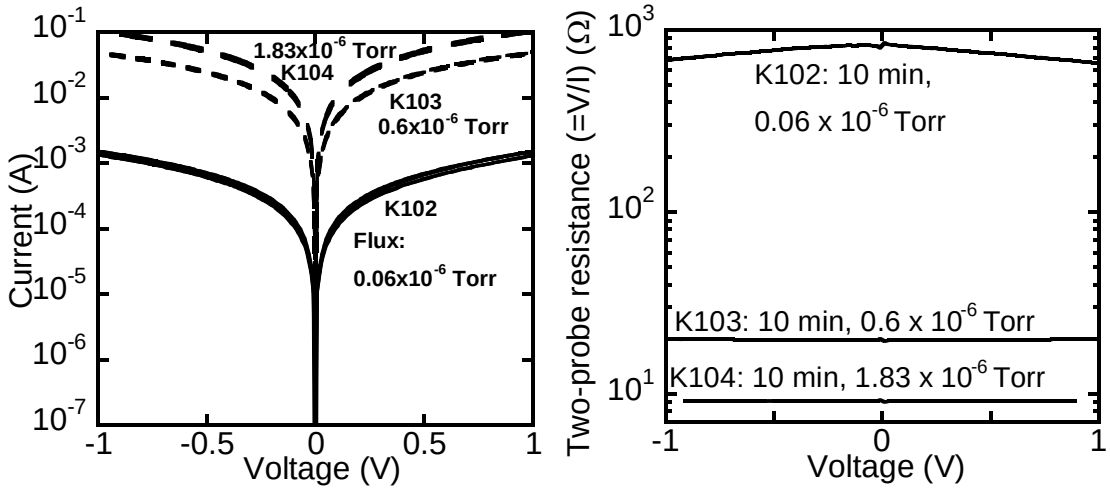


(a) (b)

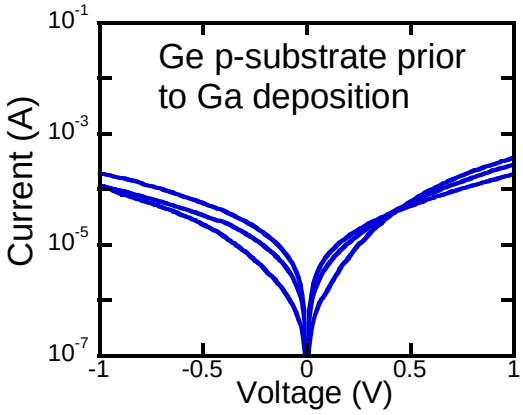
Figure 4.5 Ge surface of wafer K104 after (a) Ga doping in MBE at 800 ºC, 1.8 x 10^{-6} Torr, for 10 minutes, showing Ga droplets, and (b) following removal of Ga droplets using a 10 minute HCl etch to remove the Ga.

Current-voltage characteristics of the Ga-doped surfaces were measured using 25 μm tip diameter coaxial probes separated by 30 μm, Fig. 4.6(a). The probe separation was set using a 30 μm metal pad, and was kept constant across all the wafers measured in this work. In wafers K102-K104, the surface conductivity increased with the Ga flux. The *I-V* characteristic of the *p*-Ge surface prior to Ga doping is shown in 4.6(c) for comparison, from which it is clear that after the MBE Ga deposition an increase in current levels has occurred in K102-K104. A linear *I-V* characteristic is obtained in K103 and K104, as can be seen from the plot of resistance shown in Fig. 4.6(b). The linear *I-V*s obtained in K103 and K104 suggest that ohmic contacts are obtained at the fluxes used in

these wafers. The *I-V* characteristic obtained after deposition at 0.06 x 10^{-6} Torr however is nonlinear. It is likely that in this wafer the density of Ga incorporated was not sufficient to form ohmic contacts upon probing. Since the surface conductivity was highest at a flux of 1.8 x 10^{-6} Torr, indicating higher Ga density, this flux was used for subsequent deposition runs.



(a) (b)



(c)

Figure 4.6 Current-voltage characteristics of Ga doped Ge surfaces measured using a two-probe configuration separated by 30 μm. Shown are the *I-V* characteristics of (a) K102, K103 and K104 which received MBE deposition of Ga at 800 ºC, for 10 minutes, at a flux of 0.06, 0.6 and 1.8 x 10^{-6} Torr respectively, and (b) two-probe resistance calculated as ratio of voltage upon current for every bias point in the *I-V*s shown in Fig. 4.6(a). The *I-V* of the *p*-Ge surface prior to Ga doping is shown in (c) for comparison.

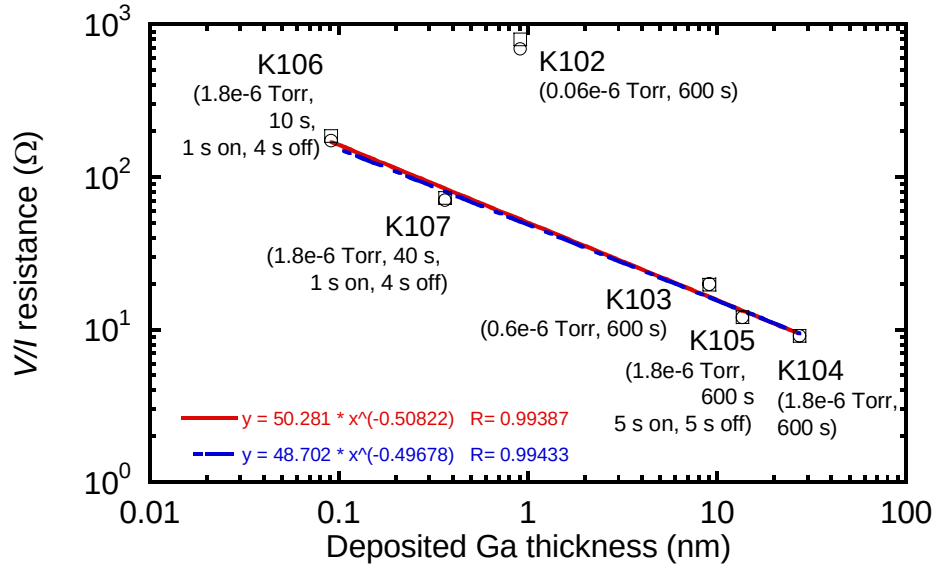
Experiments were performed to determine deposition conditions that yield crater-free Ge surfaces while incorporating Ga at solid solubility levels at 800 ºC using a flux of 1.8 x 10^{-6} Torr. For this purpose, a deposition scheme was explored where the Ga flux

was intermittently shuttered on and off, to allow for the deposited Ga to diffuse into Ge during the off period, before the next Ga deposition period. Using this scheme, Ga was deposited on three wafers, K105, K106 and K107, chronologically, with deposition times of 10 minutes, 10 s and 40 s respectively. The shorter duration growths in K106 and K107 were explored to reduce the amount of Ga being deposited and hence avoid Ga droplet formation, as will be discussed later. The substrate temperature was 800 ºC, and the pressure was 1.8 x 10^{-6} Torr. The calculated flux, and Ga thickness and other experimental details of all the wafers are shown in Table 4.2. After run K105, Ga droplets were still observed. However, the droplets were reduced in size relative to K104 with a diameter of 2-7 μm. Following run K105, the deposition time was reduced in K106 and K107 to deposit lower amounts of Ga and avoid droplet formation. This deposition scheme yielded a Ge surface without formation of Ga droplets as measured by optical microscopy at a magnification of 100x.

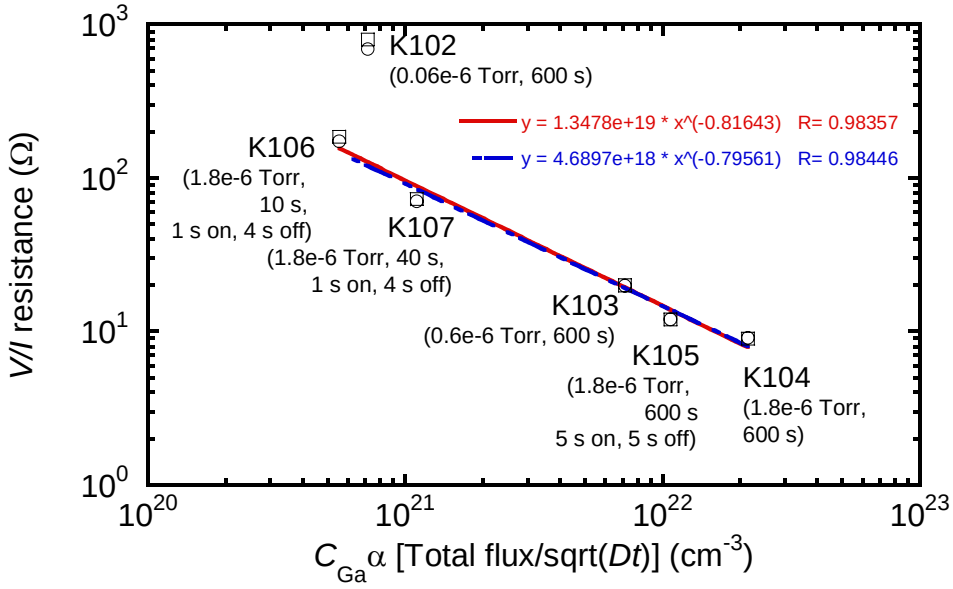
Table 4.2 Summary of MBE deposition experiments of Ga deposition on Ge at a substrate temperature of 800 ºC.

Sample	Growth pressure (10^{-6} Torr)	Calculated Ga Flux (10^{14} /cm^{2}s)	Deposition time (s)	Calcualted Ga thickness (nm)	$\sqrt{(D_{Ga}t)}$ diffusion length (nm)
K102	0.06	0.08	600	0.91	64.54
K103	0.6	0.77	600	9.07	64.54
K104	1.8	2.31	600	27.02	64.54
K105	1.8	2.31	600 (5 s on, 5 s off)	13.6	64.54
K106	1.8	2.31	10 s (1 s on, 4 s off)	0.09	8.33
K107	1.8	2.31	40 s (1 s on, 4 s off)	0.36	16.67

The two-probe *V/I* resistance of all the wafers was examined as a function of the deposited Ga thickness, and is shown in Fig. 4.7(a), at two bias points, 0.2 V and 0.8 V. The resistance decreased with increasing Ga thickness, Fig. 4.7, except in the case of K102 which had the lowest growth pressure 0.06 x 10^{-6} Torr. In the case of K102 it is likely that due to the low flux used in this run, the substitutional density obtained compared to the other wafers is lower. One reason for lower concentration may be that the desorption rate might be significant compared to the flux used in wafer K102. Also, shown in Fig. 4.7(b) is the resistance vs the concentration of Ga incorporated, C_{Ga}, calculated as proportional to the total Ga flux (=$Ft * time\ period$) divided by the $\sqrt{D_{Ga}t}$ diffusion length. While the resistance is expected to be inversely proportional to the Ga concentration, a $C_{\mathrm{Ga}}^{-0.8}$ dependence is obtained. The reason for the deviation is probably that the Ga profile is not a box profile as assumed.



(a)



(b)

Figure 4.7 Two-probe *V/I* resistance of Ga-doped Ge surfaces at 0.2 V (squares) and 0.8 V (hollow circles), measured using 25 μm probe tips separated by 30 μm. The resistance is shown vs (a) deposited Ga thickness, and (b) concentration of Ga incorporated into the Ge.

While the lowest two-probe resistances were obtained in K103, K104, and K105, the surfaces of these wafers had craters. Wafer K106 provided a crater-free surface, but had a non-linear *I-V* as observed from the different resistance values at 0.2 and 0.8 V, Fig. 4.7. This indicates that for the deposition conditions used in K106, ohmic contacts are not obtained when probing this wafer, likely due to a shallow diffusion depth in these wafers which does not accommodate a depletion width and leads to a Schottky barrier. In wafer K107, the deposition time was increased to allow for a deeper Ga. The surface resistance in K107 decreased by a factor of approximately 2.5 over K106, and also improved in linearity. The deposition conditions used in K107 was adopted as the Ga doping parameters for obtaining a *p*+ layer in Ge during subsequent depositions.

4.5 Fabrication of rapid melt regrown Ge junctions

In the first approach used for the Ge junction formation, the *n*+ layer was formed by ion implantation, and the *p*+ side of the junction was formed by RMR. The process used for the junction fabrication is as follows. The Ge surface was first implanted with P at a dose of 5 x 10^{15} cm^{-2}, an energy of 15 keV, and a 7^{o} tilt, as described in section 4.1. Without an implantation anneal, a 25 nm thick Al layer was then deposited on the implanted surface, followed by lithography and etch to form the emitter. A 50 nm SiN_x layer was used to cap the Al layer. After deposition of the SiN_x layer it was observed that bursts were formed in the Al layer, Fig. 4.8. The bursts may have resulted from hydrogen atoms trapped between the Al layer and the Ge surface escaping through the Al-film during the 250 ºC SiN_x deposition. The H on the Ge surface could have resulted from a

BHF dip used to remove the native oxide. The process was continued despite bursts in the film since the Al-layer was intact over the remaining area. Following the SiN_x deposition, the RMR process was performed in a rapid thermal processor at temperatures of 550, 600, 650 and 750 ºC for 1 s, at 100 ºC/s ramp rate, in a 95:5 N_2:H_2 ambient. The rapid thermal anneal was intended to both activate the implanted P, and form the RMR Al-doped Ge layer. After the junction formation, an Al layer was evaporated onto the back of the substrate to form a back-contact.

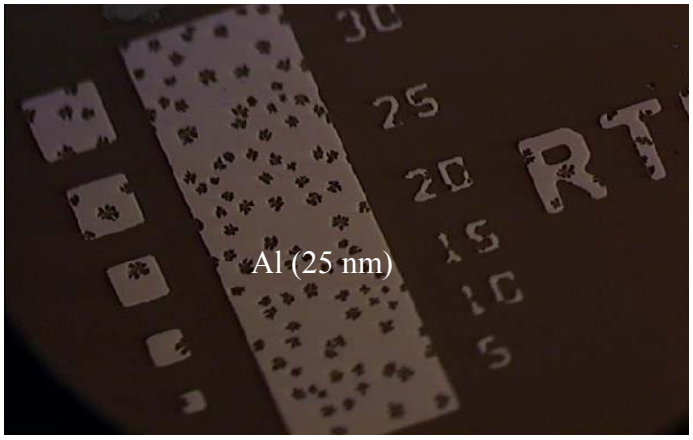


Figure 4.8 Optical micrograph of a Ge surface following a 50 nm SiN_x deposition at 250 ºC, showing bursts in a 25 nm thick Al layer. The numbers at right give the lengths of the squares at left.

Two-terminal measurements of *I-V* characteristics of the Ge diodes were made between the emitter and the back-c ontact, Fig. 4.9. An NDR region was not observed in the diodes for any anneal temperature. In the wafers annealed at 550, 600 and 650 ºC, a shoulder is observed in the *I-V* below 0.5 V, the origin of which is likely recombination current. In Fig. 4.9, data is shown for diodes of designed areas of 15 x 15, 25 x 25, and

40 x 40 μm^2. The current increased monotonically with area, but did not scale with area as expected due to bursts in the metal film changing the area of the diodes.

Comparison of the reverse current to the forward current at +/−0.3 V vs. anneal temperature is shown in Fig. 4.10, Backward diodes with higher conduction in the reverse direction than the forward direction were obtained after anneal at 550, 600, and 650 ºC, while forward diodes were formed at 700 ºC. The absence of NDR in these junctions could result from a low P concentration, either due to low electrical activation or low physical concentration. It has been reported that for implanted P using the same parameters, complete activation was achieved using a 600 ºC for 1 s anneal [62]. Therefore, it does not seem likely that low electrical activation is the reason for lack of NDR. Instead, low physical concentration, resulting from loss of P during the melt-back process, may account for the lack of NDR. During regrowth, the melting of Ge at the surface at the eutectic temperature 420 ^oC is expected to occur before any significant diffusion of the P implant takes place. Phosphorus in the melted Ge layer will not be available for the formation of the *n*+ layer. In effect, there is a P dose loss which reduces the magnitude of the P incorporated. The dose loss is estimated to be the ratio of the integrated P density over the melt-back depth to the total integrated profile.

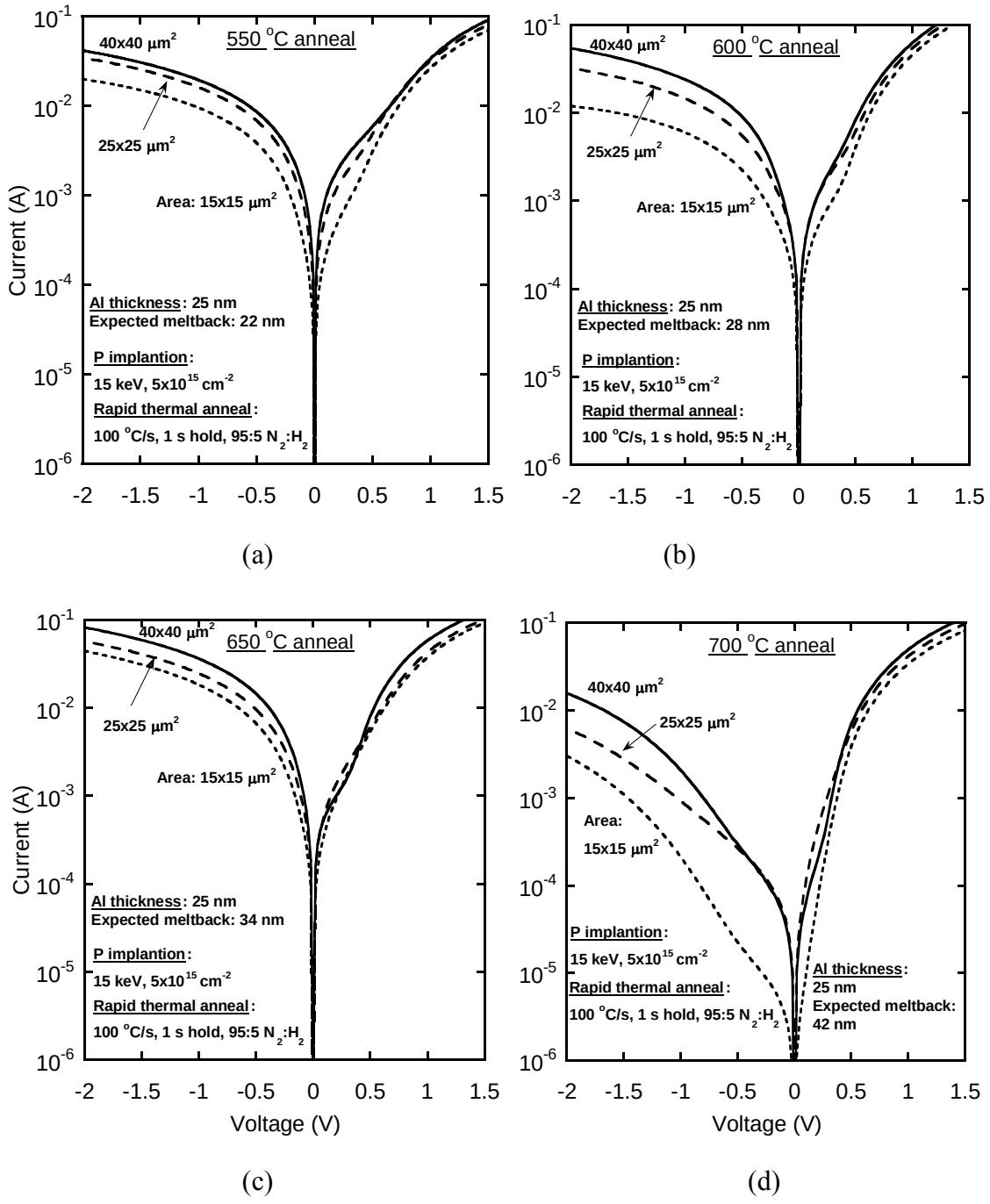


Figure 4.9 Current-voltage characteristics of Ge junctions formed by Al-doped *p*+ Ge regrowth on a P-implanted *n*+ Ge surface at anneal temperatures of (a) 550, (b) 600, (c) 650, and (d) 700 ºC.

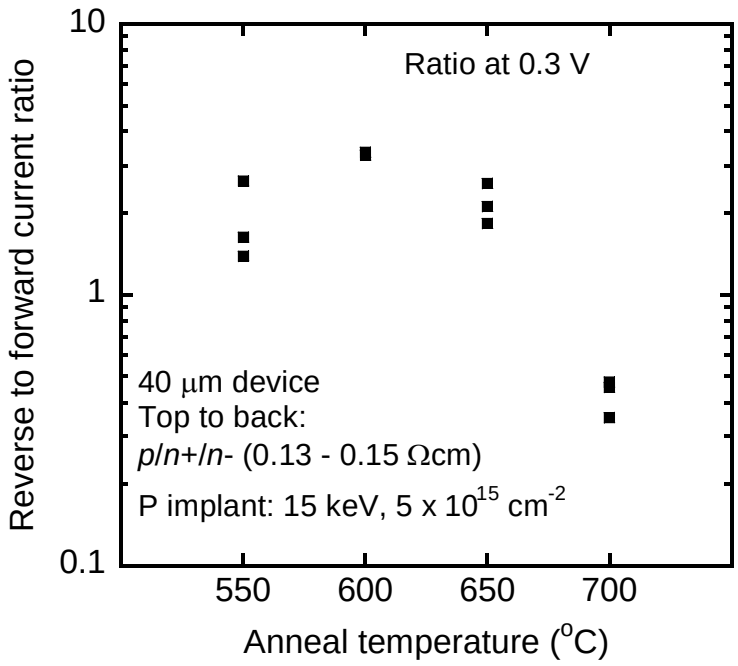
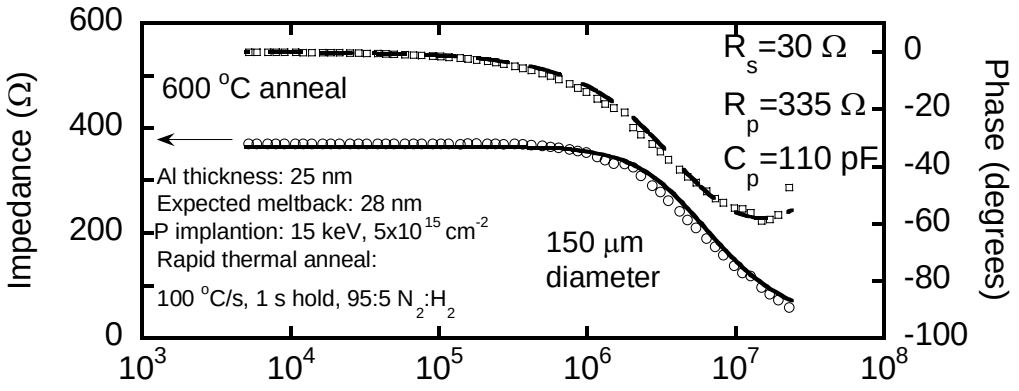


Figure 4.10 Ratio of reverse current to forward current at a bias of +/–0.3 V in Ge junctions formed by Al-doped *p*+ Ge regrowth on a P-implanted Ge surface vs. anneal temperature.

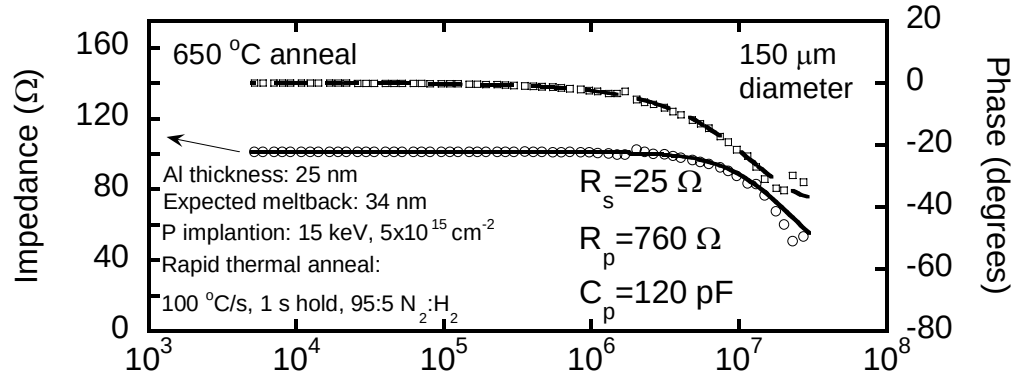
The Ge melt-back at 550, 600, 650, and 700 ºC is calculated from the Al-Ge phase diagram, using Eq. (4.1). The Ge melt-back depths are calculated to be 22, 28, 34, and 42 nm at the anneal temperatures of 550, 600, 650 and 700 ºC. After regrowth the P dose in this meltback thickness is likely unavailable for the formation of the *n*+ layer. The reduced dose available for the formation of the *n*+ layer can be calculated by integrating the P density in the as-implanted profile beyond the melt-back depths that correspond the anneal temperature. The remaining dose, Q_r, after regrowth at 550, 600, 650 and 700 ºC is found to be to be 6.8, 3.3, 1.5 and 0.5 x 10^{14} cm^{-2} by integrating the as-implanted SIMS profile of Fig. 4.1 from the melt-back depths to the extent of the SIMS data. The as-implanted dose, Q, is calculated by integrating the as-implanted P profile, Fig. 4.1, to be 3.9 x 10^{15} cm^{-2}. Clearly, the dose available for the *n*+ layer formation is much lower

than the as-implanted dose and hence the *n*+ concentration could be much lower than that required for tunnel junction.

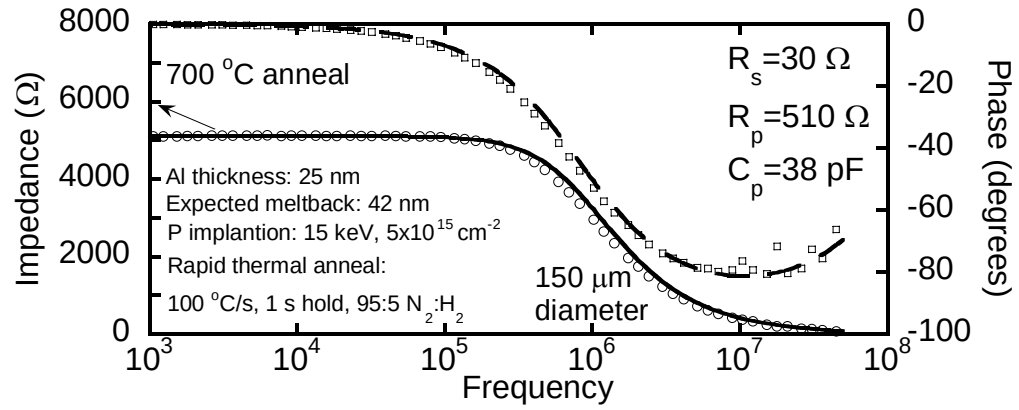
To determine the effective doping density in the Ge junctions, the impedance of the diodes were measured, from which the capacitance of the junction was extracted. A three-element circuit model, with a parallel combination of a resistor and a capacitor, R_p and C_p, in series with a resistor R_s, was used to fit the measured impedance. The effective doping density was then calculated from the capacitance using the relation $C_p = \sqrt{q\varepsilon_s N/2(V_{bi} - 2kT/q)}$ [71]. Impedance measurements were made at zero bias using an Agilent 4294 impedance analyzer, over a frequency range 5 kHz to 50 MHz, Fig. 4.11. The results for the wafer annealed at 550 ºC are not shown because the capacitance could not be extracted due to the conductance dominating at all measured frequencies. The extracted capacitance reveals an effective doping density of 2.1×10^{18} cm^{-3} and 2.5×10^{18} cm^{-3} for diodes annealed at 600 and 650 ºC, and a doping density 2.5×10^{17} cm^{-3} for the diodes annealed at 700 ºC.



(a)



(b)



(c)

Figure 4.11 Measured impedance characteristics at zero bias, of Ge junctions formed using Al regrowth process for *p*+ doping, and implanted P for *n*+ doping. A three element model with parallel resistance and capacitance, R_p and C_p, in series with a resistance R_s, was used to fit the measured impedance (circles) and phase (squares). For purposes of clarity, only thirty percent of the measured data points are shown here.

The above results indicated the need for a higher dose, deeper P implant which would reduce the significance of dose loss in the near-surface region. The deeper implant also allows for the use of thicker Al layers which should eliminate bursts that occurred in the thinner Al films.

4.6 Ge RMR junctions using deeper P implants

In the search for P implants for RMR *p*+*n*+ junctions, the key requirements were high concentration, and implant depths that were higher than the Al metal thickness to be used in the RMR process. A thicker Al film of 100 nm was chosen to avoid the bursts that occurred in the thinner Al film of 25 nm in the previously described experiment during the 250 ºC SiN_x PECVD step. The deeper P implant profiles were chosen based on the work of Satta, *et al*. [62], where a P profile with a peak concentration of 5 x 10^{20} cm^{-3} is demonstrated, Fig. 4.12. The P through a 10 nm PECVD oxide, using an energy of 150 keV and a dose of 10^{16} cm^{-2}. Satta demonstrated profiles after activation anneal at 600 ºC for 1 s, and at 600 ºC for 60 s, Fig. 4.12. In the present work these two profiles, for which the SIMS data is available from the work of Satta *et al*., were chosen to form the *n*+ layers and subsequent formation of RMR junctions. In this experimental run, the activation of the implant was done prior to the RMR process to avoid dose loss during the RMR process as observed in the prior run.

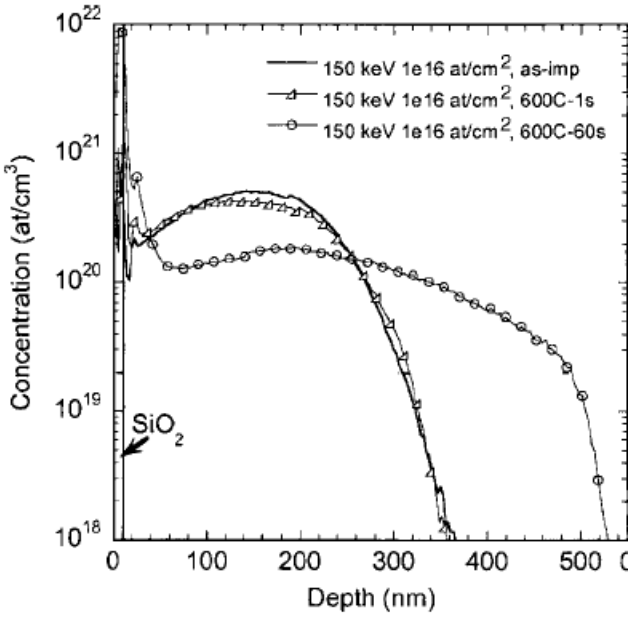
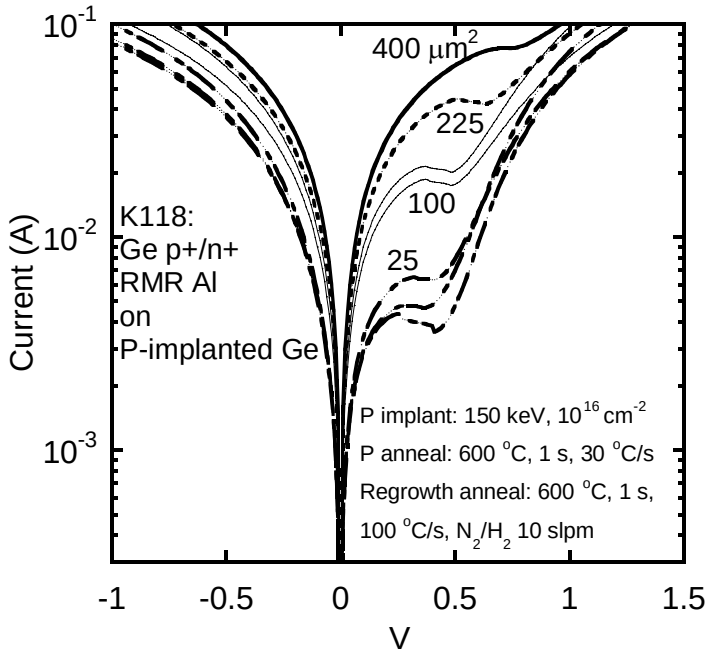


Figure 4.12 SIMS profiles of P implants into Ge from Satta, *et al*. [62].

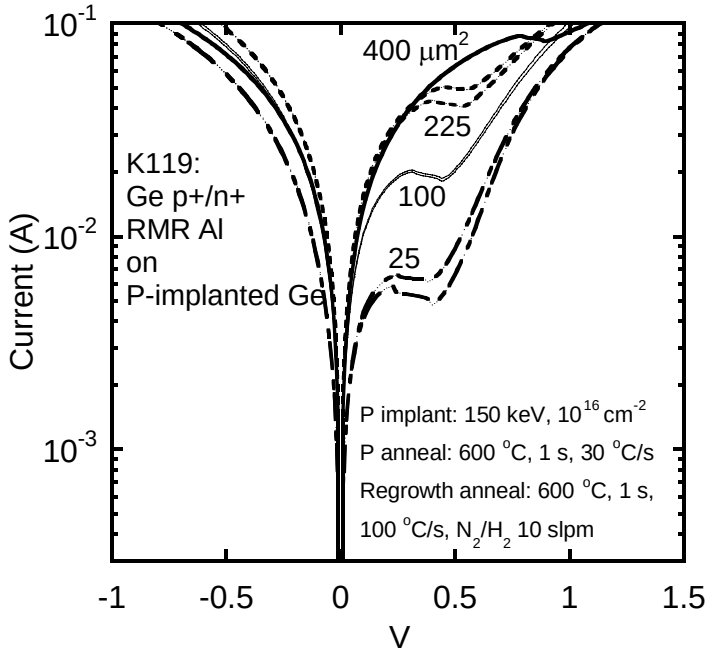
The process used for the fabrication of Ge diodes was as follows. The Ge wafers were degreased using acetone and methanol followed by a 25 s dip in BHF to remove the native oxide. A 10 nm PECVD oxide was deposited on the Ge surface prior to the implantation. The P was implanted at an energy of 150 keV and a dose of 10^{16} cm^{-2}, at a 7^{o} tilt. Two Ge junctions were fabricated with the P implant activation time as the primary variable. Activation anneals were performed at 600 ºC for a duration of 1 s and 60 s. A 100 nm thick Al layer was deposited and patterned on the *n*+ Ge surface, and then capped with a 50 nm silicon nitride layer. The RMR process was then performed using a rapid thermal anneal at 600 ºC, for 1 s, 100 ºC/s in a 95:5 N_2:H_2 ambient. The full procedure is given in Appendix V.

The *I-V* characteristics of the Ge tunnel junctions were measured using a HP4155B SPA over a 1 x 2 cm^2 area for device sizes of 5x5, 10x10, 15x15 and

20x20 μm^2 area. Tunnel diodes exhibiting NDR were obtained for the implant activation anneal durations of 1 s and 60 s, Fig. 4.13. A peak current density of 0.18 to 0.27 $mA/\mu m^2$ was obtained for the 1 s anneal, and 0.20 to 0.27 $mA/\mu m^2$ was obtained for the 600 ºC, 60 s anneal.



(a)

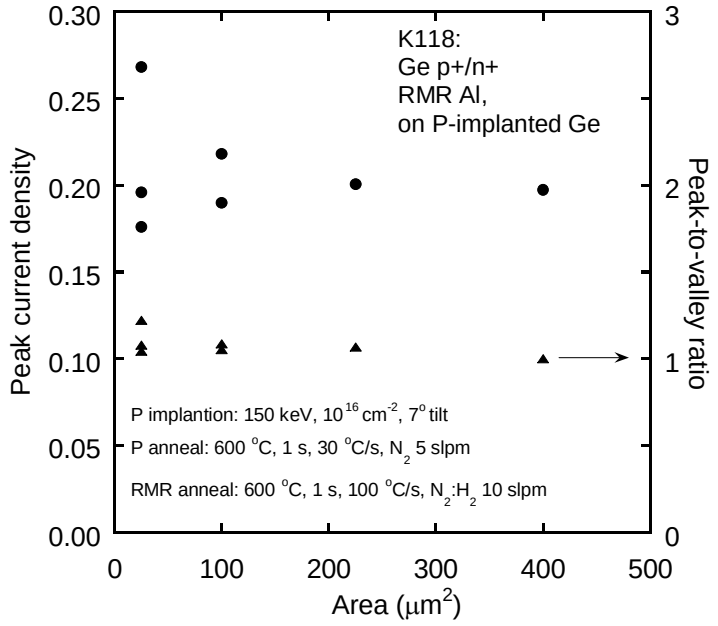


(b)

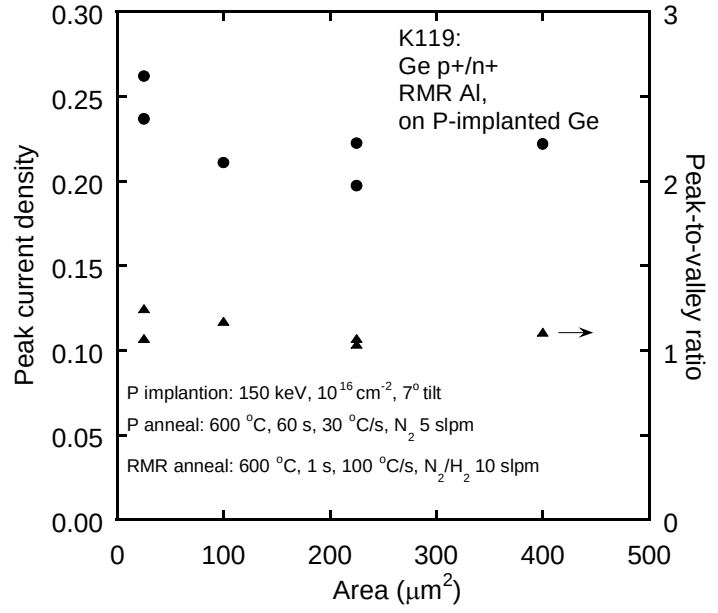
Figure 4.13 Current-voltage characteristics of Ge tunneling-junctions with *n*+ doping formed by P implantation and *p*+ Al doping formed by rapid melt growth process. Shown are results of junctions formed using a P implant activation anneal of (a) 600 ºC, 1 s, 30 ºC/s and (b) 600 ºC, 60 s, 30 ºC/s in 95:5 N_2:H_2 ambient.

The average peak tunneling-current densities obtained using P implant profiles annealed at 1 s and 60 s are 0.20 and 0.22 mA/μm^2, which indicates that the longer activation anneal did not increase level of P activation significantly. These results suggest that the P is completely activated after 1 s anneal at 600 ºC, and further improvement is not obtained for increased anneal duration. Satta *et al*. [62] measured an activation level of 5-6 x 10^{19} cm^{-3} for implanted P at 600 ºC using spreading-resistance profiling.

Figure 4.14 summarizes the current density and PVRs seen in the junctions after the 600 C, 1 s and 60 s anneals. The PVRs are in the range 1.03 to 1.23, Fig 4.14 (a) and (b). The PVRs observed are similar to the results obtained by Zhao *et al.* [36] for the same Al alloying conditions, but a different P-doping technique using spin-on diffusants. These results suggest that the low PVR is intrinsic to the RMR using Al and not the P doping method. Zhang *et al*. [22] showed by transmission electron microscopy (TEM) that a nonplanar melt-back results after regrowth of Al-Ge with no apparent defects at the *p*+*n*+ junction but with significant nonuniformity on the scale of microns to tens of microns across the TEM image.



(a)



(b)

Figure 4.14 Peak current density and peak-to-valley ratio in rapid-melt-regrown Ge junctions on P-implanted Ge with P activation anneal at 600 ºC for (a) 1 s, and (b) 60 s.

4.7 Ge tunnel junctions using diffused Ga

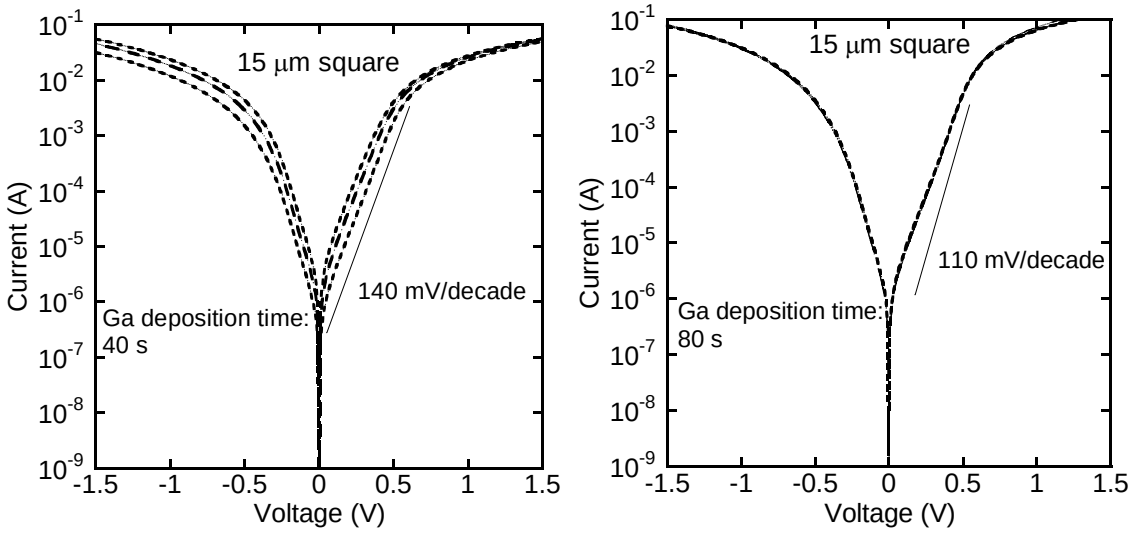
The MBE doping technique for Ga developed in this work was used to form junctions with Ga as the *p*-type dopant and P as the *n*-type dopant. Two sources of P doping were employed; implantation and spin-on diffusants. The deep implantation process discussed in section 4.6 was used for P doping using implantation. Specifically, an energy of 150 keV, 10^{16} cm^{-2} and 7º tilt was used for the implant into an *n*- Ge wafer (0.02-0.15 Ωcm). The implanted P was activated using a 600 ºC, 30 ºC/s anneal in N_2 flowing at 5 slpm. In the SOD process, a *n*- Ge wafer was spin-coated with Emulsitone's 5 x 10^{20} cm^{-3} SOD, and then diffused at 800 ºC, 30 ºC/s, for 10 s in 95:5 N_2:H_2 flowing at 10 slpm in a rapid thermal processor. The peak doping density after the SOD diffusion was 7.8 x 10^{19} cm^{-3} as obtained from SIMS data which is discussed in section 4.2.

Following the P doping, the Ge wafers were doped with Ga using MBE. The Ga was incorporated at a flux of 1.8 x 10^{-6} Torr, using a periodic flux of 1 s Ga on and 4 s Ga off. Two growth times were used for the Ga growth for each P doping technique. Gallium deposition times of 40 s and 80 s were used. In the SOD based wafer, the Ga deposition times of 40 s and 120 s were used. The longer Ga deposition time used in the SOD based wafer compared to the implanted wafer was because the P profile depth in the SOD wafer is deeper and hence can tolerate a deeper Ga doped *p*+ layer as well.

Following the *p*-type doping, the Ge wafers were processed for fabrication of mesa diodes. Aluminum contacts 300 nm thick were patterned onto the Ge wafer using a lift-off process. Germanium mesas of 200 nm were then formed using a CF_4 RIE etch. During the MBE Ga doping process, In was used on the backside of the Ge wafer for the

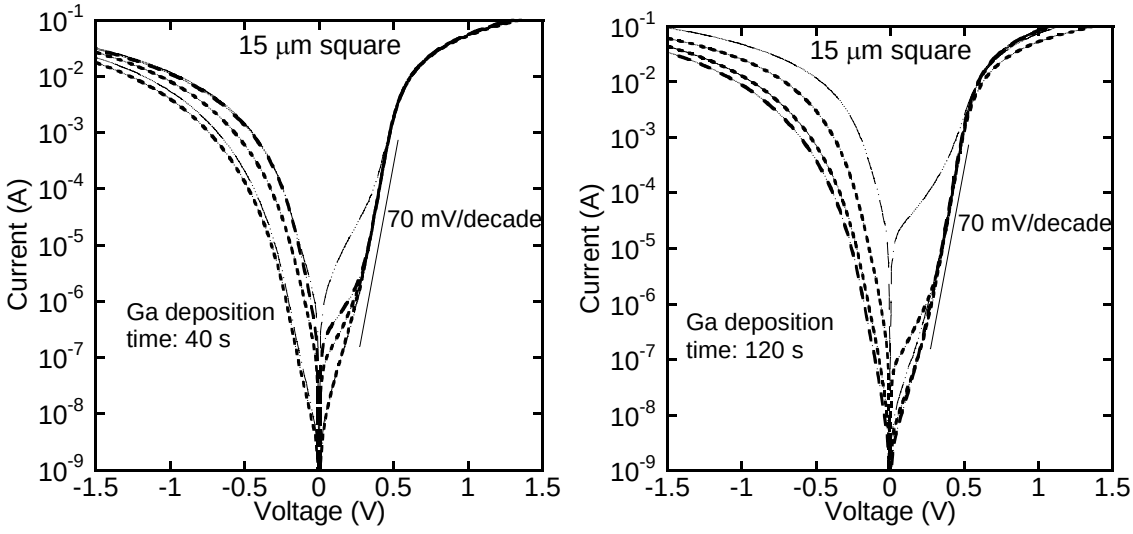
purpose of mounting the wafer onto a Si substrate that acted as a wafer carrier. The In coating was used as the back contact for *I-V* measurements. Processing details are provided in Appendix VI.

The *I-V* characteristics of the fabricated diodes were measured between the Al contact and the back contact, Figs. 4.15 and 4.16. In all wafers it was observed that the reverse current was higher than the forward current, but no NDR is observed in the forward direction. The reverse current being higher than the forward current implies that the *p*-type doping is close to being degenerate, resulting in a backward diode, or that an *n*-Schottky diode is present at the surface. Since the *I-V* characteristics of the Ge junctions shown above indicate either backward diodes or *n*-Schottky diodes, the Ga density is deduced to be either comparable or less than the *n*-type concentration at the surface. The *n*-type concentration in the P diffused wafers 3-4 x 10^{19} cm^{-3}, as seen from the SIMS data in Fig. 4.4. In the case of wafers with implanted P, the active concentration expected for P is 5-6 x 10^{19} cm^{-3} from prior reported results of Satta [62]. Based on the *I-V* characteristics, therefore the Ga doping density is expected to be in the vicinity of the aforementioned P concentrations.



(a) (b)

Figure 4.15 Current voltage characteristics of Ge junctions fabricated using implanted P for the *n*+ doping and Ga doping by MBE at 800 ºC, at a Ga flux of 1.3 x 10^{-6} Torr, which was periodically on for 1 s and off for 4 s, for a growth time of (a) 40 s, and (b) 80 s. The P implantation was done using an energy of 150 keV, a dose of 10^{16} cm^{-2}.



(a) (b)

Figure 4.16 Current voltage characteristics of Ge junctions fabricated using P diffused from SODs for the *n*+ doping and Ga doping by MBE at 800 ºC, at a Ga flux of 1.3 x 10^{-6} Torr, which was periodically on for 1 s and off for 4 s, for a growth time of (a) 40 s, and (b) 120 s.

The above estimates for Ga density are an order of magnitude lower than the solid solubility of Ga in Ge at 800 ^{o}C, 4 x 10^{20} cm^{-3}. While the fluxes used for the Ga doping were calculated to be sufficient to dope the Ge at the solid solubility level, the lower doping levels obtained indicate that the sticking coefficient of Ga needs to be accounted for. It is clear that the Ga flux used during the MBE depositions needs to be to be increased to attain solid solubility levels of Ga in Ge.

The results obtained on Ge junctions are now briefly summarized here. In this work rapid melt re-grown Ge tunnel junctions were demonstrated wherein the *n*+ doping was attained using ion implantation. Two sets of implant profiles, with a depth of 55 nm and 340 nm (taken at a concentration of 10^{19} cm^{-3}, for the purposes of discussion) were explored. In the case of the shallower profiles, an NDR was not obtained after RMR. A possible reason is if a dose loss of P into the Al-doped layer occurred during regrowth, reducing the *n*-type concentration. Tunnel junctions exhibiting an NDR region were obtained for the deeper P profiles, with peak current densities of up to 0.27 $mA/\mu m^2$ and PVRs of 1.1-1.23.

The low PVRs obtained using Al-Ge junctions motivated investigation of Ga as the *p*-type dopant. Gallium doping by diffusion using an MBE source has been demonstrated in this work. Two sets of diodes were fabricated using Ga doping, with the *n*-doping achieved either using implantation or diffusion from SODs. The diodes displayed higher reverse current than forward current, indicative of a backward diode or *n*-Schottky diode. It is believed that diodes exhibiting NDR can be obtained by increasing the Ga doping density by increasing the Ga flux during growth by an order of magnitude over that used in this work.

CHAPTER 5. CONCLUSIONS

This work has explored the fabrication and electrical characterization of *p*+*n*+ tunnel junctions in $In_{0.53}Ga_{0.47}As$ and Ge. The InGaAs junction current-voltage characteristics were investigated as a function of the C and Si density. Germanium tunnel junctions were fabricated using two approaches: (1) rapid melt regrowth of Al-doped *p*+ Ge from an Al metal source into *n*+ Ge and (2) *p*+ Ga doping by diffusion from a Ga metal source into *n*+ Ge.

5.1 $In_{0.53}Ga_{0.47}As$ tunnel junctions

In the InGaAs junctions, C peak densities of 2 and 10 x 10^{19} cm^{-3}, and Si peak densities of 1 to 18 x 10^{19} cm^{-3} were investigated. Steep dopant slopes of 2.3-2.5 nm/decade at a concentration of 10^{19} cm^{-3} were achieved for C. However, it was observed that the C concentration in the Si-doped regions was higher than expected. This could indicate that the solubility of C is increased in heavily-doped InGaAs, or an enhanced diffusion of C in heavily Si-doped InGaAs, however other factors may be responsible e.g. residual C in the growth system or a SIMS artifact e.g. roughness of the etch crater or anomalous change in etch rate during profiling.

$In_{0.53}Ga_{0.47}As$ tunnel junctions with peak current densities up to 0.94 mA/μm^2 at room temperature were demonstrated, which is comparable to the best reported value for an $In_{0.53}Ga_{0.47}As$ tunnel junction. In the junctions used in this work, an NDR is visible at room temperature in $In_{0.53}Ga_{0.47}As$ tunnel junctions for effective doping densities less than 1.50 x 10^{19} cm^{-3}. At densities higher than 2.55 x 10^{19} cm^{-3}, an NDR is not visible at room temperature. In the highest doped junctions, it seems that the excess current causes the absence of NDR at room temperature. When cooled down to 4.2 K, an NDR is revealed with a peak current density of 2.3 mA/μm^2 is measured.

In the forward direction, the highest peak current density observed was 0.94 mA/μm^2 at room temperature, while a peak current density of 2.3 mA/μm^2 was measured at 4.2 K in the heaviest doped junction. Reverse current density in $In_{0.53}Ga_{0.47}As$ junctions has been modeled on the basis of tunneling barrier width, expressed as $J/V_R = J_o \exp(-w/\lambda)$. The exponential fit resulted in a prefactor value of 4.8 to 12.71 mA/μm^2/V, and an attenuation length of 2.5 to 3.3 nm, the latter for junctions fabricated with effective doping densities less than 1.55 x 10^{19} cm^{-3}. In the two junctions with the highest effective doping density, greater than 2.55 x 10^{19} cm^{-3}, the attenuation length reduced to 1.5 and 1.6 nm, a possible reason being an increase in the tunneling mass of the carriers.

5.2 Ge tunnel junctions

In Ge tunnel junctions, two fabrication approaches were investigated. The first approach was based on rapid melt regrowth for junction formation. The RMR process

was used the *p*-type doping using Al, and ion implantation with P was used for *n*-type doping. In junction fabrication processes where shallow implants were used, an NDR was not obtained, possibly to due part of the P implant being lost into the re-grown *p*+ layer. This causes P concentrations to be below degenerate levels in the *n*-side of the junction. In these junctions, the implant activation was done simultaneously with the RMR anneal. It is advisable to perform implant activation anneals prior to the RMR so that the required *n*+ layer is already formed. Also, deeper P implants can be used which can tolerate the loss of P into the re-grown layer. In this work, Ge junctions using deeper P implants were used to form tunnel junctions with a peak current density of up to 0.27 $mA/\mu m^2$. The PVRs obtained in rapid melt re-grown junctions was low, being about 1.1-1.23. This is due to junction nonuniformities that result from multiple phases that form during Al-Ge regrowth. The poor junction quality in the Al-Ge based junctions motivated a diffusion based approach.

In the diffusion based approach the *p*-type doping was done via Ga diffusion in an MBE system. The flux and time used for Ga diffusion significantly affected both the doping density and Ge surface. At fluxes greater than 0.6×10^{-6} Torr and 10 minute growths, Ga droplets were formed after growth. These droplets draw in Ge from the surface below and lead to formation of craters. At fluxes below 0.6×10^{-6} Torr, while droplet formation was not an issue, electrical measurements indicated that the surface was not doped *p*+. Droplet-free growths were achieved using short period grows of 10 to 40 s.

Ge junctions were fabricated using Ga and P as dopants. The P doping was done using implantation or diffusion from SODs. In these junctions an *I-V* characteristic

indicative of a backward diode or Schottky diode behavior was obtained. This indicated that Ga was compensated by P. In-order to tunnel junctions with an NDR region, the Ga density needs to be improved. The results of this work suggest that to achieve Ga concentrations at solid solubility levels of 5×10^{20} cm^{-3} at 800 ºC, the flux needs to be an order of magnitude higher than the flux used here (1.8×10^{-6} Torr).

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SiGe Esaki tunnel diodes fabricated by UHV-CVD growth and proximity rapid thermal diffusion

L.-E. Wernersson, S. Kabeer, V. Zela, E. Lind, J. Zhang, W. Seifert, T. Kosel and A. Seabaugh

A process for realisation of SiGe Esaki diodes in layers grown by ultra-high vacuum chemical vapour deposition has been developed and the first Esaki diodes are reported for this growth method. Intrinsic SiGe-layers are grown on highly boron-doped p^+-Si layers, while post-growth proximity rapid thermal diffusion of phosphorous into the SiGe is employed to form an n^+-layer. Tunnel diodes with a depletion layer width of about 6 nm have been realised in $Si_{0.74}Ge_{0.26}$, showing a peak current density of 0.18 kA/cm^2 and a current peak-to-valley ratio of 2.6 at room temperature.

Introduction: Tunnel diodes require degenerate doping levels and a precise control of the depletion width for optimised performance. High current density SiGe tunnel diodes have been fabricated via direct growth by molecular beam epitaxy, where δ-doped layers were placed on either side of an SiGe layer to increase the current density [1, 2]. Recently, it was demonstrated that Si tunnel diodes [3] may be formed in ultra-shallow junctions realised by proximity rapid thermal diffusion from a spin-on-diffusant (SOD) source [4]. Low-pressure chemical vapour deposition is a widely used technique for growing SiGe, in particular heavily B-doped structures, for Si-based high performance electronic devices [5, 6]. We now demonstrate the formation of SiGe Esaki diodes using the proximity rapid thermal diffusion of phosphorous into a layer of SiGe on top of a p^+-Si layer grown by ultra-high vacuum chemical vapour deposition (UHV-CVD). Thereby the memory effects in the growth chamber and surface poisoning, which are limiting consequences of the required high P-doping levels, are prevented. This approach enables the integration of SiGe Esaki tunnel diodes into the mainstream SiGe technology.

Fabrication: The layer structures were grown by a UHV-CVD hot wall reactor with a base pressure of 1.2×10^{-8} mbar. The layers were grown at a temperature of 620°C using silane (SiH_4), germane (GeH_4) and diborane (B_2H_6) as source gases. Growth pressures were in the range of 10^{-3} mbar. First, a 300 nm-thick boron-doped p^+-Si base structure with a doping level of 9×10^{19} cm^{-3} (wafers 1 and 3) or 2×10^{20} cm^{-3} (wafer 2) was grown on a B-doped ($\rho \sim 0.001\Omega$ cm) 100 mm Si (100) wafer. Then a 21 nm-thick intrinsic SiGe layer with a chemical composition of 14% Ge (wafers 1 and 2) or 26% (wafer 3) was deposited, see Fig. 1. After the growth, phosphorous was diffused from an SOD source (Emulsitone phosphorosilicafilm 1×10^{21}) in a proximity rapid thermal process [4] to form a heavily doped n^+-layer at the surface of the SiGe film. The diffusion was performed as a spike anneal on quarter wafers at 900°C with a holding time of 1 s and a ramp rate of 30°C/s in a nitrogen ambient. The wafers were etched to remove residual SOD in buffered HF. Contacts, 150 µm in diameter, were fabricated by evaporation of Al combined with photolithography and metal etching in Cyantec Al-12 (HNO_3, HPO_3). Finally, mesas were etched by SF_6-based reactive ion etching.

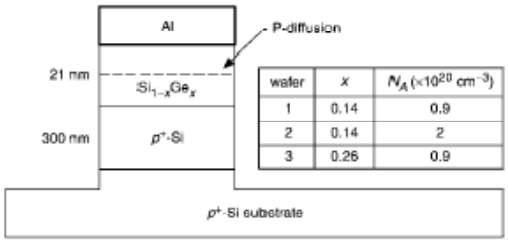

Fig. 1 *Device structure including layer structure for three different wafers*

All measurements performed between top contact (grounded) and substrate

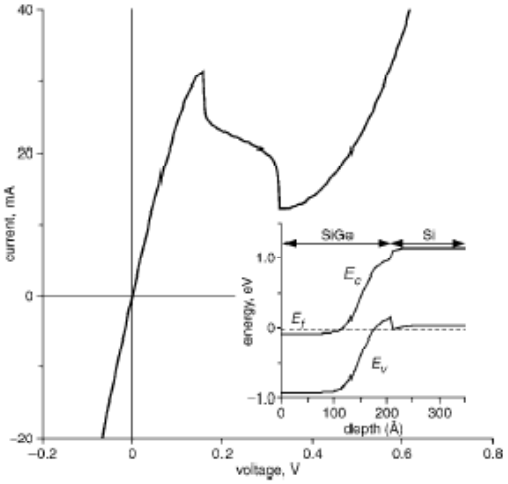

Fig. 2 *Measured room temperature current–voltage characteristics for 150 µm diameter diode*

Inset: Shows calculated bandstructure of diode, using carrier concentration 1×10^{20} cm^{-3} for n^+-SiGe and 9×10^{19} cm^{-3} for p^+-Si with 10 nm per decade gradients

SiGe assumed to have 26% Ge with $\Delta E_c = 30$ meV and $\Delta E_v = 250$ meV

Results: The diffusion of P into $Si_{0.74}Ge_{0.26}$ (wafer 1) resulted in formation of SiGe Esaki diodes as shown in Fig. 2. The highest peak current density of the $Si_{0.74}Ge_{0.26}$ diodes was 0.18 kA/cm^2 with a peak-to-valley current ratio of 2.6. Under the conditions used, our studies of P diffusion in Si by secondary ion mass spectroscopy (SIMS) showed the formation of an 8 nm-thick P-layer with a chemical concentration above 1×10^{20} cm^{-3}, followed by a doping profile with about 10 nm per decade roll-off. Since the diffusion constant for P in SiGe is comparable to that in Si, we used these values and calculated the band-structure of the device, shown as an inset in Fig. 2. The junction was estimated to be formed about 15 nm below the surface and the depletion width in the diodes to be about 6 nm. Since tunnel diodes are sensitive to the doping level, the bandgap, and the effective masses of the tunnelling carriers, diodes with varying doping levels and Ge concentrations, were fabricated, as shown in Fig. 3. Wafer 1, with low Ge concentration (14%) and moderate B-doping, showed backward tunnel diode characteristics. An increase in the doping level in the Si-layer to 2×10^{20} cm^{-3} at the same Ge concentration (14%) (wafer 2) increased the current by a factor 10, resulting in weak negative differential resistance (NDR) with a peak-to-valley current ratio of 1.01 at a current density of 1.2 A/cm^2. The increase in Ge concentration from 14 to 26% (wafer 3) increased the current density by three orders of magnitude and led to strong NDR. This increase may be attributed to a band-structure effect, where the current is enhanced by the reduced bandgap and effective masses of the carriers in the strained SiGe. The origin of the current increase may also be associated with the reduced out-diffusion of B from the highly p-doped Si layer during the subsequent growth of the Ge-rich SiGe layer and the post-growth P-diffusion [7]. Thereby, we reduce the B concentration in the SiGe and effectively sharpen the profiles of the carrier concentrations. There is a strong dependence of the tunnelling current on the depletion width between the degenerate n- and p-electrodes. In our diodes the depletion width is controlled by the doping profiles, which are determined by the process conditions. The diffusion temperature of 900°C was chosen as a trade-off between the sharper doping profiles formed at lower temperatures, and the higher carrier concentrations obtained at elevated temperatures.

Finally, the structural quality of the diodes (wafer 3) was investigated by cross-sectional transmission electron microscopy. High-resolution images of the diodes confirmed the high quality of the material and showed no evidence of dislocation formation in the pseudomorphic SiGe film even after P-diffusion at 900°C.

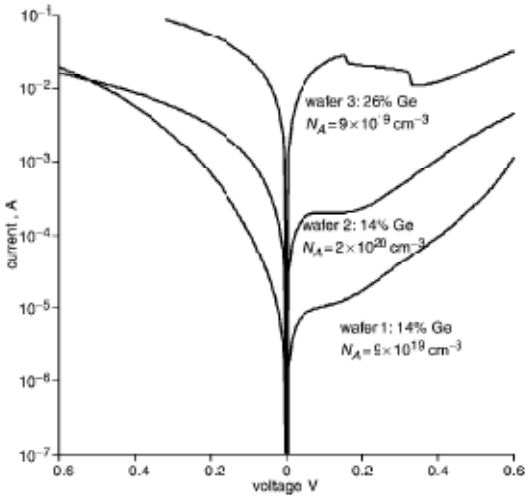

Fig. 3 *Measured room-temperature data for diodes on three different wafers*

Increase in boron doping level or Ge concentration increases tunnelling current with one and three orders of magnitude, respectively

Conclusion: SiGe Esaki diodes have been fabricated by growth of heavily-boron-doped Si and SiGe layers by UHV-CVD combined with proximity rapid thermal diffusion of phosphorous. Tunnel diodes with 26% Ge and a boron doping of 9×10^{19} cm^{-3} show a room temperature peak-to-valley current ratio of 2.6 at a current density of 0.18 kA/cm^2. The diodes show a strong dependence on the Ge fraction with a current density three orders of magnitude lower for devices with only 14% Ge.

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APPENDIX II: A combined CVD and rapid thermal diffusion process for SiGe Eski diodes by ultra-shallow junction formation

A Combined Chemical Vapor Deposition and Rapid Thermal Diffusion Process for SiGe Esaki Diodes by Ultra-Shallow Junction Formation

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Abstract—**SiGe Esaki diodes have been realized by rapid thermal diffusion of phosphorous into an SiGe layer grown by ultra-high-vacuum chemical-vapor-deposition on an Si p^+-substrate for the first time. The phosphorous-doped SiGe forms the n^+-electrode, while heavily boron-doped $Si_{0.74}Ge_{0.26}$ and Si substrate is used for the p^+ electrode. The diodes show a peak current density of 0.18 kA/cm^2, a current peak-to-valley ratio of 2.6 at room temperature, and they exhibit only a weak temperature dependence. Cross-sectional transmission microscopy showed a good crystalline quality of the strained $Si_{0.74}Ge_{0.26}$ layer even after the diffusion step at 900 °C.**

Index Terms—**Esaki diode, SiGe, tunnel diode, ultra-high-vacuum chemical vapor deposition (UHV CVD).**

I. Introduction

ULTRA-SHALLOW junction formation is crucial for the development of future generations of CMOS, and it has been predicted that junctions with a rolloff of <3 nm/decade in the doping profile will be needed for the 35-nm node technology [1]. Recently, it was demonstrated that technologies for ultra-shallow junction formation may be applied to realize Si Esaki diodes [2]. Proximity rapid thermal diffusion [3] of boron into heavily phosphorous doped Si was used to form Esaki tunnel diodes. Studies of Esaki diodes grown by molecular beam epitaxy have shown that the introduction of an SiGe layer between the heavily doped Si electrodes increases the current density [4], [5]. SiGe has a smaller bandgap than Si and the carriers have a lower effective mass, which enhances the tunneling probability and, thus, the tunnel current density. Besides, the introduction of SiGe modifies the diffusivities and, in the case of B, it reduces the diffusion. Hence, a sharper doping profile and a reduced doping compensation may be obtained. In this paper, we use one technology for ultra-shallow junction formation to form SiGe Esaki diodes in a base structure grown by ultra-high-vacuum chemical vapor deposition (UHV CVD). This growth method is widely used for the fabrication of high-performance devices like SiGe heterostructure bipolar transistors [6] and SiGe metal–oxide–semiconductor field-effect transistors [7]. Generally, sharp heterostructure interfaces, high B-doping levels, and abrupt doping profiles may be produced by UHV CVD. These are crucial for the Esaki diodes. However, it is well known that it is troublesome to realize high P-doping with this method due to memory effects in the reactor and surface poisoning [8]. To obtain degenerate n-type doping levels, we have instead employed a post-growth proximity rapid thermal diffusion process based on a spin-on doping source [2], [3]. The combination of the direct growth and the diffusion process provides a new way to realize SiGe Esaki diodes and it opens a novel possibility for the integration of the diodes into very large scale integration (VLSI) circuits.

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II. Experimental

The structures used for the diode fabrication are shown as inserts in Fig. 1. The grown layer consists of 300-nm p^+–Si on a 100-nm B-doped ($\rho = 0.8$–1.2 m$\Omega \cdot$ cm) Si (100) wafer on which a 25-nm-thick i–$Si_{0.74}Ge_{0.26}$ layer capped with 10-nm i–Si layer is deposited. For one set of devices, the top Si layer was later etched off using a selective etch (1 NH_4OH : 2 H_2O). The layer structure was grown in an UHV CVD hot wall reactor, with a base pressure of 1.2×10^{-8} mbar. Silane (SiH_4), germane (GeH_4, 10% diluted in H_2), and diborane (B_2H_6) were used as material sources. The doped Si layer was grown at a pressure of 6.1×10^{-3} mbar, the $Si_{0.74}Ge_{0.26}$ at a pressure of 2.1×10^{-3} mbar, and the intrinsic Si at a pressure of 2×10^{-3} mbar. Prior to growth, the wafers were cleaned in 3 H_2SO_4 : 1 H_2O_2 for 5 min and etched in 5% HF for 1 min to remove the native oxide and to hydrogen passivate the surface. The wafers were loaded into the reactor at 450 °C in an H_2-ambient. At this temperature, the H-passivation is preserved during the loading, while a rapid introduction of silane into the reactor initiates the growth. An undoped silicon buffer layer (<10 nm) was then grown as the reactor temperature was ramped from 450 °C to 620 °C. All subsequent layers were grown at 620 °C. The process for the Esaki diodes was completed via a post-growth, proximity diffusion of P in a rapid thermal process using a spin-on diffusant (SOD) as the dopant source [2]. A source wafer was covered with SOD (Emulsitone phosphorosilicafilm 1×10^{21}) and was placed above the device wafer using three 0.4-mm-thick quartz spacers. A spike anneal in nitrogen ambient was then performed using a ramp rate of 30 °C/s and a holding time of 1 or 3 s at temperatures in the range from 750 °C to 950 °C. After the

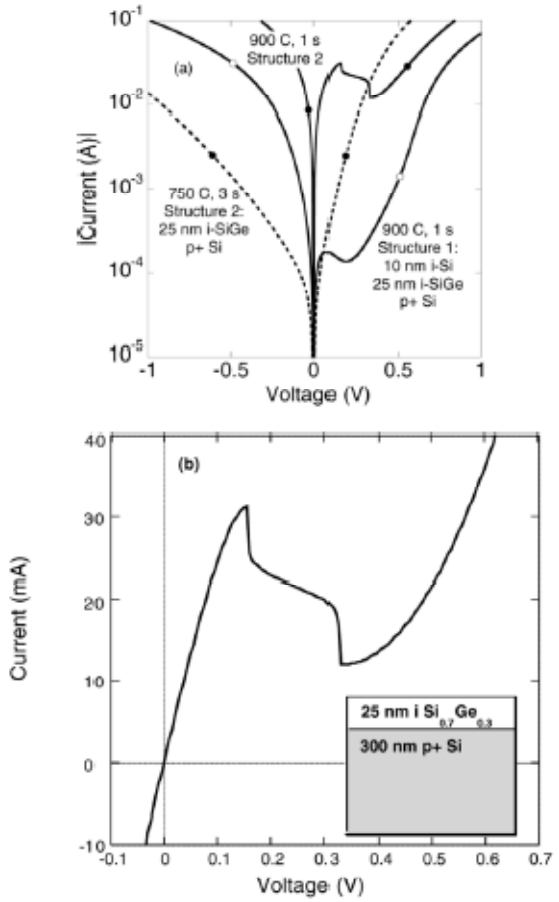

Fig. 1. Measured current–voltage of Si-based Esaki diodes formed by rapid thermal diffusion of phosphorus into UHV CVD Si and Si/SiGe heterostructures. (a) Semilog plot comparing phosphorus rapid thermal diffusions into three wafers, differing by the presence or absence of an Si cap layer: (solid line, open circles) P-diffusion of 900 °C, 1 s into the wafer with the Si cap, (dashed line, solid circles) P-diffusion of 750 °C, 3 s, and (solid line, solid circles) 900 °C, 1 s, into the wafers with the cap removed. (b) Linear current–voltage characteristic of the 900 °C, 1-s diffusion into the wafer with the cap removed.

diffusion, the wafers were cleaned in buffered HF, and Al was evaporated onto the wafers. Contacts with a diameter of 150 μm were defined by optical lithography and etching of the metal in Cyantec Al-12 (HNO_3, HPO_3). Finally, mesas were etched by SF_6 reactive ion etching. The chemical composition and thickness of the Ge layer, as well as the boron level were determined from secondary ion mass spectrometer (SIMS) measurements. On-wafer current–voltage measurements were made using an Agilent semiconductor parameter analyzer with positive bias applied to the p^+-substrate.

III. Results

Fig. 1 shows the measured current–voltage (I–V) characteristics for diodes diffused under various conditions. Diffusion into the complete layer structure (10-nm i–Si on 25-nm i–SiGe)

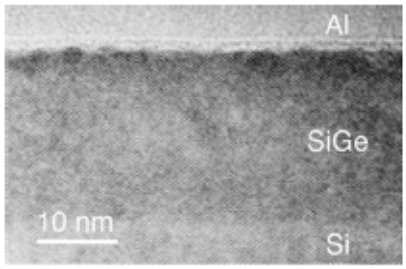

Fig. 2. Cross-sectional TEM image of an SiGe Esaki diode, showing the p^+–Si contact layer, the strained SiGe, including the diffused phosphorous layer, as well as the top Al electrode.

at 900 °C resulted in tunnel diodes with a low current density (approximately 2.4 A/cm^2) and a peak-to-valley current ratio of 1.3, as shown in Fig. 1(a). Diffusion at 750 °C and 900 °C were further carried out on wafers where the top silicon layer was selectively etched off in an ammonium hydroxide solution. At a temperature of 750 °C, a diode characteristic is observed (dashed line), with a comparably high forward current. A forward ideality factor of 2.0 was obtained in the low bias range (0.1–0.2 V) for the 750 °C junction. For a bias exceeding 0.4 V, the 750 °C diode forward current exceeds that of the comparable 900 °C device without an Si cap layer. This higher forward current is a consequence of the lower hole barrier expected for the 750 °C diffusion with a lower P concentration and compensation by the boron. The presence of a lower barrier was experimentally verified by temperature-dependent measurements of the current. At 900 °C, SiGe Esaki diodes were formed showing a peak current density of 0.18 kA/cm^2 and a current peak-to-valley ratio of 2.6 at room temperature.

The material in the tunnel diodes were characterized using cross-sectional transmission electron microscopy (TEM) on a specimen prepared on an actual diode (see Fig. 2). A high quality of the SiGe film, including the heavily P-diffused layer, and the Si/SiGe interface was observed. Occasional defects were observed outside of the active device region, namely, in the Si near the Si/SiGe interface. The specimen showed strain contrast, and maybe B-precipitates in the heavily doped material [9].

Tunnel diodes require: 1) degenerate doping levels; 2) steep doping profiles to prevent carrier compensation and, in the case of SiGe diodes; 3), a matching of the location of the p/n doping transition with the SiGe/Si heterojunction. Each of these requirements depends on dopant placement, which we achieve by proximity rapid thermal diffusion. Three mechanisms can be expected to operate in our process: mass transport from the SOD to the device wafer, reaction of phosphorous and phosphorus oxides at the surface of the wafer, and thermally activated diffusion of P within the semiconductor material. At high temperatures (>900 °C), the sheet conductivity of ultra-shallow junctions formed by proximity rapid thermal diffusion has been found to be limited by mass transport from the SOD [10]. At lower temperatures (<900 °C), a strong thermal activation of the amount of incorporated phosphorus has been observed, related to reactions at the surface of the device wafer [10]. From these studies,

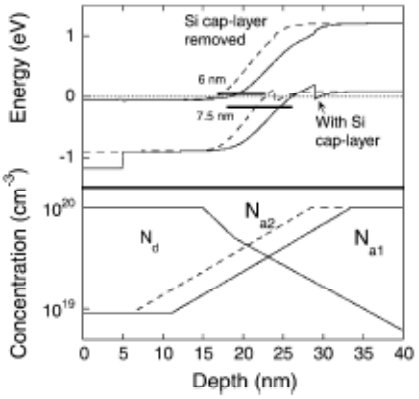

Fig. 3. Calculated band structure (top) for SiGe Esaki diodes showing a strong dependence on the placement of the two doping profiles (bottom). The data is shown with the surface as a reference and, hence, there is a change in the location of the Si/SiGe heterostructure. A depletion width of 6 nm is calculated for the structure where the Si cap layer has been etched off, while 7.5 nm is calculated for the structure with the Si cap.

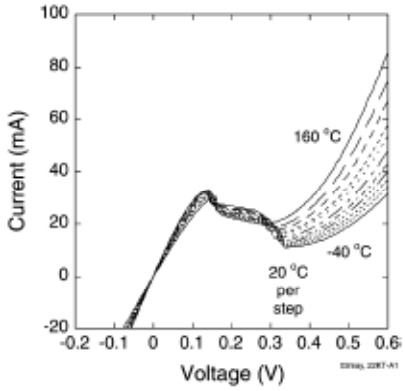

Fig. 4. Measured current–voltage characteristics for the SiGe/Si Esaki diode, 150 μm) as a function of the temperature in the range from —40 °C to 160 °C in steps of 20 °C.

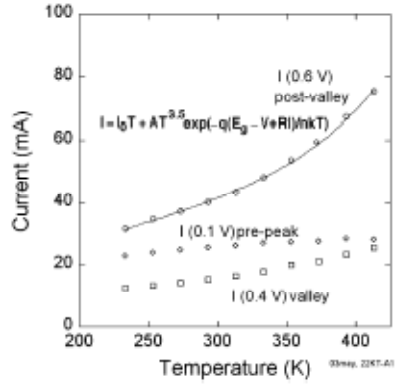

Fig. 5. Temperature dependence of the pre-peak, valley, and post-valley current as a function of the temperature.

we may expect a lower doping level with a sharper doping profile, at a lower diffusion temperature, while the doping level is higher and the gradient less sharp at higher temperatures. Low phosphorus incorporation also explains the absence of tunnel diode formation at 750 °C. Design of Esaki diodes using proximity thermal diffusion must incorporate a tradeoff between the steeper doping profiles formed at lower diffusion temperatures and the higher doping levels obtained at higher temperatures.

Fig. 3 shows the calculated band structures of the SiGe Esaki diodes formed at 900 °C (see Fig. 1). In this calculation, we have assumed a 15-nm-deep phosphorus concentration of 1×10^{20} cm^{-3} followed by a diffusion profile with 10-nm per decade rolloff, as shown in the lower part of this figure. These values are taken from SIMS measurements obtained on a set of proximity diffusions of phosphorus in 20-$\Omega \cdot$cm p-substrates. Higher electrically active phosphorus concentrations have been reported by Hartiti *et al.* [11] using rapid thermal annealing and the same SOD used in this study. For the boron profile, we used a doping level of 8×10^{19} cm^{-3} with a rolloff of 21 nm per decade. The SiGe is assumed to be strained with $\Delta E_C = 30$ meV and $\Delta E_V = 250$ meV for a Ge content of 26%. The simulations were done using parabolic valence bands with an effective mass of 0.31 for the strained SiGe [12]. From the simulated band structure, we estimate a reduction in the depletion width from 7.5 nm for diffusion into the as grown wafer to 6 nm for the etched wafer. Given the exponential dependence of the tunnel current on the depletion width, we estimate that a change in the depletion width by 1 nm will change the current density by a factor of 200. Thus, this reduction may well explain the change from a weak tunnel diode to an Esaki diode with a strong negative differential resistance as the cap layer is removed (see Fig. 1). From simulations of structures with varying doping profiles and junction positions, we expect a further increase in the current density by a factor of 100 after adjustment of the layer structure.

The temperature dependence of the current transport in the tunnel diodes, where the phosphorous was diffused directly into the SiGe, was measured to check the stability of the diodes against temperature variations. We observed an increase in the peak current density by 9.5% as the temperature was increased from —40 °C to 160 °C. In the same temperature range, the peak-to-valley current ratio was reduced from 2.7 to 1.65. The measured current–voltage (I–V) characteristics are shown in Fig. 4, while Fig. 5 shows extracted data for the pre-peak (0.1 V), valley (0.4 V), and post-valley (0.6 V) current as a function of temperature. The current transport in the tunnel diodes may be broken into three current components with different temperature-dependent transport mechanisms [13]: band-to-band tunneling, defect assisted tunneling, and thermionic emission. These currents contribute to the measured currents in various portions at the different biases. The band-to-band tunnel current in our diode has a weak temperature dependence, as seen in the pre-peak data. Its contribution to the measured current is further reduced in the post-peak region. We have fitted the current in the post-valley region to a function with one linear term and one exponential term related to the excess current and the thermally activated current, respectively. The linear term is motivated by the experimental observation that the valley current shows an almost linear dependence. This change reflects the change in density of states, as well as

the small change in the bandgap. Fittings have been made for the applied biases of 0.55, 0.6, and 0.7 V. The fitting at 0.6 V is shown in Fig. 5, taking a series resistance of 0.35 Ω into account. We deduce a value of 0.84 eV for the bandgap and 1.3 for the ideality factor for all four voltages studied. We attribute the value of the bandgap to thermionic emission of holes from Si to SiGe and it is in agreement with the expected value for strained $Si_{0.74}Ge_{0.26}$. The ideality factor may be attributed to the presence of a heterostructure in the junction, with a realistic doping ratio of three to one. The prefactors I_0 and A are found to be weakly voltage dependent, which may be associated with a temperature-dependent series resistance or a combined thermionic and diffusion process.

IV. Summary

We have, in summary, developed a process for the realization of SiGe Esaki diodes via proximity rapid thermal diffusion of phosphorus into an SiGe heterostructure grown via UHV CVD. Cross-sectional TEM shows a high quality of the active device region. Tunnel diodes with a peak current density of 0.18 kA/cm^2 and a current peak-to-valley ratio of 2.6 at room temperature have been achieved. The bandgap of the $Si_{0.74}Ge_{0.26}$ has been determined to be 0.84 eV from fittings to the temperature-dependent measurements of the current transport.

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His current research interests are fabrication and circuit applications of silicon-based Esaki diodes.

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From 1993 to 2000, she was an Assistant Lecturer with the Department of Physics, Polytechnic University of Tirana. From 2000 to 2001, she was Guest Researcher with the Department of Solid State Physics, Lund University. She is currently involved with the growth of SiGe nanostructures with the UHV CVD technique with Lund University.

Erik Lind was born in Luleå, Sweden, in 1976. He received the M.Sc. degree in engineering physics and Ph.D. degree in solid-state physics from Lund University, Lund, Sweden, in 2000 and 2004, respectively.

His research focuses on fabrication of III–V and SiGe devices for high-speed and low-power applications, design, and modeling of resonant tunneling-based devices and circuits, and quantum transport in nanostructures.

J. Zhang, photograph and biography not available at time of publication.

Werner Seifert was born in Germany, in 1941. He received the Dr.rer.nat. and Dr.sc.nat. degrees from the University of Leipzig, Leipzig, Germany, in 1970 and 1982, respectively, and the Docent degree in solid-state chemistry in 1985.

For six months in 1976, he worked within industry where he was involved with the optimization of CVD for LED applications with Werk für Fernsehelektronik, Berlin, Germany. Since 1991, he has been with Lund University, Lund, Sweden, where he is Head of the Epitaxy Group. For three months in 1997, he was with the University of California at Santa Barbara, where he was involved with the growth and characterization of nanostructures GaInN. Since 2000, he has been a Professor with Solid State Physics, University of Lund. His research interests are the epitaxy of semiconductor compounds, *in situ* growth, and self-organization of nanostructures.

Thomas H. Kosel received the B.S., M.S., and Ph.D. degrees in materials science and engineering from the University of California at Berkeley, in 1967, 1970, and 1975, respectively.

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Alan Seabaugh received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Virginia, Blacksburg, in 1977, 1979, and 1985, respectively.

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Dr. Seabaugh is a member of the American Physical Society. He is the 2005 Device Research Conference general chair. He was the recipient of the Teacher of the Year Award presented by the Student Chapter of the IEEE (University of Texas at Dallas, 1989–1990) and the Notre Dame Department of Electrical Engineering Outstanding Teacher Award in 2001.

APPENDIX III: Process traveler for *p* on *n* InGaAs tunnel junctions

Purpose: To fabricate *p*+*n*+ InGaAs tunnel junctions

Surface roughness of samples

1._____,2._____,3._____

Solvent clean

- Soak in hot acetone (boiling point 56.5 ºC) hot plate 60 ºC, 3 min
- Soak in hot methanol (boiling point 64.7 ºC) hot plate 60 ºC, 3 min

Remove surface oxide

- Prepare 1-10 etchant 1HCl:10H_2O – add acid to water, wait to cool.
- Rinse in DI water (DI) 1 min.
- Soak in 1-10 10 s.
- DI rinse 1 min
- Blow dry with N_2
- Microscope inspection – step profile roughness if necessary

AZ5214E image reversal photoresist process

- Spin AZ5214E 5000 rpm (1000 rpm/s ramp) 30 s (1.2 μm)
- Hot plate soft bake 105 °C 30 s
- Measure intensity on Karl Suss MJB3 (expect 14 mW/cm^2) _____ W/cm^2
- Expose in KarlSuss MJB aligner (mask SIRT2 emitter1) 100 mJ/cm^2. Time _____s
- Hot plate reversal bake 110 °C 60 s
- Flood-expose in Karl Suss, 250 mJ/cm^2 (250/intensity = 18 s) _____ s
- Develop in AZ917-MIF[1] ____(35) s
- Rinse in DI 30 s
- Blow dry with N_2
- Descum in O_2 plasma in Tegal Barrel asher[2]: _____ mTorr (300), gas flow setting ____(2), forward power____W (100), reflected power____W(10), time ____s (60)99.999% O_2 purity.
- Soak in 1-10 5 s

[1] MIF,metal ion free, active chemistry TMAH, tetramethylammonium hydroxide, $(CH_3)_4NOH$

[2] Tegal company Model 421.

- DI rinse 10 s
- Blow dry with N_2
- Load without delay

Evaporate RTD emitter FC1800[3] # (1)

Pump chamber to < 2 x 10^{-6} Torr. Record base pressure ___ x 10^{-7} Torr

FC1800 system set points – check and record actual setting

Evaporation parameters						Beam parameters			
Metal	Pd	Pt	Ti	Pd	Au		Pd	Ti	Au
Tooling*	370	120	370	370	370	V (kV)	8.5	8.5	8.5
Density (g/cm^3)	12.04	21.4	4.50	12.04	19.30	I (A)	0.1	0.08	0.08
Z-ratio	0.36	0.245	0.63	0.36	0.38	Long. freq. (Hz)	3	3	3
Rate (Å/s)	2.00	0.5	5.00	2.00	7.00	Lat. freq. (Hz)	3	3	3
Thickness (Å)	100	100	400	400	2400	Long. Ampl. (A)	0.1	0.1	0.1
						Lat. Ampl. (A)	0.3	0.3	0.3

Lift-off

- Heat acetone (boiling point 56.5 ºC) on hot plate to 55 ºC
- Transfer wafers into acetone
- Vertically soak wafer in acetone, 5 min. Record actual soak time _____ min
- Acetone spray to complete lift-off
- Soak in room temperature methanol 2 min
- Blow dry with N_2

Step profile metal stack

1._____,2._____,3._____

Wet Etch to form the TDs

- Prepare 1-8-160 H2SO4: H2O2:H2O etchant as previously described. InGaAs etch rate ~ 40-60 Å/s
- Rinse in DI 1 min
- Etch in 1-8-160 to etch through the junction interface
- Rinse in DI 1 min, step profile.

[3] Airco Temescal electron-beam evaporator

Time	Thickness/Roughness (A)		
	Position 1	Position 2	Position 3

Solvent clean

- Soak in hot acetone (boiling point 56.5 ºC) hot plate 60 ºC, 3 min
- Soak in hot methanol (boiling point 64.7 ºC) hot plate 60 ºC, 3 min

Remove surface oxide

- Prepare 1-10 etchant 1HCl:10H_2O – add acid to water, wait to cool.
- Rinse in DI water (DI) 1 min.
- Soak in 1-10 10 s.
- DI rinse 1 min
- Blow dry with N_2
- Microscope inspection – step profile roughness if necessary

PECVD oxide deposition to protect diodes (30 min)

- Deposit 3500 Å (sio2dep.prc) 7:47 min at 450 Å /min. DC_____V

(Recipe: sio2dep.prc, 25 W, 80:900 sccm SiH_4 : N_2O, 900 mTorr, 250 ^oC)

1813 photoresist process

- Spin 1813 4000 rpm (2000 rpm/s ramp) 30 s
- Hot plate soft bake 90 °C 60 s
- Measure intensity on Karl Suss MJB3 (expect 14 mW/cm^2) _____ W/cm^2
- Expose in KarlSuss MJB aligner (mask SIRT2 emitter-ring 6x6 mm) 56 mJ/cm^2. Time _____s
- Develop in AZ917-MIF[4] ____(20) s
- Rinse in DI 30 s
- Blow dry with N_2
- Descum in O_2 plasma in Tegal Barrel asher[5]: _____ mTorr (300), gas flow setting ____(2), forward power____W (100), reflected power____W(10), time ____s (60)99.999% O_2 purity.

[4]MIF,metal ion free, active chemistry TMAH, tetramethylammonium hydroxide, $(CH_3)_4NOH$

Etch PECVD oxide

- Etch 3500 Å PECVD oxide in Buffered oxide etch[6] 1:32 min. Etch rate 37 Å/s
- Soak in 1-10 5 s
- DI rinse 10 s
- Blow dry with N_2
- Load without delay

Evaporate Collector FC1800[7] # (2)

Pump chamber to < 2 x 10^{-6} Torr. Record base pressure ___ x 10^{-7} Torr

FC1800-2 system set points – check and record actual setting

Evaporation parameters					Beam parameters			
Metal	Ti	Pt	Pt	Au		Ti	Pt	Au
Tooling*	180	120	180	180	V (kV)	8.8	8.8	8.8
Density (g/cm^3)	4.50	21.4	21.45	19.30	I (A)	0.06-0.08	0.16	0.07
Z-ratio	0.63	0.245	0.24	0.38	Long. freq. (Hz)	3	3	3
Rate (Å/s)	2.50	0.5	2.50	7.00	Lat. freq. (Hz)	3	3	3
Thickness (Å)	100	100	100	2000	Long. Ampl. (A)	0	0	0
					Lat. Ampl. (A)	0.4-0.5	0.4-0.5	0.4-0.5

Lift-off

- Heat acetone (boiling point 56.5 ºC) on hot plate to 55 ºC
- Transfer wafers into acetone
- Vertically soak wafer in acetone, 5 min. Record actual soak time _____ min
- Acetone spray to complete lift-off
- Soak in room temperature methanol 2 min
- Blow dry with N_2

[5] Tegal company Model 421.

[6] J.T. Baker Buffered Oxide Etch (30-50% NH4: 40-70% H2O: 0.5-10% HF: surfactant 0.1-0.3%), the surfactant is a hydrocarbon

[7] Airco Temescal electron-beam evaporator

Step profile metal stack

1._____,2._____,3._____

Etch PECVD oxide to reveal Emitter contacts

Etch 3500 Å PECVD oxide in Buffered oxide etch[8] 1:32 min

Step profile metal stack

1._____,2._____,3._____

[8] J.T. Baker Buffered Oxide Etch (30-50% NH4: 40-70% H2O: 0.5-10% HF: surfactant 0.1-0.3%), the surfactant is a hydrocarbon

APPENDIX IV: Process traveler for *n* on *p* InGaAs tunnel junctions

Purpose: To fabricate *p*+*n*+ InGaAs tunnel junctions with a self-aligned collector formed by a head-on evaporation process.

Solvent clean

- Soak in hot acetone (boiling point 56.5 ºC) hot plate 60 ºC, 3 min
- Soak in hot methanol (flash point 64.7 ºC) hot plate 60 ºC, 3 min

Remove surface oxide

- Prepare 1-10 etchant 1 HCl : 10 H_2O – add acid to water, wait to cool.
- Rinse in DI water (DI) 1 min.
- Soak in 1-10 10 s. Etch rate_____
- DI rinse 1 min
- Blow dry with N_2
- Microscope inspection – step profile roughness if necessary

AZ5214E image reversal photoresist process

- Mask: RFID-1, Emitter layer. Size of pattern: 15.875 x 15.875 mm^2 (center: 7.94, 7.94)
- Measure room temperature _____ ºC. Humidity _____%
- Spin AZ5214E 5000 rpm (1000 rpm/s ramp) 30 s (1.2 μm)
- Hot plate soft bake 105 °C 30 s
- Stepper temperature _____ ºC (19 ºC). Calibration date ___/___/2008
- Expose (GCA 6300 stepper[9]) _____ s (3.5 s)
- Hot plate reversal bake 110 °C 60 s
- Measure intensity on Karl Suss MJB3 (expect 14 mW/cm^2). _____ W/cm^2
- Flood-expose in Karl Suss, 250 mJ/cm^2. (250/intensity = 18 s) _____ s
- Develop in AZ917-MIF[10] 30 s
- Rinse in DI 30 s
- Blow dry with N_2

[9] Exposure wavelength for g-line stepper is 436 nm
[10] MIF,metal ion free, active chemistry TMAH, tetramethylammonium hydroxide, $(CH_3)_4NOH$

- Descum in O_2 plasma in Tegal Barrel asher[11]: _____ mTorr (300), gas flow setting ____(2), forward power____W (100), reflected power____W(10), time ____s (60)99.999% O_2 purity.
- Soak in 1-10 5 s
- DI rinse 10 s
- Blow dry with N_2

Load without delay

Evaporate collector FC1800[12] # (2)

Pump chamber to < 2 x 10^{-6} Torr. Record base pressure ___ x 10^{-7} Torr

FC1800-2 system set points – check and record actual setting

Evaporation parameters					Beam parameters			
Metal	Ti	Pt	Pt	Au		Ti	Pt	Au
Tooling					V (kV)	8.7	8.7	8.7
Density (g/cm^3)	4.50	21.4	21.45	19.30	I (A)	0.06-0.08	0.16	0.07-0.09
Z-ratio	0.63	0.245	0.24	0.38	Long. freq. (Hz)	3	3	3
Rate (Å/s)	6.0	0.5	2.5	9.5	Lat. freq. (Hz)	3	3	3
Thickness (Å)	500	100	250+250	2000	Long. Ampl. (A)	<0.1	<0.1	<0.1
					Lat. Ampl. (A)	0.4-0.5	0.4-0.5	0.4-0.5

Lift-off

- Heat acetone (boiling point 56.5 ºC) on hot plate to 55 ºC
- Transfer wafers into acetone
- Vertically soak wafer in acetone, 15 min. Record actual soak time _____ min
- Acetone jet spray to complete lift-off
- Soak in room temperature methanol 2 min

Blow dry with N_2

[11] Tegal company Model 421.
[12] Airco Temescal electron-beam evaporator

ckness/Roughness scan length:			
	Position 1	Position 2	Position 3

Make TLM measurements

Make TLM measurements on n+ control sample, before and after 350 C 20 s anneal listed below

Anneal n+ TLM control sample

	Time (s)	Temp (ºC)	gas N_2/H_2
Idle	90	0	15
Ramp	12	350	2
Hold	20	350	2
Idle	120	0	15

Factors	
1	4
2	1
3	1
4	4

Wafers	Peak Temp. T_P (ºC)

TLM measurements. Contact width 40 μm

Contact separation (μm)	Resistance (Ω)						Resistance (Ω)					
2-probe												
1.5												
3												
7.5												
15												
30												
Sheet res. (Ω/sq.)												
Specific Contact resistance												
Correlation coefficient												

Wet etch to form the TDs

- Prepare 1-8-160 H_2SO_4: H_2O_2:H_2O etchant as previously described. InGaAs etch rate ~ 40-60 Å/s
- Rinse in DI 1 min
- Etch in 1-8-160, etch time 44 s (target 220 nm, at 50 Å/s)
- Rinse in DI 1 min, step profile.

After 44 s on one sample, measure etch rate

Thickness/Roughness (A)			
	Position 1	Position 2	Position 3

Etch remaining samples

After 44 s

Thickness/Roughness (A)			
	Position 1	Position 2	Position 3

Evaporate Pd collector FC1800[13] # (1)

- Pump chamber to < 2 x 10^{-6} Torr. Record base pressure ___ x 10^{-7} Torr
- FC1800 system set points – check and record actual setting

Evaporation parameters			
Metal	Pd	Ti	Pd
Tooling*	370	370	370
Density (g/cm^3)	12.04	4.50	12.04
Z-ratio	0.36	0.63	0.36
Rate (Å/s)	2.0	5.0	2.0
Thickness (Å)	100	400	200

Beam parameters		
	Pd	Ti
V (kV)	10	10
I (A)	0.02	0.05
Long. freq. (Hz)	3	3
Lat. freq. (Hz)	3	3
Long. Ampl. (A)	0.1	0.1
Lat. Ampl. (A)	0.15	0.3

[13] Airco Temescal electron-beam evaporator

Contact anneal in RTP600S[14]

- Anneal contacts

	Time (s)	Temp (ºC)	gas N_2/H_2
Idle	90	0	15
Ramp	12	350	2
Hold	20	350	2
Idle	120	0	15

Factors	
1	4
2	1
3	1
4	4

Wafers	Peak Temp. T_P (ºC)

Measure I-V of tunnel junctions

- Continue on for RFID inductor-TD process
- PECVD SiNx deposition to protect diodes
- Deposit 5000 Å (sinxb.prc) 25 min at 200 Å /min. DC_____V
- Recipe SiNxb
  - Expected rate 20 nm/min.
  - SiH_4 40 sccm, NH_3 4 sccm.
  - 200 W, 500 mTorr.
  - Heat exchanger 60 ºC, substrate 250 ºC

Pattern vias

- Soak in hot acetone (boiling point 56.5 ºC) hot plate 60 ºC, 2 min
- Soak in hot methanol (flash point 64.7 ºC) hot plate 60 ºC, 2 min
- Rinse in DI 2 min
- Blow dry with N_2
- UV Ozone, 10 psi, 60 s

AZ5214E image reversal photoresist process

- Use mask RFID-4, Via layer
- Measure room temperature _____ ºC. Humidity _____%
- Spin AZ5214E 5000 rpm (1000 rpm/s ramp) 30 s (1.2 μm)

[14] RTP600S Rapid Thermal Processing System by Modular Process Technology Corp.

- Hot plate soft bake 105 °C 30 s
- Stepper temperature _____ ºC (19 ºC). Calibration date ___/___/2008
- Expose (GCA 6300 stepper[15]) _____ s (3.5 s)
- Hot plate reversal bake 110 °C 60 s
- Measure intensity on Karl Suss MJB3 (expect 14 mW/cm^2) ._____ W/cm^2
- Flood-expose in Karl Suss, 250 mJ/cm^2. (250/intensity = 18 s) _____ s
- Develop in AZ917-MIF[16] 45 s
- Rinse in DI 30 s
- Blow dry with N_2
- Descum in O_2 plasma in Tegal Barrel asher[17]: _____ mTorr (300), gas flow setting ____(2), forward power____W (100), reflected power____W(10), time ____s (60)99.999% O_2 purity.
- Soak in 1-10 5 s
- DI rinse 10 s
- Blow dry with N_2
- Load without delay

RIE[18] of vias through nitride

- Clean RIE chamber using O_2 plasma for 20 min: 30 sccm, 80 mTorr, 300 W, DC bias
- Condition chamber for 10 mins: SF_6-20 sccm, 20 mTorr, 50 W (70-75 V)_____V.
- RIE etch 5000 Å PECVD nitride for 231 s. Etch rate for PECVD ~26 Å/s. 20% over etch
- Remove PR in ACE, MET 5 mins each at 70 C

AZ5214E image reversal photoresist process

- Use mask RFID-5, Metal layer
- Measure room temperature _____ ºC. Humidity _____%
- Spin AZ5214E 5000 rpm (1000 rpm/s ramp) 30 s (1.2 μm)
- Hot plate soft bake 105 °C 30 s
- Stepper temperature _____ ºC (19 ºC). Calibration date ___/___/2008

[15]Exposure wavelength for g-line stepper is 436 nm
[16] MIF,metal ion free, active chemistry TMAH, tetramethylammonium hydroxide, $(CH_3)_4NOH$
[17] Tegal company Model 421.
[18] Plasmatherm 790 Series

- Expose (GCA 6300 stepper[19]) _____ s (3.5 s)
- Hot plate reversal bake 110 °C 60 s
- Measure intensity on Karl Suss MJB3 (expect 14 mW/cm^2) . _____ W/cm^2
- Flood-expose in Karl Suss, 250 mJ/cm^2. (250/intensity = 18 s) _____ s
- Develop in AZ917-MIF[20] 45 s
- Rinse in DI 30 s
- Blow dry with N_2
- Descum in O_2 plasma in Tegal Barrel asher[21]: _____ mTorr (300), gas flow setting ____(2), forward power____W (100), reflected power____W(10), time ____s (60)99.999% O_2 purity.

Soak in 1-10 5 s

- DI rinse 10 s
- Blow dry with N_2
- Load without delay

Evaporate collector FC1800[22] # (1)

Pump chamber to < 2 x 10^{-6} Torr . Record base pressure ___ x 10^{-7} Torr

FC1800 system set points – check and record actual setting

Evaporation parameters			
Metal	Ti	Pd	Au
Tooling*	370	370	370
Density (g/cm^3)	4.50	12.04	19.30
Z-ratio	0.63	0.36	0.38
Rate (Å/s)	5.0	2.0	7.0
Thickness (Å)	400	400	2400

Beam parameters			
	Pd	Ti	Au
V (kV)	8.5	8.5	8.5
I (A)	0.1	0.08	0.08
Long. freq. (Hz)	3	3	3
Lat. freq. (Hz)	3	3	3
Long. Ampl. (A)	0.1	0.1	0.1
Lat. Ampl. (A)	0.3	0.3	0.3

Lift-off

- Heat acetone (boiling point 56.5 ºC) on hot plate to 55 ºC

[19]Exposure wavelength for g-line stepper is 436 nm
[20]MIF,metal ion free, active chemistry TMAH, tetramethylammonium hydroxide, $(CH_3)_4NOH$
[21] Tegal company Model 421.
[22] Airco Temescal electron-beam evaporator

- Transfer wafers into acetone
- Vertically soak wafer in acetone, 15 min. Record actual soak time _____ min
- Acetone spray to complete lift-off
- Soak in room temperature methanol 2 min
- Blow dry with N_2

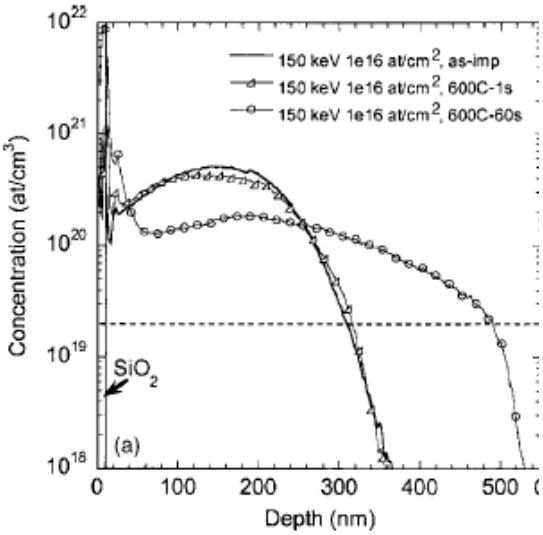
APPENDIX V: Process Traveller for Ge tunnel junctions grown using rapid melt regrowth of Al on Ge for *p*+ doping, and implanted P for *n*+ doping

Experiment Design/Purpose: Form Al/Ge *p*+ *n*+ alloyed Esaki diodes.

The *n*+ layer is formed by implantation of P at 150 keV, 10^{16} cm^{-2}, 7 ^{o} tilt, followed by a rapid thermal annealing at 600 C 1 s, and 60 s, to activate the *n*+ layer. The anneal parameters are taken from the work of Satta et al, *J. of Vac Sci Tec B*, 24(1), 2006, p. 494. The *p*+ layer is formed by depositing a 100 nm Al film, followed by rapid melt regrowth.

P Implantation details:

150 keV, 10^{16} cm^{-2}, 7 ^{o} tilt. Shown below are the SIMS results of as-implanted P and annealed profiles from the work of Satta et al, J. of Vac Sci Tec B, 24(1), 2006, p. 494



Aluminium on Ge alloy characteristics (Dr. Seabaugh's calculation):

T_{PEAK}	$t_{a\text{-}Ge}$ / t_{Al} Deposited films (nm)		t_{Ge} Ge (T_{PEAK} °C) meltback	t_{epi} Regrown epitaxial Ge	$t_{eu} = t_{Ge} - t_{epi}$ Al-Ge mix. interface	$t_{eu\text{-}mix}$ Al-Ge mix. thickness	Density			Phase diagram fractions	
°C	Ge	Al	nm	nm	nm	nm	(g/cm^3)		C_L		0.69
600	0	100	113	61	52	203	r_{Ge}	5.32	0.63	C_E	0.51
							$r_{a\text{-}Ge}$	3.9	0.69	C_{SE}	0.99
							r_{Al}	2.7	0.73	F_{Ge}	0.505
							$r_{a\text{-}Al}$	2.7	0.77	F_{Al}	0.495

Al solubility in Ge (Trumbore): ~$5x10^{20}$ cm^{-3} at 600 °C

Ge wafer numbers/description:

<100>, Sb-doped, Ωcm

- Degrease the Ge wafer in hot acetone and methanol at 70 C for 5 minutes each
- Blow dry
- DO NOT ETCH IN BHF (A 100 Å layer SiO_2 is present on the surface)
- Inspect

Implant activation anneal

600 C, 1 s, 30 C/s, N2

	Time (s)	Temp (ºC)	gas1: N_2	gas2 N_2:H_2	Factors	
Idle	90	25	0	10	1	2.5
Ramp	20	600	0	10	2	1
Hold	1	300	0	10	3	1
Idle	90	0	0	10	4	1

600 C, 60 s, 30 C/s, N2

	Time (s)	Temp (ºC)	gas1: N_2	gas2 N_2:H_2	Factors	
Idle	90	25	0	10	1	2.5
Ramp	20	600	0	10	2	1
Hold	60	300	0	10	3	1
Idle	90	0	0	10	4	1

Pattern Collector Window[23]

Image Reversal Photoresist process
DO FOLLOWING ON A PILOT FIRST

- Measure room temperature _____ ºC. Humidity _____%
- Spin AZ5214E 5000 rpm (1000 rpm/s ramp) 30 s (1.2 μm)

[23] GCA 6300 g-line (436 nm) wafer stepper

- Hot plate soft bake 105 °C 30 s
- Stepper temperature _____ ºC (19 ºC). Calibration date ___/___/2008
- Expose (GCA 6300 stepper[24]) _____ s (3.2 s)
- Hot plate reversal bake 110 °C 60 s
- Measure intensity on Karl Suss MJB3 (expect 14 mW/cm^2) . _____ W/cm^2
- Flood-expose in Karl Suss, 250 mJ/cm^2. (250/intensity = 18 s) _____ s
- Develop in AZ917-MIF[25] 40 s
- Rinse in DI 30 s
- Blow dry with N_2
- Descum in O_2 plasma in Tegal Barrel asher[26]: _____ mTorr (300), gas flow setting ____(2), forward power____W (100), reflected power____W(10), time ____s (60)99.999% O_2 purity.
- Soak in 1-10 5 s
- DI rinse 10 s
- Blow dry with N_2
- Load without delay

Evaporate TD emitter (FC1800[27] # 2)

- Pump chamber to < 2 x 10^{-6} Torr. Record base pressure ___ x 10^{-7} Torr
- FC1800 system set points – check and record actual setting

Evaporation parameters		Beam parameters	
Metal	Al		Al
Tooling*	180	V (kV)	8.5
Density (g/cm^3)	2.7	I (A)	0.2
Z-ratio	1.08	Long. freq. (Hz)	3
Rate (Å/s)		Lat. freq. (Hz)	3
Thickness (Å)	1000	Long. Ampl. (A)	0.1

***** This tooling is for the flat bar.

Lift-off

- Transfer wafers into acetone
- Soak in hot acetone 5 min and start timer. Record actual soak time _____ min
- Acetone spray to complete lift-off
- Soak in methanol 2 min
- Blow dry with N_2

[24]Exposure wavelength for g-line stepper is 436 nm
[25]MIF,metal ion free, active chemistry TMAH, tetramethylammonium hydroxide, $(CH_3)_4NOH$
[26] Tegal company Model 421.
[27] Airco Temescal electron-beam evaporator

Thickness/Roughness (A)			
	Position 1	Position 2	Position 3

Do TLM measurements

Contact separation (μm)	Resistance (Ω)		Resistance (Ω)	
	K118	K119	K118	K119
2-probe resistance				
2 4 8 16 32				
Sheet res. (Ω/sq.)				
Specific Contact resistance				
Correlation coefficient				

Clean-up

- Degrease the Ge wafer in hot acetone and methanol for 5 minutes each
- Rinse in D.I. water and blow dry
- UV Ozone[28] clean 120 s. Record UV/ozone O_2 inlet pressure _____ psi 99.999% O_2 purity, 10 psi inlet pressure, removes photoresists ~0.25 Å/s

Plasma-Enhanced Chemical Vapor Deposition[29]

- Prepare, RCA clean, Si pilot wafer, load with samples
- Load samples
- Cap the Al/Ge with 50 nm SiN_X (Recipe SiNxb)
  - SiH_4 40 SCCM, NH_3 4 SCCM
  - Heat exchanger 60 ºC, substrate 250 ºC
  - Power: 200 W
  - Pressure: 500 mTorr
  - Expected rate 20 nm/min

[28] Jelight Company Model 144AX
[29] Uniaxis 790

- Time: 2.5 min (expecting 50 nm)

Ellipsometry

- Measure Si_3N_4 thickness using GEMP (Gaertner Ellipsometer Measurement Program) on Si pilot with incident angle 70 ˚

Location	Si thickness (nm)	n
1		
2		
3		

Rapid Thermal Anneal

- Run program 600C1.RPD
- Verify the RTA program by running on a test wafer
  600 ºC, 1 s, ramp rate 100 ºC/s, forming gas ambient (N_2:H_2 95:5)

  600C1.RPD

	Time (s)	Temp (ºC)	gas1: N_2	gas2 N_2:H_2
Idle	90	25	0	10
Ramp	10	300	0	10
Hold	20	300	0	10
Ramp	3	600	0	10
Hold	1	600	0	10
Idle	90	0	0	10

Factors	
1	4.2
2	1
3	1
4	1

- Rapid thermal anneal each sample, record actual annealing temperatures and times

Sample	Peak Temp. T_P (ºC)	Cooling start time (s) at T_P	T_P - 50 ºC	Time (s) at T_P - 100 ºC	T_P - 150 ºC	Cooling Rate (ºC/s)

Measurements

- I-V measurements before removal of SiNx cap layer

SiNx RIE etch if needed

- Condition chamber (SF_6 20 sccm @ 20 mTorr, 50 W for 2 min)

- Use SiNx on Si to determine the etch time
- Etch (SF_6 20 sccm @ 20 mTorr, 50 W for _____ sec, DC _____ V (90-80)); overetch factor _____ (1.3)
- SiNx etch rate 1300 Å/min
- Etch stops when metal appears

APPENDIX VI: Process traveler for Ge tunnel junctions using Ga from MBE source as *p*-type dopant and implanted P or SOD diffused P as *n*-type dopant

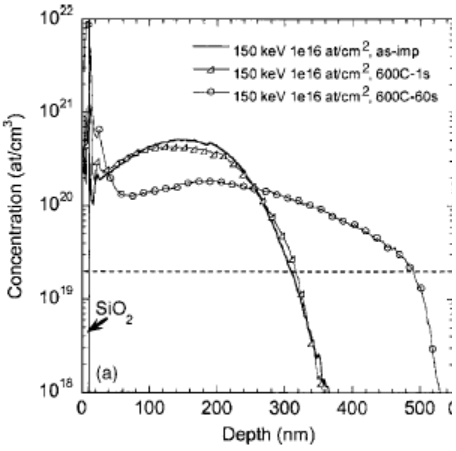
Experiment Design/Purpose: Form *p+(Ga) n+(P)* Ge Esaki diodes using Ga doping from an MBE source

Basic sample structure

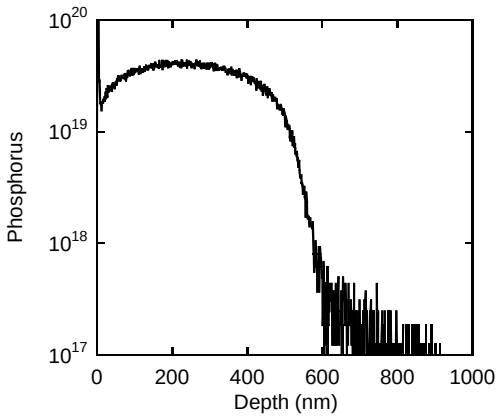
Al contact
p+ Ge, Ga MBE doped
n+ Ge P doped (implant, or SOD)
n- Ge substrate
Indium from MBE growth

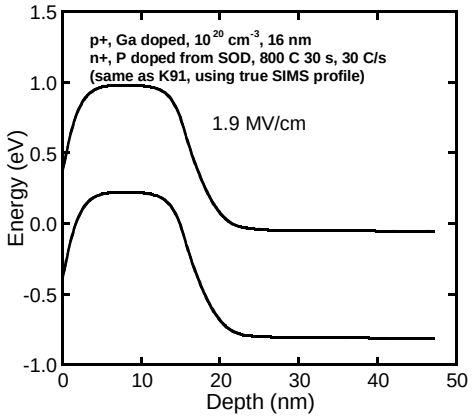
n+ doping details

1. Implanted P: SIMS of P implant & RTA anneal taken from Satta et al, J. Vac Sci Tec B, 24(1), 2006, p. 494



2. P from Emulsitone's Phosphorosilicafilm $5x10^{20}$ at 800 C, 10 s, 30 C/s, 95:5 N_2:H_2 10 slpm. But here we show SIMS of K91, which is diffused at 800 C for 30 s, closer to reality, as subsequent Ga MBE growth is at 800 C for 40 s





p+ layer Ga doping in MBE (based on K107 result of Ga doping of Ge, 40 s growth)

Temperature: 800 C, Flux: 1.83 x 10^{-6} Torr.

Growth Times: 40 s, 80 & 120 s. Periodic Flux ON time: 1 s, OFF time 4 s

Estimation of Ga diffusion depth, using √(Dt)

Ga diffusivity		Diffusivity reference: Vacancy-impurity complexes & diffusion of Ga & Sn						
Do (cm^2/s)	80	in intrinsic and p-Ge, by Riihimaki, I.						
Ea (eV)	3.21	*q*	1.6E-19	k	1.38E-23	J/K		
Growth step	Temperature C	Time s	Ga Diffusivity cm^2/s	Diff. length nm				
Ga growth	800	40	7.1E-14	16.80				
Ga growth	800	80	7.1E-14	23.76				
Ga growth	800	120	7.1E-14	29.10				

To be determined:

- Surface morphology after P SOD diffusion
- P doping density: TLM of SOD piece? Need a p-type sample
- Surface after Ga diffusion
- Ga doping density: TLM measurements of Ga-doped Ge
- IV of diodes, top to bottom
- If NDR absent? C-V measurements to extract doping density?

Ge wafer numbers/description:

<100>, Sb-doped, 0.038-0.04 Ωcm, 500 μm, from MTI corp.

- Degrease the Ge wafer in hot acetone and methanol at 70 C for 5 minutes each
- Blow dry
- DO NOT ETCH IMPLANTED WAFER IN BHF (A 100 Å layer SiO_2 is present on the surface)
- Etch native oxide of other wafers in BHF for 20 s
- Rinse in DI, blow dry
- Inspect

Spin-on Phosphorosilicate Film

Cover spinner ring with aluminum foil

- Bake SOD at 120 C for 2 mins to remove moisture
- Drip coat source wafers with Emulsitone Phosphorosilicafilm 5 x 10^{20} spin-on diffusant[30]
- Spin program: 1000 rpm 10 s, 3000 rpm 30 s. (thickness ~ 550 nm)
- Bake the wafer at 150 °C for 20 min.
    - 110 C for 3 mins
    - 120 C for 3 mins
    - 130 C for 3 mins
    - 140 C for 3 mins
    - 150 C for 20 mins
- Note surface morphology

RTA in RTP600S

Activation anneal for implanted wafer: 600 °C, 60 s, 30 °C/s, N_2:H_2. File name:

	Time (s)	Temp (ºC)	gas1: N_2	gas2 N_2:H_2	Factors	
Idle	90	25	0	10	1	2.5
Ramp	20	600	0	10	2	1
Hold	60	300	0	10	3	1
Idle	90	0	0	10	4	1

[30] **Phosphorosilicafilm SOD expires _____ months after opening**

SOD diffusion: 800 ^{o}C, 10 s, 30 ^{o}C /s, N_2:H_2. File name:

	Time (s)	Temp (ºC)	gas1: N_2	gas2 N_2:H_2
Idle	90	25	0	10
Ramp	27	800	0	10
Hold	10	800	0	10
Idle	90	0	0	10

Factors	
1	2.5
2	1
3	1
4	1

Peak Temp. T_P (ºC)	Cooling start time (s) at T_P	T_P - 50 ºC	Time (s) at T_P - 100 ºC	T_P - 150 ºC	Cooling Rate (ºC/s)

- Etch SOD residue in buffered HF for 5 min to remove SOD
- Rinse in D.I. 2 min
- Blow dry in N2

Surface morphology:

- Inspect and take micrographs after SOD diffusion
- Step profile surface roughness

Thickness/Roughness (A)			
	Position 1	Position 2	Position 3

- Etch 10 nm of PECVD oxide on implanted wafer in BHF for 20 s
- Rinse in DI, blow dry

Ga MBE doping

Ga diffusion for three growth times:

- Flux: 1.83 x 10^{-6} Torr
- Growth Time: 40 s, 80 s and 120 s. Periodic Flux ON time: 1 s, OFF time 4 s
- Cell temperature: 1100 C/1000 C

Inspect surface

- Micrographs of surface after Ga diffusion
- Degrease the Ge wafer in hot acetone and methanol at 70 C for 5 minutes each
- Blow dry
- Etch native oxide in BHF for 20 s

- Rinse in DI, blow dry

Pattern Collector Window[31]

Image Reversal Photoresist process using Test structure mask
DO FOLLOWING ON A PILOT FIRST

- Measure room temperature _____ ºC. Humidity _____%
- Spin AZ5214E 5000 rpm (1000 rpm/s ramp) 30 s (1.2 μm)
- Hot plate soft bake 105 °C 30 s
- Stepper temperature _____ ºC (19 ºC) . Calibration date ___/___/2009
- Expose (GCA 6300 stepper[32]) _____ s (3.1 s)
- Hot plate reversal bake 110 °C 60 s
- Measure intensity on Karl Suss MJB3 (expect 14 mW/cm^2). _____ W/cm^2
- Flood-expose in Karl Suss, 250 mJ/cm^2. (250/intensity = 18 s) _____ s
- Develop in AZ917-MIF[33] 40 s
- Rinse in DI 30 s
- Blow dry with N_2
- Descum in O_2 plasma in Tegal Barrel asher[34]: _____ mTorr (300), gas flow setting ____(2), forward power____W (100), reflected power____W(10), time ____s (60)99.999% O_2 purity.
- Soak in 1-10 5 s
- DI rinse 10 s
- Blow dry with N_2
- Load without delay

Evaporate TD emitter (FC1800[35] # 2)

- Pump chamber to < 2 x 10^{-6} Torr. Record base pressure ___ x 10^{-7} Torr
- FC1800 system set points – check and record actual setting

Evaporation parameters		Beam parameters	
Metal	Al		Al
Tooling*	180	V (kV)	8.5
Density (g/cm^3)	2.7	I (A)	0.13
Z-ratio	1.08	Long. freq. (Hz)	3
Rate (Å/s)	7	Lat. freq. (Hz)	3
Thickness (Å)	3000	Long. Ampl. (A)	0.1

[31] GCA 6300 g-line (436 nm) wafer stepper
[32]Exposure wavelength for g-line stepper is 436 nm
[33]MIF,metal ion free, active chemistry TMAH, tetramethylammonium hydroxide, $(CH_3)_4NOH$
[34] Tegal company Model 421.
[35] Airco Temescal electron-beam evaporator

* This tooling is for the flat bar.

Lift-off

- Transfer wafers into acetone
- Soak in hot acetone 80 C, 10 min and start timer. Record actual soak time _____ min
- Acetone spray to complete lift-off.
- Ultrasonic 5mins
- Soak in methanol 2 min
- Blow dry with N_2

Thickness/Roughness (A)			
	Position 1	Position 2	Position 3

Break off piece for TLM measurements

RIE (for Ge) in RIE 790

- Clean RIE using O_2 plasma for 20 min: 30 sccm, 80 mTorr, 300 W, DC bias
- Condition chamber for 10 mins: CF_4 plasma for 20 min: 25 sccm, 25 mTorr, 100 W, DC bias
- Expected etch rate: 3.8 nm/s
- Etch for 53 s which results in 200 nm etch depth. DC bias:

Thickness/Roughness (A)			
	Position 1	Position 2	Position 3