SILICON-BASED TUNNEL DIODE TECHNOLOGY

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Abstract

By

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Tunnel diodes have received interest because of their remarkable multivalued $I-V$ characteristic and inherent high switching speeds. The exploration of tunnel diode applications was impeded by the incompatibility of tunnel diode fabrication technology with integrated-circuit processing. Rapid thermal diffusion from spin-on diffusants is the particular focus of this work as a basis for establishing a rapid thermal processing method compatible with commercial foundry processes.

Vertical tunnel diodes formed on high resistivity substrates have been demonstrated to allow S-parameter measurements and extraction of a full ac device model. A current density of 2.7 $\mu$A/µm$^2$ and peak-to-valley current ratio (PVR) of 2.25 has been achieved, which is the best result ever achieved using spin-on diffusants. Several other approaches were also explored such as flash-lamp annealing and rapid thermal annealing from doped metal sources. Phosphorus activation was improved using flash-lamp annealing. Tunnel diodes were formed by rapid thermal annealing from an Al:B:Si source on Si with a peak
current density of 2.7 \( \mu A/\mu m^2 \). Backward diodes were formed by evaporating 50 and 100 nm undoped Ge layer as well as 100 nm Al on an \( n^+ \) Ge. This indicates that the undoped amorphous Ge was successfully transformed into heavily doped crystalline Ge. Transmission Electron Microscopy (TEM) was taken which allow characterization of the regrown layer thickness. TEM also showed that the regrown layer is clearly epitaxial and free of defects. The potential and limitations of each approach is discussed in this work.
To my beloved daughter and husband
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CHAPTER 1:  
INTRODUCTION

The interband tunnel diode, also known as the Esaki diode, was first discovered by Leo Esaki in 1957 [1] when exploring internal field emission in heavily-doped reverse biased germanium p-n junctions. He observed the distinctive N-shaped current-voltage (I-V) characteristic of this same junction when biased in the forward bias direction similar to the I-V characteristic of the Si tunnel diode shown in Figure 1.1.

Following Esaki’s discovery, tunnel diodes have received interest because of their remarkable multivalued I-V characteristic and inherent high switching speeds. They have been used in circuits such as amplifiers [2], oscillators [3], pulse generators [4], and analog-to-digital converters (ADCs) [5]. More recently it has been shown that incorporating tunnel diodes (Esaki diodes or resonant tunneling diodes (RTDs)) with transistors can improve circuit performance [6], by increasing the speed of signal processing circuitry or decreasing power consumption at the same speed. A variety of these hybrid III – V transistor/RTD circuits have been demonstrated, e.g., ADCs [7] and oscillators [8]. A new tunnel diode differential comparator has been proposed [9] which lowers power dissipation by a factor of two relative to a transistor-only comparator while also increasing speed.
Tunnel diodes have also been applied to memory circuits where topologies have been proposed to reduce static power dissipation relative to conventional approaches. Van der Wagt demonstrated that static random access memory (SRAM) cells utilizing low current density diodes (≈ 1 A/cm²) can save power and area (4 times smaller) [10] compared to transistor-only SRAM cells. Discrete tunnel diodes have also been used as signal sources in the radio-frequency range [11] to perform noncontact resistivity measurements. In this approach, the tunnel diode is used to power an LC tank circuit, whose frequency of oscillation changes when the samples are inserted into the inductor core. The change in
frequency is related to the skin depth which is in turn related to resistivity.

In the 1960s and 1970s, the exploration of tunnel diode applications was impeded by the incompatibility of tunnel diode fabrication technology with integrated-circuit (IC) processing [12]. Early approaches for tunnel diode fabrication used alloying of dopant-rich metals onto heavily-doped substrates of Ge [13], Si [14], GaSb, or InP [15]. More recently, Si tunnel diodes have been formed by a variety of techniques including molecular beam epitaxy (MBE) [16], implantation [17], ultra-high-vacuum chemical-vapor-deposition (UHV-CVD) [18], and rapid thermal diffusion from spin-on diffusants [19]. The latter approach is a particular focus of this work as a basis for establishing a rapid thermal processing method compatible with commercial foundry processes.

Tunnel diodes were demonstrated for the first time at Notre Dame using proximity rapid thermal annealing and spin-on diffusants [19]. Since this time, vertical tunnel diodes formed on high resistivity substrates have been demonstrated to allow S-parameter measurements and extraction of an ac device model [20]. A current density of 2.7 \( \mu \text{A}/\mu \text{m}^2 \) and peak-to-valley current ratio (PVR) of 2.25 has been achieved, which is the best result ever achieved using spin-on diffusants. Several other approaches were also explored such as flash-lamp annealing and rapid thermal annealing from doped metal sources. The potential and limitations of each approach is discussed in this work.

In prior work, silicon tunnel diodes have achieved an oscillation frequency as high as
48 GHz [21]. A transmission line pulse generator has been previously demonstrated using InP-based RTDs [22]. A mask set and process for realizing these circuits was designed and laid out and is described in Appendix 1.

The dissertation is organized as follows. In chapter 2, the theory of interband tunneling is reviewed to establish the device attributes required to achieve high current densities. In chapter 3, a fabrication process for vertical tunnel diodes is outlined. The process flow and mask set designed to fabricate vertical tunnel diodes and integrated circuits, is further described. In chapter 4, vertical tunnel diode characterization is described. In chapter 5, tunnel junction formation using flash annealing is described. Flash annealing is a nonequilibrium process with heating and cooling rates at around $10^5$ °C/s. Flash annealing was explored because of its potential to increase the activation of impurities while limiting diffusion. In chapter 6, tunnel junction formation using spin-on diffusants and doped metal source is discussed. Chapter 7 summarizes the thesis and outlines areas for future research.
CHAPTER 2:
TUNNELING THEORY

2.1 Tunnel Diode Current-Voltage Characteristics

The nonlinear $I-V$ characteristic of an Esaki tunnel diode originates from electron transport across a degenerately doped $p+n+$ junction. Heavy doping (typically $> 10^{19}/\text{cm}^3$) in these junctions creates high electric fields, exceeding two million volts per centimeter, across a depletion layer of several nanometers. Across this thin depletion layer, electrons can quantum-mechanically tunnel. The tunneling phenomenon is responsible for a high conductance near zero bias. A negative differential resistance (NDR) arises in the tunnel diode in a small range of biases typically between approximately 100 and 300 mV.

The current-voltage characteristic of an Esaki diode can be qualitatively explained using the band diagram and $I-V$ characteristic shown schematically in Figure 2.1. When a reverse bias is applied, Figure 2.1(a), current flows by electron tunneling from occupied states on the $p$-side valence band into unoccupied states in the $n$-side conduction band. In equilibrium, with no applied bias, Figure 2.1(b), the net tunneling current is zero. When a forward bias is applied, current flows by electron tunneling from occupied states in the $n$-side conduction band into unoccupied states in the $p$-side valence band. Maximum
alignment between electrons on the \( n \) side and holes on the \( p \) side gives rise to a peak current, \( I_p \), at a voltage, \( V_p \), as labeled in Figure 2.1(c). When the conduction band minimum on the \( n \) side is raised above the valence band maximum on the \( p \) side, the valley current, \( I_v \), results at a voltage, \( V_v \), Figure 2.1(d). With further increase in the voltage, the current increases due to tunneling through defect states in the depletion layer and thermionic emission over the diode internal barrier, Figure 2.1(e).

The static \( I-V \) characteristic of a tunnel diode is the superposition of three primary current transport paths: band-to-band tunneling current, excess (defect-assisted) current,
and thermal current [23], as shown in Figure 2.2. At low forward bias, current flow in the junction is dominated by band-to-band tunneling. For biases exceeding the valley current ($\sim 2 V_P$), the current is considerably higher than the thermionic diode current, and this current is called the excess current. The excess current is attributed to tunneling of electrons through the energy gap via intermediate levels within the gap [24, 25]. Two possible origins of intermediate levels in the forbidden gap are impurities and lattice defects [26]. At high bias the current flows by thermal emission across the forward-biased $p$-$n$ junction. The excess current typically limits the PVR.

For circuit simulations a SPICE (Simulation Program for Integrated Circuits Emphasis) model is needed. The measured $I$-$V$ characteristics of the interband Esaki tunnel diode are well described by the the Broekaert resonant tunneling diode (RTD) SPICE model [7]. The three current components just discussed, Figure 2.2, can be unraveled by fitting the measured $I$-$V$ characteristic, as shown for a commercial Ge tunnel diode. The first two terms in the Broekaert model are tunneling terms. The first term models the primary tunneling current giving rise to the peak in the $I$-$V$ characteristic. The second term in the RTD models the second resonance state, which in the Esaki tunnel diode, models the excess, defect-assisted tunneling current. The third term in the Broekaert models describes the thermionic current. This fit to the Broekaert model was first shown in reference [27].
Figure 2.2: Measured current-voltage characteristics (open circles) of a Ge Esaki diode (TD266, Germanium Power Devices, Andover, MA). Three current components, band-to-band tunnel current, excess/valley current, and thermal/diffusion current, are shown.

2.2 Tunneling Current Density

The tunneling process in semiconductors can be either direct or indirect defined by whether or not the conduction-band minimum and the valence-band maximum have the same position in k-space. Direct tunneling is observed in semiconductors with direct bandgap, such as GaAs and GaSb. Indirect tunneling can be seen in semiconductors with indirect bandgap, such as Ge and Si. To conserve momentum in indirect semiconductors phonon or impurity scattering is required.

An analytic expression for tunneling current density in a $p^{+}n^{+}$ junction is given by
Sze [28] for the indirect tunneling case,

\[
J_t = \frac{\sqrt{2} q^3 m^{*1/2} \xi V_a}{4\pi^2 \eta^2 E_g^{1/2}} \exp\left(-\frac{4\sqrt{2} m^*(E_g - \eta \omega)^{3/2}}{3q \eta \xi}\right), \tag{2-1}
\]

where \( q \) is the electron charge, \( m^* \) is the carrier effective mass, \( \xi \) is the maximum junction electric field, \( V_a \) is the applied reverse voltage, \( \eta = h/2\pi \) is Planck’s constant, \( E_g \) is the bandgap of the semiconductor (for Si \( E_g = 1.12 \) eV at 300 K), and \( \eta \omega \) is the phonon energy. The phonon term is small compared to the bandgap energy (0.063 eV for the optical phonon in Si) and can be ignored.

To maximize the current density in a tunnel junction, Eq. (2-1) shows that effective mass, energy bandgap, and peak internal electric field are the primary design variables. For example, SiGe and Ge have lower energy bandgap and lower effective mass compared to Si, hence higher tunneling current. For a given material with a fixed bandgap and effective mass, the way to increase current density is to increase the junction internal electric field. The maximum electric field in an abrupt \( p-n \) junction, is related to the thickness of the depletion layer, \( W \), by

\[
\xi = \frac{2(V_{bi} - V_a)}{W}, \tag{2-2}
\]

where \( V_{bi} \) is the junction built-in voltage. The depletion layer thickness is given by

\[
W = \sqrt{\frac{2e}{q} \frac{V_{bi} - V_a}{N_{eff}}}, \tag{2-3}
\]

where \( N_{eff} \) is the effective doping density which can be calculated using
\[ N_{\text{eff}} = \frac{N_A N_D}{N_A + N_D}, \quad (2-4) \]

where the terms \( N_A \) and \( N_D \) are the acceptor and donor densities, respectively. Using Eqs. (2-2) and (2-3), the expression for electric field becomes

\[ \xi = \sqrt{\frac{2qN_{\text{eff}}}{\epsilon}(V_{bi} - V_a)}, \quad (2-5) \]

From Eq. (2-5), it is clear that to obtain a high electric field, high dopant densities are required. Figure 2.3 plots current density as a function of the maximum electric field for an applied forward bias of 0.1 V, for Si. Also shown is the effective doping density required to obtain the corresponding electric field. For example, to obtain a current density of 1 mA/µm² in Si, an electric field of around 5 MV/cm and an effective doping density of \( 7 \times 10^{19} \) cm\(^{-3} \) are required.

The predictions in Figure 2.3 assume abrupt doping profiles; however, abrupt doping profiles are not achieved in practice. To understand the effect of a finite doping slope on the junction electric field, it is necessary to incorporate the effect of doping abruptness in the calculation of electric field. The maximum electric field in a \( p-n \) junction, for a given doping profile, can be evaluated by using a one-dimensional (1-D) Poisson solver. A profile, roughly approximating the diffusion of B into a homogeneous \( n \)-type P density is shown in Figure 2.4. The \( p \)-type doping density as a function of distance beginning at some distance from the surface where the doping density begins to change, is given by

\[ N_A = N_{A0} \exp(-ax), \quad (2-6) \]
where $N_{Ao}$ is the solid solubility of the $p$-dopant, $x$ is the distance from the start of the doping gradient and $a$ is a measure of the doping abruptness, given by

$$a = \frac{1}{d} \ln(10), \quad (2-7)$$

where $d$ is the distance over which the doping density decreases by a factor of ten. With this doping profile the electric field can be calculated numerically as a function of doping density and doping abruptness.

Figure 2.3: Tunneling current density in an abrupt $p$-$n$ junction as a function of the maximum electric field for an applied forward bias of 0.1 V, and the corresponding effective doping density required to achieve it.
Figure 2.4: Schematic doping profile for electric field calculation. $N_A$ and $N_D$ are the acceptor and donor densities, respectively.

The dependence of electric field vs. junction abruptness is shown in Figure 2.5, computed using the software Simwindows [29] which gives the energy band profile and electric field for any input doping profile. It can be seen from Figure 2.5 that at a slope of 5 nm/decade, the effective doping density required to attain the electric field of 5 MV/cm is approximately $2 \times 10^{20}$ cm$^{-3}$, which is significantly higher than the effective doping density needed for an abrupt junction, $7 \times 10^{19}$ cm$^{-3}$. 
The effective doping density achievable at any temperature in an equilibrium process is limited by the solid solubility of the dopants. Nobili [30] gives the following Arrhenius equation for solid solubility of B and P in Si which fits well to experimentally determined values,

\[ \text{Nss} = A \exp\left(-\frac{E}{kT}\right). \]  \hspace{1cm} (2-8)

The values of \( A \) and \( E \) for B and P are listed in Table 2.1. The solid solubility of B and P calculated in this way and including the parameter uncertainty is plotted in Figure 2.6.
TABLE 2.1:
ARRHENIUS EQUATION PARAMETERS FOR THE SOLID SOLUBILITY OF B AND P IN Si [30].

<table>
<thead>
<tr>
<th>Dopant</th>
<th>$A$ ($\times 10^{22}$ cm$^{-3}$)</th>
<th>$E$ (eV)</th>
<th>Temperature range (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boron</td>
<td>9.25  ± 0.04</td>
<td>0.73 ± 0.04</td>
<td>900-1325</td>
</tr>
<tr>
<td>Phosphorus</td>
<td>1.8 ± 0.2</td>
<td>0.40 ± 0.01</td>
<td>750-1050</td>
</tr>
</tbody>
</table>

Figure 2.6: Computed solid solubility of boron and phosphorus in silicon at different temperatures, from the analytic fit of Nobili [30].
From Figure 2.6 it is clear that the solid solubility of boron is lower than that of phosphorus. Therefore diffusing boron into phosphorus-doped Si at the solid solubility limit may be expected to lead to complete compensation of boron in the temperature range 900 to 1100 °C, assuming both dopants are fully electrically activated. Therefore, at the solid solubility limits, P diffused into B should provide a higher current density tunnel junction than B diffused into P-doped Si.

Given the solid solubility limits of B and P in Si, one can estimate the peak junction electric fields that can be achieved in Si with these dopants. This depends explicitly on the solid solubility which depends on anneal temperature. The doping abruptness also depends on temperature. Since doping abruptness can vary, a plot of the effect of dopant abruptness on the electric field is generated for three temperatures and solid solubilities, Figure 2.7. This calculation illustrates that junction fields greater than 5 MV/cm require temperatures of 1000 °C and doping abruptness less than 2 nm/decade. A constant $p$-type dopant (boron) density is assumed throughout the substrate, and the gradient of the $n$-type (phosphorus) is varied from 0 to 5 nm/decade. From Figure 2.7, the doping abruptness to achieve a given electric field can be estimated. For example, to obtain an electric field of 5 MV/cm, a doping abruptness of approximately 2.5 nm/decade at 1100 °C or approximately 1 nm/decade at 1000 °C is required. From Eq. (2-4), it is apparent that if acceptor and donor densities are equal the effective density is half the doping density. Also, considering doping compensation, the junction dopings must, in practice, be 4 times the desired effective density. On diffusing P into B-doped Si, for a given P doping
concentration, a B concentration of half the P concentration is preferred. Therefore, for a P concentration of $4.2 \times 10^{20}$ cm$^{-3}$ at 900 °C, a B concentration of $1.9 \times 10^{20}$ cm$^{-3}$ at 1100 °C should yield the best effective doping concentration.

![Figure 2.7: Junction electric fields vs. doping abruptness and effective doping concentrations for Si doped at the solid solubility limits at the anneal temperatures indicated.](image)

In order to improve dopant abruptness, the thermal cycle used in rapid thermal processing must be minimized without compromising dopant activation. This means high heating and cooling rates, and spike anneals (zero hold time at the peak diffusion temperature) are to be anticipated.
According to the analysis of this section, there appears to be no impediment to achieving 1 mA/μm² junctions by diffusing P into B-doped Si. In practice this has not verified by experiment. The most important issue is that this analysis assumes full electrical activation. Activation is improved by increasing annealing time but at the cost of decreasing the dopant slope. This will be analyzed in chapter 4.

2.3 Tunnel Diode Switching Time

The speed of a tunnel diode is dependent on the slew rate for charging or discharging a capacitance $C$ by a current $i$. The slew rate can be written by $\frac{dV}{dt} = i / C$. The slew rate increases linearly with current for a given device capacitance. The time to switch a tunnel diode from a stable bias point near the peak voltage, to a forward bias point, $V_F$, beyond the voltage of the current minimum has been estimated by Diamond et al. [31]

$$\tau = \left[ \frac{C}{I_p} \right] \frac{V_F - V_p}{1 - \frac{I_v}{I_p}} \frac{V_p}{I_v}, \quad (2-9)$$

where $I_p / C$ is called the speed index, $I_p$ is the peak current, $I_v$ is the valley current, and $I_p / I_v$ is the PVR. The switching time is linearly dependent on the voltage swing and inversely related to the speed index and the PVR.

The capacitance per unit area, $C_j$, of an abrupt $p$-$n$ junction is given by
\[ C_j = \frac{\varepsilon}{W} = \left( \frac{\varepsilon}{2V_{bi}} \right)^\frac{\xi}{\varepsilon}, \]  

(2-10)

where \( \varepsilon \) is the dielectric constant. Both current density and junction capacitance are functions of peak junction electric field and these trade off inversely. When peak junction electric field increases, the current density increases, but the junction capacitance also increases. Fortunately, because of the presence of exponential term in the current density formula, the current density increases faster than the capacitance for fields up to approximately 5 MV/cm, so a speed benefit results from raising the junction current density. This can be seen in Figure 2.8.

![Figure 2.8: Current density and capacitance per unit area of the tunnel diode as a function of peak junction electric field in an abrupt \( p^+n^+ \) junction.](image)

\( J_p \) \hspace{4cm} \( C_j \)

\( E_g = 1.12 \text{ eV} \)
\( m^* = 0.33 m_0 \)
\( V_a = 0.1 \text{ V} \)
\( V_{bi} = 1.1 \text{ V} \)
One useful figure of merit for the tunnel diode is speed index. The speed index is the rate of the voltage change. Due to the faster change of current density compared to the capacitance, the speed index generally increases as we increase the current density, shown in Figure 2.9. Increasing the effective doping concentration can improve the electric field, therefore improving both the peak current density and the speed index.

Figure 2.9: Speed index of the tunnel diode as a function of peak junction electric field in an abrupt $p^+n^+$ junction. The speed index generally increases as the electric field increases.

The switching time of the tunnel diode is improved by increasing the PVR. The effect of PVR and speed index on switching time are estimated using Eqs. (2-1), (2-9), and (2-10), in Fig. 2.10. In this figure, current density is varied from 1 μA/μm$^2$ to 1 mA/μm$^2$. The capacitance for each current density is calculated from the corresponding
electric field. It can be seen in Figure 2.10 that increasing the PVR beyond 3 does not contribute significantly to the device speed.

Figure 2.10: Dependence of switching time on PVR for varying current.

Switching time depends much more strongly on speed index. Figure 2.11 shows the computed switching time vs. speed index for a PVR of 3. A greater decrease in switching time occurs when the speed index increases.
In this chapter, the governing equations and material relationships for designing tunnel diodes have been assembled. The physical properties of the $p^{+}n^{+}$ junction needed to achieve high current density have been described. Doping concentration and dopant abruptness are the most important factors, based on solid solubility and on measured profiles for phosphorus and boron. The relationship between tunneling current density and peak junction electric field as well as effective doping density show that current density of 1 mA/µm² is achievable by diffusing P into B doped Si. Experimental findings and the physics working against dopant activation and the achievement of high dopant slope will be discussed in the following chapters.
CHAPTER 3:

VERTICAL TUNNEL DIODE FABRICATION

In this chapter, vertical tunnel junction fabrication using rapid thermal diffusion from spin-on diffusants is described. The processes use SODs for both the n and p dopants. Phosphorus is diffused first and B is then diffused into the P region. As discussed, diffusion of P into B-doped regions is preferable for achieving high current density junctions. A process flow for this junction is outlined in Appendix 1, and a stepper-based mask set designed in the course of this research is described.

3.1 Rapid Thermal Diffusion from Spin-on Diffusants

In rapid thermal diffusion from spin-on diffusants (SOD) [32-34], a layer of SOD is applied by spinning or spraying onto a wafer surface. Diffusion is then performed in a rapid thermal processor, in this work, a Modular Process Technology RTP-600S, which is a table top unit for 100 mm wafers which uses tungsten-halogen lamps. Diffusion time scales, usually measured in seconds, are characteristic of rapid thermal processing (RTP) as compared to conventional furnace thermal cycles of minutes to hours. Doping from some SODs applied directly to Si, e.g., boron SOD, leaves a residual film on the Si substrate, which is “soft, carbon rich, and insoluble in HF” [35]. Such a film “may
deteriorate device operation” [35]. Residues can be minimized without sacrificing doping density using a technique called proximity rapid thermal diffusion. In this technique, the SOD is applied to a dummy source wafer which is spaced just over or under the device wafer in the RTP.

Specifically, in proximity rapid thermal diffusion [35-37] a SOD is spun onto a cleaned Si wafer, called the source wafer. This dopant source wafer is placed in proximity to a Si device wafer, separated by quartz spacers, with the source wafer typically placed on top of the device wafer with the SOD facing the device wafer, Figure 3.1. With this arrangement, on heating, radiation from the tungsten-halogen lamps heats the wafers from both sides at tens to hundreds of degrees per second to temperatures around 1000 °C. The temperature is monitored by a type-K thermocouple in contact with the back side of the device wafer or a pyrometer. Compared to rapid thermal diffusion in which the spin-on diffusant is in direct contact with the device wafer, proximity rapid thermal diffusion inhibits the formation of a residue layer.
Figure 3.1: Schematic diagram of the proximity rapid thermal diffusion apparatus [35]. The tube, spacer, and tray are quartz; SOD means spin-on diffusant. The temperature of the cooling water is approximately 16 °C.

3.2 Residue Layers

The existence of a residue layer was revealed by secondary ion mass spectroscopy (SIMS) measured after rapid thermal diffusion and after the SOD was removed in a buffered HF (BHF) soak for 5 minutes. Boron impurity profiles in Si, comparing direct rapid thermal diffusion and proximity rapid thermal diffusion are shown in Figure 3.2, [19]. In this figure, SIMS measurements of both the source wafer and the proximity-diffused wafer from the same anneal are shown. It can be seen that the residue thickness was reduced to approximately 5 nm while achieving comparable B concentrations to that achieved with the SOD in direct contact with the wafer. The residue layer is approximately 80 nm in thickness when the dopant is diffused directly from the SOD. For boron SOD, a residual etch-resistant compound insoluble in hydrofluoric acid remains on
the surface following the RTP. It has been proposed from x-ray diffraction measurements [38] that the residue, which forms at the B$_2$O$_3$-Si interface in the temperature range 900 – 1200 °C, closely resembles SiB$_4$ or SiB$_6$.

![Boron profiles](image)

Figure 3.2: Secondary ion mass spectroscopy measurements (Charles Evans Inc.) of boron diffusion into silicon comparing a source wafer in direct contact with the spin-on diffusant with the profile resulting from proximity diffusion into the device wafer, from ref. [19], appendix 5.

3.3 Spin-on Diffusants

Spin-on diffusants have been used for shallow junction formation because of their potential for compatibility with CMOS technology and simplicity [32-34, 37]. The doping sources used in this work to fabricate Esaki tunnel diodes are made by Emusiltone Company, Whippany, New Jersey. The two products used to form n-type and p-type doping are Phosphorosilicafilm $1 \times 10^{21}$ and Borofilm 100, respectively.
Phosphorosilicafilm $1 \times 10^{21}$ has a phosphorus concentration of $1 \times 10^{21}$ cm$^{-3}$. It is an alcohol-soluble Si polymer containing P$_2$O$_5$ and SiO$_2$. Boron 100 has a boron concentration of $5 \times 10^{20}$ cm$^{-3}$. It is a water-based carbon polymer film that contains B$_2$O$_3$.

Proximity rapid thermal diffusion using SODs have been described by Zagozdzon-Wosik, et al. [35]. In this process, a dopant-rich gas is released from the SOD layer onto a wafer adjacent to, but separated from, a device substrate. The released dopant-bearing-compounds (dopant oxide) are evaporated and transported in the gas phase to the surface of the device wafer, followed by surface adsorption, and a surface reduction-oxidation reaction. In this reduction-oxidation reaction, Si is oxidized and the dopants are released and diffuse into the Si. The oxide formed in the redox reaction is removed by buffered HF after the diffusion.

The anneal ambient in proximity rapid thermal diffusion can change the composition of the residue film remaining after the diffusion. For example, it has been observed in this work that for Borofilm 100, oxygen is needed in the diffusion ambient to allow subsequent removal of the residue. One easy way to test whether the residue is resistant to buffered HF is to spin on and anneal the SOD on a thermal oxide. If an oxide step is measured after a BHF etch then the residue had to be removed. If no oxide step is formed then the etch residue must remain. An experiment was designed in which P and B SODs were proximity rapid thermal diffused, in N$_2$ or N$_2$/O$_2$ ambients, over oxide window features (photoresist was used as the etch mask), and then etched in J.T. Baker buffered-
oxide etch (30-50% NH₄OH:40-70% H₂O:0.5-10% HF:surfactant 0.1-0.3%). If the oxide thickness decreases with etch time then the SOD residue must have been removed. Phosphorosilicafilm in pure N₂, Borofilm 100 in pure N₂ and N₂/O₂ (97/3%) respectively were used in this experiment. Thermal oxide, 3000 Å in thickness, was grown on each device wafer, followed by lithography and etching to form oxide windows. The SOD was then spun onto each source wafer. Proximity rapid thermal diffusion was performed at 900 °C for 90 s. The thickness of the oxide window was then measured by step profiling on each device wafer. The wafers were then dipped into J. T. Baker buffered-oxide etch for different etch times and thickness was measured by step profiling after each etch. Figure 3.3 shows the oxide thickness changes after each etch. This plot shows that Emulsitone’s B spin-on diffusant, Borofilm 100, coated on thermal oxide, when annealed at 900 °C for 90 s in pure N₂, leaves a surface layer on the oxide which is resistant to etching in J. T. Baker buffered-oxide etch at room temperature. From the data it is less than 0.18 Å/s based on the error bars. When this SOD is annealed under the same conditions in 97 % N₂ : 3% O₂, the etch rate proceeds at 9.0 Å/s and is comparable to Emulsitone phosphorosilicafilm 1 x 10²¹ SOD annealed under the same conditions on a thermal oxide, which is 8.2 Å/s. Both etch rates are slightly less than the etch rate of the as-grown thermal oxide, which is 9.3 Å/s. The decrease of the etch rate might be caused by the higher density of SiO₂ after the 900 °C anneal. This indicates that the residue of Phosphorosilicafilm diffused in pure N₂ and Borofilm 100 diffused in 97% N₂ : 3% O₂ were removed in 10 % commercial buffered HF.
Figure 3.3: Measurements of oxide thickness after etch in 10% buffer HF for different times. The oxide was covered by SOD proximity diffused at 900 °C for 90 s.
3.4 Vertical Process for Tunnel Diode Fabrication

A process using a wafer-stepper-based mask set has been designed for fabrication of vertical tunnel diodes. The vertical process is shown in Figs. 3.4 to 3.7 with different scales in the x and y directions. This drawing is for a 1 x 1 μm² junction device with a design which assumes a 0.5 μm alignment accuracy. An overview of the process is given here. Starting with an RCA-cleaned, high resistivity, 1000-5000 Ω - cm, 100 mm, (100) Si wafer, a layer of thermal oxide is grown as a diffusion mask, Figure 3.4. Then diffusion windows are opened using the Isolation mask (first mask), followed by phosphorus proximity RTP.

The wafer then is dipped into BHF to remove the SOD residue, Figure 3.5(a); this step thins the thermal oxide. A second layer of oxide is deposited on the wafer by plasma-enhanced chemical-vapor-deposition (PECVD) at a temperature of 250 °C, Figure 3.5(b).
Figure 3.5: Scale drawing of the vertical tunnel diode process: (a) etch to remove SOD residue and (b) plasma-enhanced chemical vapor deposition of oxide.

Diffusion windows are opened using the Emitter mask (Second mask), followed by boron proximity RTP, Figure 3.6(a). Again, the wafer is dipped into BHF to remove the SOD residue and clear the CVD oxide, Figure 3.6(b).
Figure 3.6: Scale drawing of the vertical tunnel diode process: (a) oxide etch followed by boron proximity rapid thermal processing and (b) etch to remove SiO$_2$ and B SOD residue.

Then another layer of PECVD oxide is grown on the wafer and is patterned using the Via mask (third and fourth masks) and etched to remove SiO$_2$ and B SOD residue, Figure 3.7(a). Then a layer of Al is deposited onto the wafer and contacts are patterned by wet chemical etching process in Cyantec’s Al-12 etchant (HNO$_3$, HPO$_3$) using the Bond-Pad mask (fourth mask), Figure 3.7(b).
Figure 3.7: Scale drawing of the vertical tunnel diode process: (a) deposit CVD oxide then etch vias and (b) evaporate Al then wet-chemically etch to form bond-pads.

To minimize parasitic capacitance, it was decided to use benzocyclobutene (BCB) as the dielectric layer which has a permittivity of 2.6 as compared to 4 for that of oxide. However the via etch through BCB involves use of SF$_6$ in a reactive ion etching process. The SF$_6$ gas etches Si and therefore would affect the highly doped Si layers below the
BCB. A new mask set was designed to circumvent this problem by adding a metal layer above the highly-doped Si surface. The BCB is spun after this protective metal layer has been deposited. The details of the mask set are shown in Appendix I.

In this chapter, a fabrication process for vertical tunnel junction formation using rapid thermal diffusion from spin-on diffusants is described. The process flow is outlined. The etch resistance of B SOD was shown to depend on anneal ambient in proximity rapid thermal diffusion. Tunnel diode characterization using this process flow is described in the next chapter.
CHAPTER 4:
TUNNEL DIODE CHARACTERIZATION

The first vertical tunnel diodes formed by rapid thermal diffusion using spin-on diffusants [18] [19] on high-resistivity Si substrates are characterized to enable the extraction of an RF device model. The device model is extracted from dc, microwave S-parameter, and RF impedance measurements. The tunnel diode characteristics are well described by the Schulman-Broekaert model [7] [39], an analytic model developed for the resonant tunneling diode and readily incorporated into SPICE and ADS modeling environments.

4.1 Vertical Tunnel Diode Characterization

Vertical tunnel diodes were made on high resistivity, 1000-5000 Ω - cm, 100 mm, (100) Si substrates. The high-resistivity substrate lowers the parasitic substrate capacitance and current loss in the substrate. It is a four-mask oxide window process on high resistivity substrates. Proximity rapid thermal diffusion of P was done at 900 °C for 1 s, followed by a 90 s driving in process at the same temperature. Proximity rapid thermal diffusion of B was done at 900 °C for 1 s. All diffusions were in pure N₂ ambient with a ramp rate of 30 °C/s to yield the device cross section of Fig. 3.7(b). The residue
was later found to be present when diffuse B in pure N₂ and that it must be either conductive or thin enough for tunneling.

The DC performance of the devices was measured using an Agilent 4155B semiconductor parameter analyzer. The highest measured peak current density obtained was 2.7 μA/μm² shown in Figure 4.1, with a peak to valley current ratio (PVR) of 2.15, which is the best result ever achieved using spin-on diffusants [20]. The best PVR obtained was 2.25. The measurements of the uniformity show a +/- 20% variation in current density for devices spanning a wafer area of 3100 x 3100 μm².

![Figure 4.1: Room temperature current-voltage characteristics of tunnel diodes formed on high resistivity Si substrates with highest peak current density.](image-url)

The microwave frequency S-parameters of these diodes were measured from 45 MHZ to 30 GHz, using an Agilent 8510XF vector network analyzer with a port power of
-33 dBm. A two-port LRM (line-reflect-match) calibration was performed using a Cascade Microtech 104-783 Impedance standard substrate. The measured S-parameters were de-embedded from the probe pads using a $\pi$ - equivalent circuit model. Excellent agreement between the measured S-parameter $S_{11}$ and simulated $S_{11}$ based on the equivalent circuit model at zero bias is shown. RF characterization of the diode was done by coauthor Qingmin Liu [20], Appendix 2.

The low frequency impedance of the above diodes has been analyzed over a frequency range of 0.5 MHz to 100 MHz. The impedance measurements were made using an Agilent 4294A precision impedance analyzer, over a bias range from 50 to 600 mV with a step of 50 mV. Figure 4.2 shows the equivalent circuit model used to represent the device, where $R_S$ is the device series resistance, $C_D$ is the junction capacitance, and $G(V)$ represents the bias dependent conductance of tunnel diode current-voltage characteristic. The parasitic effects of the Si/oxide capacitance underneath the bondpads must be accounted for to extract the intrinsic characteristic of the tunnel junction, where $R_I$ and $C_I$ represent the parasitic substrate resistance and bond-pad capacitance, respectively. From the frequency dependence of the measured impedance we extracted $R_S$, $C_D$, $G(V)$, $C_I$, and $R_I$ at all bias points. A comparison of the differentiated conductance of the I-V to the extracted conductance from the impedance measurements confirms that the model is reasonable and consistent across two measurement techniques.
Figure 4.2: Equivalent circuit model for impedance measurements.

In Figure 4.3 the $I-V$, $C-V$, and $G-V$ data of the same device are plotted. The derivative of $I-V$ data is excluded in the NDR region because the $I-V$ curve shows obvious oscillation. The good agreement between the differential conductance of the tunnel diode extracted from the impedance measurement and the derivative of the dc current-voltage curve is shown in Figure 4.3(c). From the peak current density, the corresponding electric field can be estimated from Figure 2.3, and this used to estimate the capacitance of an abrupt tunnel diode, Eq. (2-10). The capacitance obtained in this way is approximately $13 \text{ fF/}\mu\text{m}^2$. This result is about half of the measured value shown in Figure 4.3(c), a result that is surprising because less capacitance than the theoretical value
would be expected with our diffusion process. The capacitance should increase as the forward bias increases, since the depletion width decreases with increasing bias, and capacitance would therefore increase. This is observed between 50 and 100 mV of forward bias. A decrease in capacitance with bias was observed between 100 mV and 200 mV which is surprising. Similar results were found by Dashiell [40] et al. and is still unexplained.

The current density achieved in these experiments may be limited by the P activation levels. Even though the solid solubility of P is higher than that of B at the temperatures used in the experiments, diffusing B into P still yielded tunnel diodes. This has been observed in the work of Jinli [19]. An estimation of the P activation level can be obtained by the following reasoning. The highest possible electrically-activated acceptor concentration is given by the solid solubility of B at 900 °C, which is $7 \times 10^{19}$ cm$^{-3}$. The net acceptor density must take into account the compensation due to donors and is given by $(N_A-N_D)$. Since NDR is observed in the I-V characteristic the net acceptor density must be degenerate, at least equal to $N_V$, $1.04 \times 10^{19}$ cm$^{-3}$ for Si. This sets the upper bound that the n-type doping can not exceed $N_A-N_V$, which is $\sim 6.0 \times 10^{19}$ cm$^{-3}$. The lower bound is given by the doping necessary for degeneracy on the n-side of the junction. $N_C = 2.8 \times 10^{19}$ cm$^{-3}$ for Si. This implies that at the temperatures used, the P doping density obtained by the rapid thermal process is lower than the expected solubility of P and lower than that of B.
Figure 4.3: Measured (a) current-voltage ($I$-$V$), (b) capacitance extracted from impedance measurements as a function of frequency, and (c) comparison of the differential conductance of the tunnel diode extracted from the impedance measurement with the derivative of the dc current-voltage curve ($G$-$V$) showing good agreement.
4.2 Effect of Contact Anneals on Current Density and PVR

Post-metallization Al contact anneals were explored to see whether peak current density and PVR could be improved. Aluminum makes a good contact to heavily-doped Si because Al reduces the native SiO$_2$ [41]; Al also anneals out interface traps at the Si-SiO$_2$ interface [41]. The contact anneals were done by rapid thermal anneal in forming gas at a peak temperature of 300 °C, chosen to avoid Al spikes, and with a hold time of 30 s. Figure 4.4 shows the peak current density and PVR vs. metallization anneals. Rapid thermal anneals improved both current density and PVR. The sample was annealed and tested after every thermal cycle, from 1 cycle to 13 cycles. It was found that after the first cycle, the peak current density was improved by around 15% - 18%; the PVR was improved by around 15% - 17%. After the 13$^{th}$ cycle, the peak current density was improved by around 22% - 29%; the PVR was improved by around 20% - 23%. These effects are consistent with an increase in dopant activation and trap passivation leading to higher peak current density at lower voltage and lower excess current. It is obvious that post-metallization clearly didn’t activate all the P for these 13 cycles, since that would have destroyed tunnel diode.
4.3 Tunnel Diode Oscillator

When biased in the NDR region of the I-V characteristic, a tunnel diode oscillates. The oscillations occur when making DC measurements in the NDR region. The $I$-$V$ characteristic of a typical tunnel diode with oscillation is shown in Figure 4.5. By biasing this tunnel diode at 0.275 V using a 4155 semiconductor parameter analyzer, with a Tektronix oscilloscope attached to the two terminals of the tunnel diode, we observed the oscillation of Figure 4.6. The oscillation frequency was measured to be approximately 190 kHz. The intrinsic response time, estimated to be $f = I_p / (2C_D \Delta V) \approx 450$ MHz, is lowered by the parasitic capacitance of our measurement configuration.
Figure 4.5: I-V characteristic of a typical tunnel diode with oscillation occurring in the voltage range from 0.2 to 0.3 V.

Figure 4.6: Silicon tunnel diode oscillator on-wafer biased at 0.275 V and exhibiting a characteristic frequency of 190 kHz. (The same diode as in Fig. 4.5)
A set of pulse generator circuits has been designed and laid out based on an RTD-bridge by Broekaert [42]. Three oscillator frequencies were designed: 2, 10, and 20 GHz and this mask set is outlined in Appendix 3.

In this chapter, Si tunnel diodes were demonstrated using spin-on diffusants in a four-mask oxide window process on high resistivity substrates. The microwave frequency S-parameters and low frequency impedance measurements were shown. Comparison of the differential conductance of the tunnel diode extracted from the impedance measurement with the derivative of the DC measurement showed good agreement. Post-metallization Al contact anneals were explored to see the effect of contact anneals on current density and PVR. The tunnel diodes oscillator was demonstrated. The limitation of current density achieved in this technique was analyzed.
5.1 Introduction

High doping density and abrupt doping profiles are important to achieve high current density, however, there is a tradeoff. As temperature is increased to improve doping activation and raise the solid solubility of the dopant, the doping abruptness degrades. To optimize the temperature – time profile of the RTP becomes the primary control variable. Increasing ramp up and ramp down rates of RTP has been used to decrease lateral diffusion of ion implanted B and As during the spike anneal by reducing the effective diffusion time [43, 44], therefore minimize the spreading of the doping profile.

Recently an extension of conventional spike RTP, called Flash-assist RTP™ (fRTP) [45], has been developed for activating impurities while limiting diffusion. Conventional spike anneal using traditional tungsten-halogen lamps has effective diffusion times on the order of about 1.5 seconds or more [45]. Since the highest active doping concentration at equilibrium is limited by the solid solubility, a nonequilibrium process is needed to obtain higher active concentration. In fRTP, an arc lamp with continuous operation up to 750 kW is used to heat the bulk of the wafer to an intermediate temperature (Tᵢ), and then an
additional source of radiant energy with pulsed power up to 100 MW is used to heat a thin layer on the device side of the wafer to reach the peak temperature ($T_f$). A schematic time-temperature profile of this process is shown in Figure 5.1. The ramp-up rate to the intermediate temperature is similar to a spike anneal but with faster ramp up rate (up to 400°C/s). Since only a thin layer (~100 microns) is heated above the intermediate temperature and for only a few milliseconds, the rest part of the wafer remains at the intermediate temperature (which is several hundred degrees lower than the top layer) and acts as a heat sink during cooling. Therefore much faster heating and cooling rates ($\sim 10^5$ °C/s) above the intermediate temperature are achieved.

![Diagram of time-temperature profile](image)

Figure 5.1: Schematic time-temperature profile of an fRTP process [45]. $T_i$ is the substrate temperature before striking the flash; and $T_f$ is the peak temperature during the flash.
Recently, it has been demonstrated [46] that by carrying out millisecond single flash anneals using fRTP at $T_f$ of 1050 °C, active electrical B concentration as high as $6.5 \times 10^{20} \text{ cm}^{-3}$ can be achieved, which is well above the solid solubility of $1.5 \times 10^{20} \text{ cm}^{-3}$. Using a second flash anneal at a higher peak temperature (best activation at $T_i = 700^\circ\text{C}$, $T_f = 1150^\circ\text{C}$) resulted in approximately two orders of magnitude reduction in leakage currents compared to the single flash anneals [46]. The technique also resulted in a doping abruptness comparable to the as-implanted profile (~ 3.8 nm/dec). This technique improves the active doping concentration while minimizing the doping slope change, both of which could improve the current density in tunnel diodes.

A joint experiment with Vortek Industries Ltd. (now part of Mattson Technology Canada) using flash anneals of SOD $p^+n^+$ junctions was explored. Since P has a higher solid solubility than B in the diffusion temperature range of interest, a P diffusion into B-doped Si can produce higher junction concentrations. In this work flash anneals were intended to improve the P activation without degrading the inverse dopant slope. The anneal conditions are given in Table 5.1. The experiment matrix consists of two groups of samples, with the intermediate temperature of 700 °C and 800 °C, respectively. As a matter of practice, the maximum achievable temperature rise between the intermediate temperature and the peak temperature is 600 °C. Each group has the temperature rise between the intermediate temperature and the peak temperature of 450 °C, 525 °C, and 600 °C, respectively.
TABLE 5.1: 
FLASH ANNEAL CONDITIONS IN VORTEK

<table>
<thead>
<tr>
<th>Group Number</th>
<th>Wafer number</th>
<th>T₁ (oC)</th>
<th>Tᵣ (oC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>group 1</td>
<td>Y248-1</td>
<td>Y249-1</td>
<td>Y250-1</td>
</tr>
<tr>
<td></td>
<td>Y248-2</td>
<td>Y249-2</td>
<td>Y250-2</td>
</tr>
<tr>
<td></td>
<td>Y248-3</td>
<td>Y249-3</td>
<td>Y250-3</td>
</tr>
<tr>
<td>group 2</td>
<td>Y248-4</td>
<td>Y249-4</td>
<td>Y250-4</td>
</tr>
<tr>
<td></td>
<td>Y248-5</td>
<td>Y249-5</td>
<td>Y250-5</td>
</tr>
<tr>
<td></td>
<td>Y248-6</td>
<td>Y249-6</td>
<td>Y250-6</td>
</tr>
</tbody>
</table>

5.2 Properties of B and P RTP Used in Flash Anneal Experiments

The junctions consist of an ultrashallow P layers (approximately 3.5 nm at 2 x 10²⁰ cm⁻³) diffused into a heavily-doped B layer by rapid thermal annealing. The experiment was carried out using n-type Si (100) substrates. SIMS measurements of boron (Y183) and phosphorus (W31) diffusions which used the same diffusion conditions are shown in Figure 5.2. Boron was diffused from Borofilm 100 at 1100 °C for 30 s with a ramp rate of 30 °C/s in 97N₂:3O₂ ambient, by proximity rapid thermal diffusion from an SOD-coated source wafer, to a half-concentration diffusion depth of 300 nm. The wafers were then dipped into buffered HF for 30 s to remove the SOD residue. Thermal oxidation and buffered HF were used to remove the top 30 nm shown in Figure 5.2 (The surface was hydrophobic after the treatment). Phosphorsilicafilm 1 x 10²¹ was then diffused at 900 °C for 1 s with a ramp rate of 70 °C/s in pure N₂ ambient by proximity rapid thermal diffusion from an SOD-coated source wafer. A doping slope of approximately 2
nm/decade was estimated from the SIMS results (also shown in Figure 5.2). The wafers were then cleaved into approximately 1 x 1 cm² pieces and dipped into buffered HF for 30 s to remove the SOD residue (control wafer).

Figure 5.2: SIMS phosphorus and boron diffusion profiles in Si: phosphorus diffusion at 900 °C for 1 s (W31), and boron diffusion at 1100 °C for 30 s (Y183). Two SIMS measurements from two different wafers, superimposed (Courtesy Brian Doyle, Intel).

Table 5.2 shows the target anneal conditions and resultant anneal conditions (as supplied by Vortek) for each sample. The peak temperature of the top side of the wafer was measured with a very fast radiometer in the full wafer systems and the back (bulk) temperature was also measured with another radiometer. In the small sample tool as in our case, only the back side was measured, but the front side temperature was modeled using the amount of energy delivered to the front and this can
be determined from the increase in back side temperature after the flash. Sample Y248-1 was used for the set-up of the intermediate temperature and to determine the flash energy to achieve the required temperature jump. For calibration a piece of the wafer was melted so the back side radiometer could be properly calibrated. On completion, a series of flashes at various capacitor bank energies were performed on the sample to establish a temperature calibration. Some of the flashes occurred at a lower intermediate temperature than expected resulting in a lower peak temperature. For most samples, $T_i$ and $T_f$ fell within 10% compared to the requested temperature.
### TABLE 5.2:
FLASH ANNEAL CONDITIONS FROM VORTEK

<table>
<thead>
<tr>
<th>Wafer number</th>
<th>(T_i) (°C) target</th>
<th>(T_f) (°C) target</th>
<th>(T_i) (°C) resultant</th>
<th>(T_f) (°C) resultant</th>
</tr>
</thead>
<tbody>
<tr>
<td>control</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Y248-1</td>
<td>700</td>
<td>1150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Y248-2</td>
<td>700</td>
<td>1225</td>
<td>762.4</td>
<td>1116.9</td>
</tr>
<tr>
<td>Y248-3</td>
<td>700</td>
<td>1300</td>
<td>743.6</td>
<td>991.3</td>
</tr>
<tr>
<td>Y248-4</td>
<td>800</td>
<td>1250</td>
<td>866.3</td>
<td>1243.0</td>
</tr>
<tr>
<td>Y248-5</td>
<td>800</td>
<td>1325</td>
<td>872.2</td>
<td>1282.4</td>
</tr>
<tr>
<td>Y248-6</td>
<td>800</td>
<td>1400</td>
<td>873.0</td>
<td>1287.8</td>
</tr>
<tr>
<td>Y249-1</td>
<td>700</td>
<td>1150</td>
<td>765.6</td>
<td>1138.3</td>
</tr>
<tr>
<td>Y249-2</td>
<td>700</td>
<td>1225</td>
<td>738.0</td>
<td>953.9</td>
</tr>
<tr>
<td>Y249-3</td>
<td>700</td>
<td>1300</td>
<td>738.0</td>
<td>953.9</td>
</tr>
<tr>
<td>Y249-4</td>
<td>800</td>
<td>1250</td>
<td>864.5</td>
<td>1231.0</td>
</tr>
<tr>
<td>Y249-5</td>
<td>800</td>
<td>1325</td>
<td>877.1</td>
<td>1315.2</td>
</tr>
<tr>
<td>Y249-6</td>
<td>800</td>
<td>1400</td>
<td>881.1</td>
<td>1341.9</td>
</tr>
<tr>
<td>Y250-1</td>
<td>700</td>
<td>1150</td>
<td>787.5</td>
<td>1284.7</td>
</tr>
<tr>
<td>Y250-2</td>
<td>700</td>
<td>1225</td>
<td>773.2</td>
<td>1189.1</td>
</tr>
<tr>
<td>Y250-3</td>
<td>700</td>
<td>1300</td>
<td>774.7</td>
<td>1199.1</td>
</tr>
<tr>
<td>Y250-4</td>
<td>800</td>
<td>1250</td>
<td>870.5</td>
<td>1271.1</td>
</tr>
<tr>
<td>Y250-5</td>
<td>800</td>
<td>1325</td>
<td>877.9</td>
<td>1320.5</td>
</tr>
<tr>
<td>Y250-6</td>
<td>800</td>
<td>1400</td>
<td>890.4</td>
<td>1404.0</td>
</tr>
</tbody>
</table>

5.3 I-V Measurements of fRTP-Tunnel Junctions

Samples Y248-2, Y248-3, Y248-4, Y248-5, Y248-6, as well as a control sample (without any flash anneal) were processed for I-V measurements. The wafers were etched briefly in buffered HF before a layer of 200 Å Ti and 2000 Å Au was evaporated to form contacts in a lift-off process. A mesa was then formed by reactive ion etching (RIE) using CF\(_4\)/O\(_2\) for 1 minute to achieve an etch depth of approximately 49 nm. Therefore the
mesa height was greater than the \textit{p-n} junction depth by approximately 45 nm. The \textit{I-V} measurements were made using a front-to-front probe configuration, where one probe was used to contact the device area 10 x 10 \(\mu\)m\(^2\), and the other probe was placed on a bigger pad of area approximately 350 x 450 \(\mu\)m\(^2\).

The currents for both forward and reverse bias of the control sample were higher than flash annealed samples. For the flash annealed samples, both the forward and reverse currents increase as the peak temperature goes higher, but stop increasing after the peak temperature of 1243 °C. The control sample did not yield NDR. This may be due to a low \(P\) activation level during the RTP anneal done at 900 °C, 70 C/s, 1s. A low activation level of \(P\) compensated by the \(B\) already present in the sample may result in a low-barrier Schottky diode as shown in Fig. 5.3(a). This would explain the high reverse and forward bias currents. The flash annealing resulted in a more rectifying behavior in these diodes. It is inferred that the flash anneal increased the \(P\) doping density, making the surface more \textit{n} type than in the control sample. This resulted in a higher barrier and reduced reverse current as seen in the \textit{I-V}. As the flash anneal temperature further increased, the reverse current increased which might come from tunneling. However, the \textit{I-V} show that the resulting activation is not enough to make the surface degenerate, as an NDR was not achieved.
Figure 5.3: (a) Energy band diagram for a Schottky diode corresponding to the “control” current-voltage characteristic; (b) energy band diagram for a diode corresponding to the flash-annealed current-voltage characteristics; (c) current-voltage characteristics for “control” and flash-annealed samples as a function of flash-anneal temperatures.

Multiple flash anneals can be expected to further activate doping concentrations but also enable additional diffusion and degradation of the inverse doping slope. Therefore, optimization may provide a better result. Several wafers with similar anneal temperature in the first flash anneal were sent back to Vortek for multiple flash anneals. Table 5.3 shows the target anneal conditions and resultant anneal conditions for each sample. The requested number of flash anneals doesn't include the initial flash anneal. Figure 5.4 shows the current density vs. voltage of multiple-flash-annealed samples as a function of applied bias. The current increased after 2 flash anneals, but degraded after 3 and 4 flash anneals.
### TABLE 5.3:
MULTIPLE FLASH ANNEAL CONDITIONS FROM VORTEK

<table>
<thead>
<tr>
<th>Wafer number</th>
<th>Number of flash anneals</th>
<th>$T_i$ ($^\circ$C) requested</th>
<th>$T_f$ ($^\circ$C) requested</th>
<th>$T_i$ ($^\circ$C) resultant</th>
<th>$T_f$ ($^\circ$C) resultant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y249-4</td>
<td>1</td>
<td>800</td>
<td>1325</td>
<td>877.5</td>
<td>1317.8</td>
</tr>
<tr>
<td>Y250-1</td>
<td>1</td>
<td>800</td>
<td>1325</td>
<td>881.4</td>
<td>1343.9</td>
</tr>
<tr>
<td>Y249-5</td>
<td>2</td>
<td>800</td>
<td>1325</td>
<td>879.1</td>
<td>1328.5</td>
</tr>
<tr>
<td>Y250-3</td>
<td>2</td>
<td>800</td>
<td>1325</td>
<td>879.1</td>
<td>1328.5</td>
</tr>
<tr>
<td>Y249-6</td>
<td>3</td>
<td>800</td>
<td>1325</td>
<td>883.8</td>
<td>1359.9</td>
</tr>
<tr>
<td>Y250-4</td>
<td>3</td>
<td>800</td>
<td>1325</td>
<td>882.2</td>
<td>1349.2</td>
</tr>
</tbody>
</table>

Figure 5.4: Current density - voltage characteristics for multiple flash annealed tunnel junctions.
In this chapter, tunnel diode formation using flash anneal is introduced. $I-V$ measurements of fRTP tunnel junctions are shown for both single flash anneal and multiple flash anneals. It is inferred that the flash anneal increased the active P doping density, however, the $I-V$ show that the resulting activation is not enough to make the surface degenerate, as an NDR was not achieved. Multiple flash anneals were further explored to improve the active P doping density. It was shown that the current increased after 2 flash anneals, but degraded after 3 and 4 flash anneals.
CHAPTER 6:
TUNNEL JUNCTION FORMATION USING AL METAL SOURCE

In this chapter, tunnel junction formation using two Al metal sources has been investigated. In a first experiment an Al:B:Si source was used to introduce both Al and B as \( p \)-dopants into heavily-P-doped Si. In a second experiment Al and Ge were deposited and alloyed to regrow a \( p \)-type SiGe on heavily P-doped Si.

Metals such as Al, Ga, In, are \( p \) dopants in Si, thus deposited metals can be used as dopant sources. These metals can contain other elemental dopants and can also form eutectics with Si thereby lowering their melting points. Group IV metals, such as Sn and Pb, can also be used as dopant carriers for rapid thermal alloying with the underlying semiconductor. Generally, the metal is heated above the eutectic temperature. On cooling, a degenerately-doped semiconductor is regrown. The best result in Si using this alloying method achieved a peak current density of \( 10 \, \mu\text{A}/\mu\text{m}^2 \) with a PVR of 3.8 [14]. Boron and arsenic were used as doping impurities as acceptor and donor impurities respectively and the alloy temperature used was \( \sim 620 \, ^\circ\text{C} \).
6.1 Si Tunnel Diode Formation from Al:B:Si

In this work, an Al:B:Si sources were used, deposited by electron beam evaporation. The composition of the source was 98% Al, 1% B, and 1% Si. The Al was patterned and then wet etched using photoresist as a mask. After rapid thermal annealing, reactive ion etching was used to isolate the devices.

As a first experiment, the Al:B:Si was deposited and patterned on a 30-40 Ω-cm n-type substrate. The wafer was subdivided and annealed at temperatures ranging from 350 to 575 °C for 5 s, and p-n junctions formed. These temperatures ranged from well below the Al:Si eutectic temperature of 577 °C, to near the eutectic. Shown in Fig. 6.1 is the solid solubility of impurity elements in Si [47].

Figure 6.1: Solid solubility of impurity elements in silicon [47].
From diode measurements shown in Fig. 6.2(a), near surface doping of Si from the Al:B:Si source appears to occur even at temperatures as low as 350 °C, well below the temperatures at which diffusion is expected for B or Al in Si. This low temperature doping may result from the out-diffusion of Si into Al and the resulting creation of open Si lattice sites for in-diffusion of B and Al. If the B content of the deposited Al:B:Si alloy is the same as that of the evaporation source (only 1%), it is probable that the concentration of B diffused into the Si significantly lower than assumed in the band diagram. However, even in the absence of B, diffusion of Al into Si would increase the band bending and reduce the reverse current, as observed.

The experimental evidence for this low temperature doping is shown in Fig. 6.2(a) where the current-voltage characteristic of a set of diodes is shown as a function of rapid thermal annealing temperature. A Schottky barrier contact can be expected for the unannealed case as indicated by the computed energy band diagram in Fig. 6.2(b) and consistent with the measured \( I-V \) curve, “no anneal.” For a \( p \)-type surface doping layer, the barrier height of the diode can be expected to increase as shown in Fig. 6.2(c). The band diagram is based on an assumption that B is present at its solubility limit in Si. The measured \( I-V \) characteristics show a decrease in the reverse current as the anneal temperature is increased, consistent with a \( p \)-type surface doping of the diode. At a temperature of 575 °C, the reverse leakage current increases. This could result from Al spiking through the shallow junction which would be expected to increase the leakage
current. Al spike formation occurs because of dissolution of Si into the Al, leaving pits in the Si which are backfilled by Al. Since the deposited alloy contains 1% Si, this should not occur at temperatures below about 500 °C, because the solubility of Si in Al reaches 1% at about 500 °C. However, at 575 °C, dissolution of Si and spike formation should begin, because the solubility of Si in Al is about 1.5%. Due to the short (5 s) anneal time, the junction depth should be shallow enough for penetration by spiking to be possible.

Figure 6.2: Measured current-voltage characteristic (a) for an Al:B/n-Si diode as a function of anneal temperature. The upper energy band diagram in (b) shows the computed energy band profile for an Al/n-Si Schottky diode and in (c) the simulation shows the increase in barrier height resulting from the in diffusion of a box profile of boron concentration at 2 x 10^{20} /cm^3.
This experiment was repeated on a heavily $n^+$ doped substrate ($\sim 2 \times 10^{19} / \text{cm}^3$). In the computed energy band diagrams shown in Figure 6.3(b) the as-deposited Al:B:Si contact can be expected to form a tunnel ohmic contact before annealing and B activation. Upon annealing, the B forms a heavily-doped $p$-surface region, raising the built-in potential and forming a $p^+n$ diode, Figure 6.3(c). An $n$-doping of $2 \times 10^{19} / \text{cm}^3$ is not sufficient to move the Fermi energy significantly into the conduction band so negative differential resistance is not expected. The $I-V$ characteristic for no anneal, Figure 6.3(a), shows the highest currents at the lowest voltage, consistent with the computed energy band diagram for a tunnel ohmic contact. For 350 °C, the forward and reverse currents are essentially the same, which suggest the diffusion depth is still shallow enough that it behaves as a tunneling ohmic contact, but with lower current because the barrier width increases due to compensation doping. For the 425 °C case, the surface doping concentration increases and the backward diode $I-V$ behavior results with higher reverse current than forward current. The increase of forward and reverse currents compared to 350 °C could be due to interband tunneling. For the temperatures 500 and 575 °C the diode curves return to a forward diode character with more forward current than reverse current. At 500 °C, interdiffusion may reduce the abruptness of the junction, decreasing interband tunneling resulting in the lower forward and reverse currents compared to 425 °C. At 575 °C, Al spiking could increase the current, as discussed earlier.
A liquid phase epitaxy process was developed to form tunnel diodes. Proximity rapid thermal diffusion of P was used to form the $n^+$ side of the junction. The deposited Al:B:Si film serves both as an acceptor dopant source and a melt for epitaxial regrowth of $p^+$ Si. The tunnel junction formation process is understood based on the Al-Si binary phase diagram, Fig. 6-4. When the temperature increases below the eutectic temperature $T_E = 577 ^\circ C$, some Al should dissolve into the Si surface, to a depth depending on the
heating rate. At $T_E$, the Al and Si are in contact and melt to form liquid (L) of the eutectic composition (12.2 atomic % Si), which requires dissolving some of the Si substrate. As the temperature rises above $T_E$, the liquid (L) composition, with which the Si substrate would be in equilibrium, moves upwards along the liquidus line on the Si side of the eutectic point. The liquid must therefore dissolve additional Si to become more Si rich. The phase diagram composition values can be used to estimate the depth to which Si will be dissolved. Upon cooling, the liquid should precipitate Si until reaching $T_E$. Since the liquid is already in contact with the Si wafer, no nucleation is necessary, and the new Si solidified, which is Al-saturated and thus $p^+$, should grow epitaxially on the Si surface.
When \( T \) reaches \( T_E \), the eutectic reaction \( L \rightarrow \text{Al} + \text{Si} \) should occur, where both the Al and Si are solid solutions saturated with the other element at the solubility limit. When heating the wafer above \( T_E \), Al consumes an amount of Si which depends on the peak temperature \( T_p \). The ratio of the penetration depth, \( x \), of the melt below the deposited Al of thickness, \( t_{\text{Al}} \), can be determined from the Al-Si binary phase diagram according to the relation,

\[
\frac{x}{t_{\text{Al}}} = \frac{\rho_{\text{Al}}}{\rho_{\text{Si}}} \left( \frac{W_{\text{Si}}}{1 - W_{\text{Si}}} \right)
\]  

(6-1)

where \( \rho_{\text{Al}} \) and \( \rho_{\text{Si}} \) are the densities in \( \text{g/cm}^3 \) for Al and Si respectively, and \( W_{\text{Si}} \) is the weight % of Si in the Al melt. This relation is plotted in Fig. 6.5. For a \( T_p = 600 \, ^\circ\text{C} \) and 100 nm Al, Si should be consumed to a depth of approximately 19 nm.

![Figure 6.5: The ratio of the penetration depth, \( x \), to the Al deposition thickness, \( t_{\text{Al}} \), and acceptor doping density as a function of temperature, as determined from the Al-Si binary phase diagram.](image)
The experiment of P diffusion from SOD phosphorosilica film $1 \times 10^{21}$ was run at diffusion temperature of 900 °C for 1 s using proximity rapid thermal diffusion, followed by driving at 900 °C for 90 s without source wafer, and then rapid thermal processing at 620 °C for 1 s, using Al:B:Si source. Backward diodes or weak tunneling diodes were observed in this experiment. Shown in Fig. 6.6 are the $I-V$ characteristics of three diodes with device area of 10 x 10 μm$^2$. Two backward devices and one tunnel diode were obtained. The reason for device to device variation could be the temperature variation in the RTP chamber. The tunnel diode has a peak current density of 2.7 μA/μm$^2$ with a PVR of 1.02. From Fig. 6.1 it can be seen that the solid solubility of Al and B in Si is low at these temperatures which explains why the tunneling current density obtained was low.
Figure 6.6: I-V characteristics of Si diodes using doped metal source Al:B:Si and P diffusion from spin-on-diffusants. The three curves show variation across the sample.

6.2 Rapid Melt Growth from AlSiGe Melts on $n^+$ Si

At Notre Dame, Ge tunnel diodes have been formed using a rapid-melt-growth technique by regrowing Al-doped $p^+$ layers from an Al:Ge melt on an $n^+$ P-diffused Ge substrate. Peak current densities up to 1.2 mA/$\mu$m$^2$ have been demonstrated [49]. Compared to Si, Ge has the advantage for tunneling of a low transverse effective mass of 0.082 for electrons and an 0.044 light hole effective mass compared to 0.19 and 0.16, respectively, for Si. The lower mass increases tunneling probability and hence tunneling
current density. Also, Ge has a lower bandgap, 0.66 eV, compared to 1.12 eV for Si. The lower density of states in both conduction band, $1.04 \times 10^{19}$ cm$^{-3}$ for Ge and $2.8 \times 10^{19}$ cm$^{-3}$ for Si, and valence band, $6.0 \times 10^{18}$ cm$^{-3}$ for Ge and $1.04 \times 10^{19}$ cm$^{-3}$ for Si, makes Ge much easier to dope degenerately.

It is desirable to develop a process for tunnel junction fabrication on Si rather than Ge substrates. To enable a tunnel junction technology on Si, the following scheme was proposed and explored. Suppose Al and Ge layers are deposited on Si. On heating above the eutectic temperature these should melt to form an Al-Ge-Si liquid that will epitaxially regrow $p^+$ Al-doped Si$_x$Ge$_{1-x}$ on cooling, followed by a eutectic reaction. The Al:Ge ratio can be chosen so that the regrown SiGe is Ge-rich, with a high solubility for Al and thus a highly-degenerate $p^+$ layer should form. Due to the lattice parameter difference, misfit dislocations may be expected to form, and would have a deleterious effect on tunnel junction characteristics, however this may be lessened in submicron junctions, due to the proximity of edges to allow threading dislocations to escape.

6.2.1 Phase Diagram Analysis

This section examines the growth of SiGe from an Al melt. Since Al is a p-dopant, regrowth of $p^+$ SiGe on an $n^+$ substrate may be used to form a $p^+$ SiGe/$n^+$ Si tunnel junction.

In the ternary phase diagram of the Al-Ge-Si system, both the Al-Ge and Al-Si binary alloys have simple eutectic phase diagrams, while the binary Si-Ge system has
continuous solid solubility. These are seen as the vertical faces of the three-dimensional ternary phase diagram in Fig. 6.7 given by Song and Hellawell [50]; the vertical axis is temperature.

![Figure 6.7: Ternary Phase Diagram of Al-Si-Ge system after Song and Hellawell [50]. (Compositions are in weight %.)](image)

The system has a monovariant eutectic valley which extends from the Al-Si to the Al-Ge binary eutectic points, at 578 and 424 °C, respectively. Any vertical section extending from the pure Al corner of the 3-d diagram to a given Si$_x$Ge$_{1-x}$ composition $x$ on the SiGe axis would be a simple pseudo-binary diagram, similar to Al-Ge except that the Si$_x$Ge$_{1-x}$ has a range instead of a unique melting temperature. The two-phase L+Si and L+Ge regions of the binary diagrams correspond to a L+Si$_x$Ge$_{1-x}$ region for alloy compositions other than $x = 0$ or 1. A view of the liquidus surface looking down on the
diagram, known as a liquidus projection, is shown in Fig. 6.8. The region labeled (Ge, Si) is the liquidus surface above the L+Si$_x$Ge$_{1-x}$ region. The composition of the ternary alloy corresponding to any point such as X within the triangle of Fig. 6.8, can be read using the axes along the edges. The atomic fraction of Ge is the ratio of the value AC in % from the Al-Si axis, to the value AB, in % along the Ge-Si axis, or 30%.

Figure 6.8: Liquidus projection of Al-Si-Ge system after P. Villars, et al. [51] Compositions are in atomic %. For composition X, the liquidus temperature at which the alloy would begin to solidify is given on the isotherm as 1190 °C. However, the composition x of the Si$_x$Ge$_{1-x}$, which would first form from this alloy cannot be determined from either diagram without additional information. On binary diagrams, the compositions of the phases (e.g. L and
Ge) in a two-phase region can be found at the ends of a horizontal tie-line. Within a two-phase volume region like L + Si$_x$Ge$_{1-x}$, tie-lines exist [52], but their endpoints must be determined experimentally, which has not been done. The Si:Ge ratio is constant along any straight line from the Al corner to the Si-Ge axis. Like a binary system, during equilibrium cooling the liquid composition moves along the liquidus towards the eutectic temperature. In the ternary diagram, without knowing x for the Si$_x$Ge$_{1-x}$ being formed we cannot determine the change in the liquid composition. However, it must move down the liquidus surface until it reaches the eutectic valley line. Song and Hellawell measured the compositions of Si$_x$Ge$_{1-x}$ formed during the eutectic reaction for four compositions along the eutectic valley. The Si:Ge ratio of the Si$_x$Ge$_{1-x}$ being formed is greater than that of the liquid, and the Si content of the Al phase is nearly zero; this causes the liquid composition to move along the eutectic valley line towards its lowest temperature of 424 °C on the Al-Ge axis. This is consistent with other ternary alloys; the liquid composition moves down the liquidus to the eutectic valley and then down the valley. It is important to note that, based on the work of Song and Hellawell [50], the epitaxially-regrown Si$_x$Ge$_{1-x}$ is expected to increase in Ge content as it grows, with the most Si-rich composition forming first. A graded Si:Ge ratio is thus expected, and might be observed using Energy Dispersive X-ray Spectroscopy (EDXS) linescans and Z-contrast Scanning Transmission Electron Microscopy (STEM) imaging in the TEM.

Assuming equilibrium concentrations given by the ternary phase diagram, we can apply the liquidus projection in Fig. 6.8 to determine the liquid composition that should
form upon heating a Si wafer with known Al and Ge layer thicknesses to a given
temperature, and this can be used to calculate the thickness of Si which would be
dissolved.

The thicknesses of Al and Ge in the deposited layers determine the Al:Ge atom ratio.
For a given Al:Ge atom ratio, the total alloy composition lies on a straight line from the
Si corner to the Al-Ge axis in Fig. 6.8. If heated to a given temperature, the equilibrium
liquid composition lies on the intersection of this straight line with the isotherm for that
temperature. This composition point then tells the Si fraction in the liquid, from which
the Si thickness dissolved by the Al/Ge layer stack to reach equilibrium at the chosen
temperature can be calculated. The volume ratio of the Al/Ge layer stack is the same as
the thickness ratio since the area is the same for both, and the mass per unit area of each
film is the product of its thickness and density. The mass ratio of Al:Ge in the deposit is
then easily converted to an atomic ratio using their atomic weights, Table 6.1. This ratio
can then be used to construct a straight line on the liquidus projection, whose intersection
with the isotherm for a given annealing temperature gives the Si atom fraction in the
liquid, from which we can find the amount of Si dissolved in the melt. The deposit of Ge
is expected to be amorphous using an electron-beam evaporator [53].
TABLE 6.1:
DENSITY AND ATOMIC WEIGHT OF Al, Si, AND Ge

<table>
<thead>
<tr>
<th></th>
<th>Density (g/cm³)</th>
<th>Atomic Weight (g/mole)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>2.70</td>
<td>26.98</td>
</tr>
<tr>
<td>Si</td>
<td>2.33</td>
<td>28.09</td>
</tr>
<tr>
<td>Ge</td>
<td>3.90</td>
<td>72.60</td>
</tr>
</tbody>
</table>

Suppose we deposit layers of Al and Ge whose thickness correspond to Al/Ge weight ratio of 47/53, the same as the binary Al-Ge eutectic composition. The ternary liquid composition will lie on the straight line from the Si corner to the Al-Ge eutectic point, as shown in Fig. 6.8. Since the mass ratio of Al/Ge, $w_{Al}/w_{Ge}$, is 47/53, the atomic ratio of Al/Ge, $A_{Al}/A_{Ge}$, is $w_{Al}m_{Ge}/w_{Ge}m_{Al}$, where $m_{Ge}$ and $m_{Al}$ are atomic weight of Ge and Al, respectively. Therefore, $A_{Al}/A_{Ge}$ is 70.5/29.5. At each temperature, the atomic percentage of each element can be read from the liquidus projection of Al-Si-Ge system, and it can be easily converted to weight percentage using atomic weight of each element. The resulting weight percentages of Al, Si, and Ge in the liquid formed by melting the deposited layers of Al and Ge are shown in Fig. 6.9. The higher the anneal temperature, the thicker will be the Si layer consumed, since the Si content of the liquid increases as shown in Fig. 6.9.
Figure 6.9: The weight percentage of Al, Si, and Ge that melt vs. peak anneal temperature for an Al/Ge ratio equal to that of the binary Al-Ge eutectic.

The thickness ratio of Si/AlGe for 3 different Al/Ge ratios is plotted vs. peak temperature in Fig. 6.10. The Al:Ge ratio is fixed by the deposition layer thicknesses. For example, an Al:Ge thickness ratio of 1.75 achieves a composition of Al$_{0.47}$Ge$_{0.53}$ (wt %) using the formula

$$t_{Al}/t_{Ge} = \frac{xp_{Ge}}{(1-x) \cdot \rho_{Al}}.$$  \hspace{1cm} (6-2)

At each temperature, the ratio of deposited Al thickness $t_{Al}$ to the thickness $t_{Si}$ of Si dissolved by the liquid is $t_{Al}/t_{Si} = w_{Al} \rho_{Si} / w_{Si} \rho_{Al}$, where $w_{Al}$ and $w_{Si}$ are the weight percentages of Al and Si in the liquid at each temperature, respectively. Therefore, the thickness ratio of Si/AlGe at each temperature can be calculated. For each Al/Ge ratio, the ratio of the thickness of Si dissolved into the melt is calculated as a function of peak
anneal temperature to enable selection of the tunnel junction depth, as shown in Fig. 6.10.

Figure 6.10: The thickness ratio of Si/AlGe for three different Al/Ge thickness ratios vs. peak anneal temperature.

The grown Si:Ge composition ratio can similarly be computed from the phase diagram as a function of the starting Al/Ge atomic ratio in the deposited layer. This is plotted in Fig. 6.11 to facilitate design of experiments.
6.2.2 Rapid Melt Growth of Ge Tunnel Junctions

In prior work at Notre Dame, a single layer of Al was deposited on $n^+$ Ge [49] [54]. There are good reasons why it should yield better results to first deposit a pure undoped Ge layer on the $n^+$ Ge substrate, and then an Al layer. When only Al is deposited, the melt dissolves some $n^+$ Ge, and must therefore contain a high phosphorus (P) concentration as well as Al. During epitaxial regrowth, if the P partitions entirely into the Ge, it will offset the Al acceptor doping (by compensation doping). In addition, the melt dissolves the most heavily doped $n^+$ Ge, since the donor diffusion profile has maximum concentration at the surface. This must reduce the $n^+$ doping level at the final junction, to a degree that depends on the donor diffusion profile.
An experiment of depositing different thickness of undoped Ge layer with the same Al thickness was therefore done on an \( n^+ \) doped Ge wafer, and rapid-melt processed to grow a \( p^+ \) layer. The Ge tunnel junction formation process is similar to the Si tunnel junction formation process described in section 6.1, based on the Al-Ge binary phase diagram. Calculation shows that 100 nm Al and 154 nm amorphous Ge, has the same overall composition as the liquidus line of the phase diagram predicts for the peak anneal temperature of 600 °C, which is the theoretical thickness ratio that would not require any dissolution of the Ge substrate. If the layers melt to form liquid of this composition, it should form an epilayer as it cools through the L+Ge region. From the lever rule, the expected epilayer thickness can be calculated. The regrown Ge would then contain no \( n^- \) type dopant, and the resultant \( p^+ \) doping due to Al would be higher, improving the TD \( I-V \) characteristics. In this experiment, the control wafer has only Al deposited. Germanium layers of 50, 100, and 150 nm were grown on the other three pieces before the Al layer. The Al thickness was 100 nm in each of these cases, and the anneal temperature was 600 °C. All wafers were capped with a 50 nm thick silicon nitride layer formed by PECVD. The \( I-V \) characteristics are shown in Fig. 6.12. A tunnel diode was formed by growing 100 nm Al on \( n^+ \) Ge with a peak current density of 2.2 \( \mu \)A/\( \mu \)m\(^2\). Backward diodes were formed by growing 50 and 100 nm undoped Ge layer as well as 100 nm Al on \( n^+ \) Ge. This indicates that the undoped amorphous Ge was successfully transformed into heavily doped crystalline Ge. The wafer with the 150/100 nm Ge/Al ratio had a normal diode characteristic with much lower current than the others. This could be due to a thin amorphous layer make it a pin diode, and we would expect that to give the observed \( I-V \)
Figure 6.12: Current-voltage characteristics of Al doped $p^+$ Ge on $n^+$ Ge with different Al/Ge deposition stacks.

The optical image of Y264a with 100 nm Al on Ge after annealed at 600 °C is shown is Fig. 6.13. The grey areas have internal structure similar to a typical eutectic mixture, but only cover a fraction of the area. Al might segregate to these areas, leaving nearby areas devoid of metal.
Figure 6.13: Optical image of Y264a with 100 nm Al on Ge after annealed at 600 °C.

STEM cross section images of the eutectic mixture, shown in Fig. 6.14, further suggest that the Al tends to segregate to certain areas while other areas don’t have Al. Figure 6.14 shows two areas that had Al on Ge. Figure 6.14(a) is such an area where the Al pooled together and that is why it seems so thick and curved at the bottom compared to the area showed in Fig. 6.14(b) where Al is much more uniform. The dark and light areas in the metal cross section are the Ge-rich phase and Al-rich phase respectively.
Figure 6.14: STEM images of Y264a with 100 nm Al on Ge after annealed at 600 °C. (a) and (b) are different areas. (Courtesy Tom Kosel, Notre Dame).

Figure 6.15 shows a zoomed in STEM image and x-ray maps. Figure 6.15(a) is the STEM image. The pink area in Fig. 6.15(b) is x-ray map which shows only the Al in the structure. The green area in Fig. 6.15(c) is x-ray map which shows only the Ge in the structure. The green area in Fig. 6.15(c) confirms that the dark areas in the eutectic mixture are the Ge phase (with Al in it).
Figure 6.15: STEM image (a) and x-ray maps of Al (b) and Ge (c). (Courtesy Tom Kosel, Notre Dame).

The TEM image in Fig. 6.16 shows the regrown Ge epilayer between the Ge substrate and the Al-Ge eutectic mixture, in which light and dark areas are Al-rich and Ge-rich phases. Figure 6.17 shows higher magnification images of the epilayer of Fig. 6.16. From Fig. 6.17(a) it can be seen that the thickness of the regrown layer is around 60 nm. In this case, since there is no amorphous Ge deposited, the density of crystalline Ge (5.33 g/mL) is used in the calculation. A hundred nm Al and 110 nm crystalline Ge has the same overall composition as the liquidus line of the phase diagram predicts for the peak anneal temperature of 600 °C. From the lever rule, the expected epilayer thickness calculated is 60 nm, which is the same as the thickness of the uniform area showed in the TEM. The high-resolution lattice image in Figure 6.17(b) shows the crystalline nature of the regrown layer. The regrown layer is clearly epitaxial, as expected, and is free of defects such as dislocations or stacking faults.
In this chapter, vertical tunnel junction processes using rapid thermal diffusion from doped metal sources have been developed. Tunnel diode was formed using an Al:B:Si source on Si with a peak current density of 2.7 $\mu$A/$\mu$m$^2$. Rapid melt growth of Ge tunnel junctions were developed by depositing different thickness of undoped Ge layer with the same Al thickness on an $n^+$ doped Ge wafer, and rapid-melt processed to grow a $p^+$ layer. Backward diodes were formed by growing 50 and 100 nm undoped Ge layer on $n^+$ Ge. This indicates that the undoped amorphous Ge was successfully transformed into heavily doped crystalline Ge. TEM was taken which allow characterization of the regrown layer.
thickness. TEM also showed that the regrown layer is clearly epitaxial and free of defects.
CHAPTER 7:  
CONCLUSIONS AND RECOMMENDATIONS

Silicon tunnel diodes were demonstrated using spin-on diffusants in a four-mask oxide window process on high resistivity substrates. A peak current density of 2.7 $\mu$A/$\mu$m$^2$ and peak to valley current ratio of 2.25 has been achieved which is the best result ever achieved using spin-on diffusants on Si. Tunnel diodes formed on high resistivity substrates allow S-parameter measurements and extraction of the bias dependence of the junction capacitance and conductance. Experiments have been developed to determine a suitable anneal ambient and etch time in proximity rapid thermal diffusion. It has been observed in this work that for Borofilm 100, oxygen is needed in the diffusion ambient to allow subsequent removal of the residue. It was observed that the residue of Phosphorosilicafilm diffused in pure N$_2$ and Borofilm 100 diffused in 97% N$_2$ : 3% O$_2$ were removed in 10 % commercial buffered HF. The microwave frequency S-parameters and low frequency impedance measurements were done on the tunnel diodes. Comparison of the differential conductance of the tunnel diode extracted from the impedance measurement with the derivative of the DC measurement showed good agreement. The device model is extracted from dc, microwave S-parameter, and RF impedance measurements. The tunnel diode characteristics are well described by the Schulman-Broekaert model. Post-metallization Al contact anneals were explored to see
the effect of contact anneals on current density and PVR. It was found that both the peak current density and PVR of tunnel diodes improved after rapid thermal annealing in forming gas. A tunnel diodes oscillator was demonstrated with a characteristic frequency of 190 kHz. The limitation of current density achieved in this technique was analyzed and it was shown that active P concentration was lower than the solid solubility at the same temperature.

A joint experiment with Vortek Industries Ltd using flash anneals of SOD $p^+n^+$ junctions were explored. It is inferred that the flash anneal increased the P doping density, however, the $I-V$ show that the resulting activation is not enough to make the surface degenerate, as an NDR was not achieved. Multiple flash anneals were further explored to improve the P doping density. It was shown that the current increased after 2 flash anneals, but degraded after 3 and 4 flash anneals.

Vertical tunnel junction processes using rapid thermal diffusion from doped metal sources have been developed. Tunnel diode was formed using doped metal source on Si with a peak current density of 2.7 $\mu$A/$\mu$m$^2$. Rapid-melt-growth of Ge tunnel junctions were developed by depositing different thickness of undoped Ge layer with the same Al thickness on an $n^+$ doped Ge wafer. Backward diodes were formed by growing 50 and 100 nm undoped Ge layer on an $n^+$ Ge. This indicates that the undoped amorphous Ge was successfully transformed into heavily doped crystalline Ge. TEM was taken which allow characterization of the regrown layer thickness. TEM showed that the regrown
layer is clearly epitaxial and free of defects.

For tunnel diodes formation using doped metal source on Ge, the right thickness of the deposited Ge layer that gives the best current density needs to be determined experimentally. Three thicknesses have been tried in this work and two produced backward diodes. The translated-stencil-mask deposition provides an efficient way to help the Al/Ge on Ge study and create abrupt \( p^+/n^+ \) junctions [55, 56], therefore obtaining high current density tunnel diodes. This system uses piezoelectric deflection to translate a stencil mask; different sources (Al, Ge) can be electron-beam evaporated for different times to define an array of different thicknesses ratio at different locations on the same wafer. These can then be subjected to the same rapid melt growth processing allowing for a more rapid combinatorial analysis of melt compositions on the same wafer. A wide range of layer thicknesses can thus be fabricated in a single pump down cycle of an electron-beam evaporator, greatly increasing the ability to examine the effects of layer thickness ratios on the junction properties.
APPENDIX A:

PROCESS FLOW AND TEST STRUCTURES FOR TUNNEL DIODE MASK SET

NEO 2004

This appendix describes a mask set designed in this work. The full process using benzocyclobutene (BCB) was not developed, but it is described here to facilitate future research. The five-layer mask set, labeled NEO 2004, where NEO stands for nanoelectronic oscillator, was designed and laid out for use on a GCA 6300 stepper. The masks were designed using Mentor Graphics IC Station. Device size varies from 2 x 2 to 8 x 20 μm². An overview of the process is given here and repeats part of chapter 3 to provide a stand-alone description.

Starting with an RCA-cleaned high resistivity, 1000-5000 Ω - cm, 100 mm, (100) Si wafer, a layer of thermal oxide is grown as a diffusion mask, Fig. A1(a). Then diffusion windows are opened using the Isolation mask (first mask), Fig. A1(b), followed by B proximity RTP, Fig. A1(c). The wafer then is dipped into buffered HF (BHF) to remove the SOD residue, Fig. A2(a); this step thins the thermal oxide. A second layer of oxide is deposited on the wafer by plasma-enhanced chemical-vapor-deposition (PECVD) at a temperature of 250 °C, Fig. A2(b). Diffusion windows are opened using the Emitter mask (Second mask), Fig. A2(c), followed by phosphorus proximity RTP, Fig. A2(d).
Figure A1: Scale drawing, in the vertical dimension only, of the tunnel diode process: (a) grow field oxide, (b) etch oxide, and (c) diffuse B by boron proximity rapid thermal processing.
Figure A2: Vertical tunnel diode process: (a) etch to remove spin-on diffusants residue, (b) deposit SiO2 by plasma-enhanced chemical vapor deposition(CVD), (c) etch oxide, and (d) diffuse P by proximity rapid thermal processing.
Next, the wafer is dipped into BHF to remove the SOD residue and clear the CVD oxide, Fig. A3(a). Then a layer of Al is deposited onto the wafer and is patterned by wet chemical etching in Cyantec’s Al-12 etchant (HNO₃, HPO₃) using the Metal mask (third mask), Fig. A3(b) and (c). After spin coating and curing of BCB, Fig. A4(a), vias are formed using the Via mask (fourth mask), Fig. A4(b).

![Diagram](image)

**Figure A3**: Vertical tunnel diode process: (a) etch to remove spin-on-diffusant residue, (b) evaporation Al, and (c) etch Al.
Finally, a layer of Al is deposited onto the wafer, and wet chemical etching is used to define the contact using the Bond-Pad mask (fifth and final mask), Fig. A5(a) and (b).
Figure A5. Vertical tunnel diode process: (a) deposit Al, and (b) etch to define final contact areas.
Table A1 shows the tunnel diodes design sizes including the expected series resistance and shift in the peak voltage of the diode, assuming a B sheet resistance of 312 Ω/□. The device ohmic contact has a length \( l \) and a width \( w \), shown in the first two columns of Table 1. Devices were designed for alignment accuracies, \( a \), (column 3) of 0.5, 1, and 2 μm. The distance between features belonging to two consecutive layers is set to be twice the alignment accuracy (column 4). The via contact dimensions (columns 5 and 6) and emitter size, tunnel junction dimensions, (columns 7 and 8) of each device are also shown. By counting the number of squares between the emitter and the collector, the series resistance (column 11) is computed by dividing the sheet resistance (312 Ω/□) by the number of squares (column 9). Current calculated for two current densities, 1 μA/μm² and 0.1 mA/μm², are shown in column 12 and 13, respectively. Estimate of the voltage shift at a peak current density of 0.1 mA/μm² is shown in column 14. The collector metal length and width of each device are shown in the last two columns. Two, four, and five fingers devices are included in the last three rows of the table with number of fingers designed for devices with the same area, 100 μm², to compare differences in peak voltage, given in column 9.
TABLE A1:
TUNNEL DIODES ON MASK SET NEO 2004 \( (R_S = 312 \Omega/\square) \).
Figure A6. Schematic layouts of vertical tunnel diode and test structure of mask set, NEO 2004. The chip size is 3.1 x 3.1 mm.

The smallest vertical tunnel diode labeled is 2x2pn0.5. In this label, 2x2 stands for the size in square microns of the metal contact to the second diffusion, which is also the tunnel junction area. The ‘pn’ indicates a tunnel diode, and 0.5 stands for the alignment accuracy in microns. Figure A7 shows the layout of the vertical tunnel diode in plan view.
corresponding to the cross section of the diode shown in the lower part of the figure. For
the plan view of this device, the squares counting from the center are via (1 x 1 μm²),
metal (2 x 2 μm²), and emitter (3 x 3 μm²) corresponding to the n+ doping. Outside these
squares is a square ring composed of metal on top of p+ doping. The two small
rectangles inside this metal are the vias. The outermost square (10 x 10 μm²) is the
collector, which corresponds to the area of the p+ well.

The DC pads and microwave bondpad arrangements are shown in Fig. A8(a) and (b)
respectively. The microwave pads are 50 Ω, in a ground-signal-ground configuration with
a 100 μm pitch. The pad size in Fig. A8(a) is 100 x 100 μm² and the signal pad width in
Fig. A8(b) is 65 μm, the gap width between signal and ground pads is 40 μm. Open-
circuit and short-circuit test structures are also provided on the mask set for calibration
purposes.
Figure A7: The layout of the vertical tunnel diode corresponding to the cross section of tunnel diode 2x2pn0.5.
Figure A8. Measurement pad structures for (a) DC current-voltage measurements and (b) microwave S-parameter measurements. The pad size in (a) is 100 x 100 μm² and the signal pad width in (b) is 65 μm, the gap width between signal and ground pads is 40 μm.
Test structures have been designed to test the electric properties of the devices and also to calibrate and quantify process attributes. The GCA 6300 stepper is capable of alignment accuracy of 0.5 μm [57]. Two-dimensional verniers were designed to measure the alignment accuracy, Fig. A9. The verniers have been designed so as to determine the misalignment with a resolution of 0.2 μm. The number notation shown in the figure, e.g., “1-2”, measures the misalignment between layers 1 and 2.

Figure A9: Layouts of test structures on the NEO 2004 vertical tunnel diode mask set.
Figure A10. Via test structures on the NEO 2004 vertical tunnel diode mask set. The two pads on both ends have the size of 60 x 120 μm² (130 is the number of vias, 2 x 2 is the via size in square microns).

This mask set also provides interconnect and process test structures. Via test structures are designed to measure the resistance of 1 x 1 and 2 x 2 μm² vias. A 2 x 2 μm² via test structure is shown in Fig. A10. The two pads on both ends have the size of 60 x 120 μm², connecting 130 vias in series. In the label shown in the figure, 2 x 2 stands for the via size in square microns.

Figure A11(a) shows structures for area dependent device measurements. The number on the top is the misalignment tolerance that the test structure can tolerate and still yield a testable structure; the numbers on the left indicates the dimension of the
square contacts inside the rectangular well corresponding to the second diffusion. The outermost rectangle corresponds to the $p^+$ diffusion onto which a large single metal contact is formed. Transmission line method (TLM) structures are used to measure the contact resistance, sheet resistance, and therefore to estimate the doping concentration, Fig. A11(b). The number on the top is the dimension of the square contact string. The number on the left is the dimension of the gap between the squares. In Fig. A11(b) 40 is the side length of the squares in microns.

![Schematic layouts of test structures on the NEO 2004 vertical tunnel diode mask set](image)

(a)           (b)

Figure A11. Schematic layouts of test structures on the NEO 2004 vertical tunnel diode mask set: (a) area dependent measurement structure, (b) transmission line method structure.
Figure A12. Layouts of test structures on the NEO 2004 vertical tunnel diode mask set: (a) interconnect resistivity measurement structure, (b) SEM test structure.

Interconnect resistivity measurement structure allows us to measure the sheet resistance of the metal layer by dividing the resistance by the number of squares between the middle two pads which are used to measure the voltage, Figure A12(a). The pads on both ends have a size of 75 x 75 μm². The line width is 4 μm. The number of squares
between the middle two pads is 68. Scanning electron microscopy (SEM) test structure are provided, Fig. A12(b), to inspect the etching anisotropy, and alignment of each step. On the right side, the smallest feature size of each layer is used and the size is marked. For cleave convenience, the length of each feature is 300 $\mu$m. Each layer overlaps so that the alignment can be inspected under SEM.
APPENDIX B:
DC AND RF CHARACTERIZATION OF TUNNEL DIODE USING RAPID THERMAL DIFFUSION FORM SPIN-ON DIFFUSANTS

This appendix describes results from collaboration with Qingmin Liu (Notre Dame). Qingmin Liu performed these measurements on devices I fabricated. These results were published in 62nd Device Research Conference Digest, page 27-28, 2004. As can be seen in Fig. A13, the measured current-voltage characteristic for the Si tunnel diode is in good agreement with the Schulman-Broekaert analytic model expression for $I_{TD}(V)$. Extracted parameters are listed in Table A2 for the fit of Fig. A13.

In order to characterize the device RF performance, the microwave S-parameters of these diodes were measured from 45 MHz to 30 GHz, using an Agilent 8510XF vector network analyzer with a port power of -33 dBm (which is the lowest power can be used for 8510). A two-port LRM (line-reflect-match) calibration was performed using a Cascade Microtech 104-783 impedance standard substrate. The measured S-parameters were de-embedded from the probe pads using a $\pi$ - equivalent circuit model. Figure A14 shows the tunnel diode equivalent circuit, in which $R_S$ is the device series resistance, $C_D$ is the junction capacitance, and $I_{TD}(V)$ represents the tunnel diode current-voltage characteristic.
Figure A13. Measured current-voltage characteristics for the Si tunnel diode fit the Schulman-Broekaert model.

Figure A14. Tunnel diode equivalent circuit. $R_S$ is the device series resistance, $C_D$ is the junction capacitance, and $I_{TD}(V)$ represents the tunnel diode current-voltage characteristic.
Figure A15 shows the microwave test pad characterization on the high resistivity Si substrate. An open-circuited and a short-circuited test structure were measured to extract the pad parasitics. Figure A16 shows the measured S-parameter $S_{11}$ of the tunnel diode after calibration and simulated $S_{11}$ based on our equivalent circuit at zero bias. For clarity, only 5% of the 801 data of points are shown in the figure. An excellent agreement between the equivalent circuit model fit and measurement is obtained. Table A2 shows our tunnel diode SPICE model parameters derived from dc current-voltage measurements and S-parameter measurements in the range of 45 MHz to 30 GHz.

\[
\begin{array}{cccc}
C_{P1} & C_{P2} & R_P & L_P \\
1.65 \text{ fF} & 11.7 \text{ fF} & 1.73 \Omega & 26.3 \text{ pH} \\
\end{array}
\]

Figure A15: Microwave test pad characterization.
Figure A16: Comparison of measured $S_{11}$ of the tunnel diode after calibration (circles) and simulated (line) $S_{11}$ shows excellent agreement.

### TABLE A2:

SCHULMAN-BROEKAERT MODEL PARAMETERS DERIVED FROM DC CURRENT-VOLTAGE MEASUREMENTS AND S-PARAMETER MEASUREMENTS IN THE RANGE 45 MHZ TO 30 GHZ

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Resonance 1 (primary)</th>
<th>Resonance 2 (excess)</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$J_p$</td>
<td>0.0149</td>
<td>0.0473</td>
<td>Peak current density</td>
<td>mA/μm²</td>
</tr>
<tr>
<td>$V_N$</td>
<td>0.176</td>
<td>1.55</td>
<td>Voltage of maximum NDR</td>
<td>V</td>
</tr>
<tr>
<td>$V_T$</td>
<td>-0.307</td>
<td>0.654</td>
<td>Resonance turn-on voltage</td>
<td>V</td>
</tr>
<tr>
<td>$\Gamma$</td>
<td>0.155</td>
<td>0.000017</td>
<td>Full-width at resonance half max</td>
<td>V</td>
</tr>
<tr>
<td>$n$</td>
<td>9.23</td>
<td>2.19</td>
<td>Resonance subthreshold ideality factor</td>
<td></td>
</tr>
<tr>
<td>$J_V$</td>
<td>0.000026</td>
<td></td>
<td>Thermionic leakage current at $V_V$</td>
<td>mA/μm²</td>
</tr>
<tr>
<td>$n_V$</td>
<td>4.98</td>
<td></td>
<td>Thermionic leakage current ideality</td>
<td></td>
</tr>
<tr>
<td>$V_V$</td>
<td>0.501</td>
<td></td>
<td>Valley voltage</td>
<td>V</td>
</tr>
<tr>
<td>$C_D$</td>
<td>12.6</td>
<td></td>
<td>Junction capacitance</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>$R_S$</td>
<td>54.7</td>
<td></td>
<td>Device series resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>$kT$</td>
<td>0.0259</td>
<td></td>
<td>Thermal voltage</td>
<td>V</td>
</tr>
<tr>
<td>$A$</td>
<td>64</td>
<td></td>
<td>Area</td>
<td>μm²</td>
</tr>
</tbody>
</table>
APPENDIX C:
HIGH SPEED TUNNEL DIODE / TRANSMISSION LINE PULSE GENERATOR
CIRCUIT DIAGRAM AND TEST STRUCTURES

The circuit diagram [58] for a 20 GHz pulse generator is shown in Figure A17(a) and its layout is shown in Figure A17(b). Interdigitated capacitor test structures and calibration structures, open and short, are shown in Figure A18. The line width is 65 μm, the gap between signal and ground pads is 40 μm. These dimensions correspond to a characteristic impedance of 50 Ω for the coplanar transmission line. The gap between the metal plates of the interdigital capacitor is 5 μm. Other circuits with different frequencies have the same layout except with different transmission line lengths.

Figure A17: Tunnel diode/transmission line pulse generator: (a) simplified circuit diagram (b) layout of circuit with frequency of 20 GHz.
Figure A18. Interdigitated capacitor test structure and calibration structures of (a) 30 femto-farads, (b) open, and (c) short.

The tunnel diode transmission line pulse generator circuit consists of a pair of tunnel diodes, a pair of capacitors, and a pair of quarter-wavelength transmission lines terminated in a short. Both diodes are biased pre-peak. The clock signal is given for a few cycles to perturb the tunnel diode from its prepeak bias voltage to a postpeak voltage. The state change of the diode into a postpeak position generates a voltage step that travels out and back on the transmission line. The wave reflected from the load snaps the diodes back to their prepeak state. The clock is turned off once the oscillation sustains itself. The oscillation frequency, \( f \), is four times the transit time along the transmission line, which is given by

\[
    f = 4 \frac{v_p}{\lambda} = \frac{4}{\lambda \sqrt{\mu \varepsilon}}, \tag{A.1}
\]

where \( \lambda \) is the wavelength, \( v_p \) is the velocity of light and being determined by the
dielectric constant and permittivity, $\mu$ is the permeability of the media, and $\varepsilon$ is the permittivity of the media.
APPENDIX D:

VERTICAL SILICON TUNNEL DIODE ON HIGH RESISTIVITY SILICON

The following article is the reprint from 62nd Device Research Conference Digest, pp. 27-28, 2004.
Vertical Tunnel Diodes on High Resistivity Silicon

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Silicon tunnel diodes operating at below 1 GHz have applications in micropower circuits for radio frequency identification (RFID), sensors and sensor networks, and low power RF communications. Here we demonstrate for the first time, vertical tunnel diodes formed by rapid thermal diffusion using spin-on diffusants [1,2] on high resistivity (100) Si substrates, 1000-5000 Ω cm, 100 mm, allowing the extraction of an RF device model. The simple process flow is compatible with techniques found in any commercial front end. The device model is extracted from dc, microwave frequency S-parameter, and RF impedance measurements. The tunnel diode characteristics are well described by the Schulman-Broekaert [3,4] analytic model developed for the resonant tunneling diode and therefore fit readily into SPICE and ADS modeling environments.

The microwave frequency S-parameters of these diodes were measured from 45 MHz to 30 GHz, using an Agilent 8510XF vector network analyzer with a port power of -33 dBm. A two-port LRM (line-reflect-match) calibration was performed using a Cascade Microtech 104-783 Impedance standard substrate. The measured S-parameters were de-embedded from the probe pads using a π-equivalent circuit model. Excellent agreement between the measured S-parameter $S_{11}$ and simulated $S_{11}$ based on the equivalent circuit model at zero bias is shown.

When biased in the negative resistance region of the I-V characteristic, a tunnel diode oscillates. By biasing the tunnel diode at 0.275 V using a 4155 semiconductor parameter analyzer, with a Tektronix oscilloscope attached to the two terminals of the tunnel diode, we observed the oscillation with frequency of approximately 190 kHz. The estimated response frequency, $f = I_p / (2C_0 \Delta V) \approx 450$ MHz, is lowered by the parasitic capacitance of our measurement configuration. The intrinsic speed index of this tunnel diode is estimated to be 0.23 mV/ps is within the speed range of interest for micropower circuits.

We have also taken the RF impedance measurements on these diodes from 0.5 MHz to 100 MHz, using an Agilent 4294A precision impedance analyzer. Differential conductance of the tunnel diode extracted from the impedance measurement and the derivative of the dc current-voltage curve shows good agreement between RF model extraction and dc measurement.

Si$_3$N$_4$

1000 nm - 200 nm

Fig. 1. Schematic cross section of vertical Si tunnel diode formed by rapid thermal diffusion on a high resistivity substrate.

$P$-doped
$n^+ 10^{20} \text{ cm}^{-3}$

$B$-doped
$p^+ 10^{20} \text{ cm}^{-3}$

(100) Si 1-5 kΩ cm

Fig. 2. Comparison of measured current-voltage characteristic and SPICE model fit using the Schulman-Broekaert model.

$J_p = 266 \text{ A/cm}^2$

$PVR = 2.15$

$4 \times 16 \mu \text{m}^2$

Fig. 3. Equivalent circuit model for the Si tunnel diode, where $R_s$ is the series resistance, $C_D$ is the junction capacitance and $I_{TD}(V)$ represents the tunnel diode current-voltage characteristic. $C_1$ and $R_1$ represent the parasitic resistance and capacitance respectively, due to the Si/SiO$_2$ interface under the bonding pads.

Fig. 4. One-port microwave test pad equivalent circuit. An open-circuited and a short-circuited test structure were measured to extract the pad parasitics.

Fig. 5. Comparison of measured (circles) and simulated (line) $S$-parameter shows excellent agreement of the model. The equivalent circuit model, shown in Fig. 3, is used in the simulation. 5% of the 801 measured data of points are shown for clarity.

Fig. 6. Silicon tunnel diode oscillator on-wafer biased at 0.275 V and exhibiting a characteristic frequency of 190 kHz.

Fig. 7. (a) Measured $I$-$V$ characteristics. (b) extracted junction capacitance $C_D$ and $1/C_D^2$. (c) comparison between the extracted conductance (circle) from our model in Fig. 3 and that from the direct derivative of $dI/dV$ (line).
APPENDIX E:

SILICON TUNNEL DIODES FORMED BY PROXIMITY RAPID THERMAL DIFFUSION


I would like to express special gratitude to the co-authors J. Wang, D. Wheeler, S. Howard, and A. Seabaugh.
Silicon Tunnel Diodes Formed by Proximity Rapid Thermal Diffusion

Jinli Wang, Dane Wheeler, Yan Yan, Jialin Zhao, Scott Howard, and Alan Seabaugh

Abstract—We demonstrate the first silicon tunnel diodes (TDs) formed using proximity rapid thermal diffusion and spin-on diffusants. Room temperature peak-to-valley current ratio of 2 is obtained at approximately 100 A/cm² peak current density. Secondary ion mass spectroscopy is used to compare proximity rapid thermal diffusion with rapid thermal diffusion from spin-coated diffusants in direct contact with a device wafer. The proximity rapid thermal diffusion approach provides a cleaner wafer surface for subsequent processing and yields TDs with good local uniformity.

Index Terms—Negative differential resistance (NDR), negative resistance, rapid thermal diffusion, spin-on diffusant, tunnel diode.

I. INTRODUCTION

Tunnel diodes (TDs) with negative differential resistance (NDR) and multivalued current–voltage (I–V) characteristics can add circuit design options to a CMOS process, with the potential for reduction in power dissipation and area [1]. Early Si TD technology suffered from being fundamentally discrete [2]. Recently, molecular beam epitaxy has demonstrated both Si [3], [4] and SiGe [5]–[8] tunnel diodes. The incorporation of TDs with CMOS technology awaits the development of a production-compatible fabrication process. In this letter, we demonstrate for the first time that the Esaki Si TD can be produced using rapid thermal processing tools and spin-on dopant (SOD) sources.

II. DEVICE SIMULATION AND FABRICATION

The vertical p⁺n⁺ tunnel diode device structure and energy band diagram are shown in Fig. 1(a). Phosphorus-doped 1.5-mio cm 100-mm (100) silicon device wafers were cleaned and hydrogen terminated in buffered HF in preparation for rapid thermal diffusion. Source wafers, in this case, n-type, 18–19 cm Si source wafers, were similarly cleaned and spin coated with SOD (Emulsitone phosphorosilicafilm 1×10⁻⁶ and Borofilm 100). To remove the volatile organics in the spin-on film, the source wafers were baked for 20 min at 200 °C in air prior to loading into a Modular Process Technology RTP600 rapid thermal processor. Three cleaned quartz spacers (thickness 0.46–0.48 mm) were placed symmetrically on the source wafer at the wafer edge. The device wafer was placed on top of the quartz spacers, facing the spin-coated source wafer. With this arrangement, on heating, the dopants transport across the short space from the source wafer to the device wafer in a nitrogen (2 slpm flow rate) ambient, a process called proximity rapid thermal diffusion [9]. In the Modular Pro reactor, the tungsten halogen lamps simultaneously illuminate the wafers from both sides. Temperature was measured by a thermocouple in contact with the backside of the source wafer. For diffusion of phosphorus, a heating rate of 30 °C/s was used with an anneal of 900 °C for 1 s. The source wafer was then removed and the device wafer was annealed again at 900 °C for 90 s to lower the phosphorus surface concentration. The wafer was next cleaned in buffered HF. Similarly, for boron rapid thermal diffusion, a single anneal of 900 °C for 1 s using...
Fig. 2. SIMS measurements of boron diffusion into silicon comparing the profile obtained from a source wafer in direct contact with the spin-on diffusant with the profile resulting from proximity diffusion from the source wafer.

30 °C/s heating rate was used. The cooling rate is approximately 30 °C/s for the first 400 °C, after which the cooling takes less than 90 s to return to 200 °C. Buffered HF was used again to remove the residual SODs. Aluminum was applied by electron beam evaporation, then lithography and wet chemical etching in Cyantec Al-12 (HNO₃, HPO₃) was used to define the device contacts. Reactive ion etching in SF₆, 26 sccm, 30 mTorr, 200 W was used to form the device mesa, approximately 700-nm deep, using aluminum as the etch mask.

A process simulation of the phosphorus and boron diffusion profiles using Silvaco’s Suprem3 is shown in Fig. 1(b). We utilized the transient-enhanced diffusion model with the model parameters obtained from curve fitting to secondary ion mass spectroscopy (SIMS) measurements of boron diffusions from Emulsitone’s 5257 diffusion source utilizing ramp rates between 60 °C/s and 75 °C/s. By lowering the ramp rate to 30 °C/s, the transient-enhanced diffusion is significantly suppressed. From Fig. 2, a boron profile with an abruptness of 4 nm/decade at a junction depth of approximately 5 nm is expected. For carrier densities exceeding 10¹⁰ cm⁻³, a zero bias depletion width of approximately 3.5 nm is expected [Fig. 1(a)].

In contrast with rapid thermal diffusion of the spin-on diffusant in direct contact with the wafer, the clean-up process is significantly improved using proximity rapid thermal processing and the doping efficiency is not significantly impeded. Shown in Fig. 2 are SIMS measurements of the concentration profiles obtained from boron diffusion from both source and proximity-diffused wafers from the same anneal were analyzed. Both wafers were cleaned in buffered HF to remove the spin-on diffusant prior to the SIMS analysis. A significant insulating residue with high boron content, approximately 80-nm thick, remains on the source wafer, while in the proximity-diffused wafer, the residue thickness is less than 5 nm.

III. RESULTS AND DISCUSSION

The $I–V$ characteristics for the proximity rapid-thermal-diffused tunnel diodes are shown in Fig. 3. The highest peak current density is 112 A/cm² in Fig. 3(a) and the highest peak-to-valley current ratio (PVR) is 2.11 in Fig. 3(b). We observe a sharp decrease in the peak current after the peak voltage to a plateau region followed by a similar sharp decrease in the current to the valley current minimum. This well-known plateau is an indication of oscillation in the NDR region of the characteristic, which we have confirmed experimentally by dc biasing the tunnel diode at 0.275 V (using probes on a wafer chuck) as shown in Fig. 4. We observe that this 150-µm-diameter TD oscillates at a frequency of 370 kHz. This frequency is consistent with the 20-mA peak current and the capacitance (120 pF) of the probe configuration. The intrinsic oscillation frequency of this device is approximately 100 MHz.

We observe that the peak current scales linearly with area, indicating that no edge leakage effects are present for the device sizes tested [10]. Temperature dependence of the TD’s $I–V$ chart.
characteristics measured from −60 °C to 160 °C [10] shows a monotonic increase in current with temperature. As has been reported previously [11], the temperature dependence of the current beyond the peak voltage is not exponential and may depend on tunneling through defect states in the bandgap.

We observe good local uniformity of adjacent tunnel diodes, as shown in Fig. 5(a). In a 900 × 900 μm² area, a 3 × 3 device array is investigated with ±2% deviation in peak current and ±3% deviation in peak voltage. Two adjacent identical TDs are connected in series and symmetric I–V characteristics are achieved, as shown in Fig. 5(b). The global uniformity is controlled by factors relating to the geometry of the rapid thermal annealing system and in the configuration of the quartz spacers used for proximity diffusion. Thus, larger variations are observed across the wafer, as is apparent in comparing the device characteristics in Fig. 3. Since the speed index is the primary factor governing switching speed, we survey prior best results across fabrication approaches in Table I. The initial results for the proximity diffused tunnel diodes are lower than what has been previously achieved; the limits of this approach are currently under investigation.

IV. CONCLUSION

We demonstrated the first silicon tunnel diodes formed by proximity rapid thermal diffusion from SODs. The ability to form tunnel diodes in a simple process is a first step toward an integrated tunnel diode/CMOS process.

TABLE I

<table>
<thead>
<tr>
<th>First Author</th>
<th>Year</th>
<th>Approach</th>
<th>Type</th>
<th>Current Density (kA/cm²)</th>
<th>Speed Index (mV/pS)</th>
<th>PVR²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Franks [12]</td>
<td>1965</td>
<td>Alloy</td>
<td>SiSiGe</td>
<td>1</td>
<td>1.2</td>
<td>3.8</td>
</tr>
<tr>
<td>Duschi [7]</td>
<td>1999</td>
<td>MBE</td>
<td>SiSiGe</td>
<td>8</td>
<td>4.0*</td>
<td>5.4*</td>
</tr>
<tr>
<td>Rommel [5]</td>
<td>2000</td>
<td>MBE</td>
<td>SiSiGe</td>
<td>10.8</td>
<td>5.4*</td>
<td>1.41</td>
</tr>
<tr>
<td>Dashiel [3]</td>
<td>2000</td>
<td>MBE</td>
<td>Si</td>
<td>47</td>
<td>23.5*</td>
<td>1.3</td>
</tr>
<tr>
<td>Auer [8]</td>
<td>2001</td>
<td>MBE</td>
<td>SiSiGe</td>
<td>0.52</td>
<td>0.45*</td>
<td>2.1</td>
</tr>
<tr>
<td>Dashiel [4]</td>
<td>2002</td>
<td>MBE</td>
<td>Si</td>
<td>16</td>
<td>7.1</td>
<td>-</td>
</tr>
</tbody>
</table>

This work 2002 RTP Si 0.1 0.05* 2.0

* Computed using a tunnel diode capacitance (C) of 20 fF/μm² obtained from simulation of an abrupt tunnel diode with symmetric n and p doping densities of 10²⁷ cm⁻³ using the Poisson solver, BandProf, written by W. R. Frensley.

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REFERENCES

REFERENCES


[38] E. Arai, H. Nakamura, and Y. Terunuma, "Interface reactions of B2O3-Si system


[57] [www.ee.nd.edu/ndnf/processing/gca6300.html](http://www.ee.nd.edu/ndnf/processing/gca6300.html).