PIEZOFLEXURE-ENABLED NANOFABRICATION USING TRANSLATED STENCIL MASKS

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Zoltán Rácz, M.S.

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Alan C. Seabaugh, Director

Graduate Program in Electrical Engineering
Notre Dame, Indiana

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Abstract

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In this study, piezoflexure-enabled nanofabrication (PEN), a new technique for forming nanometer-scale features based on the combination of dynamic stencil lithography and lift-off processing is analyzed, investigated, and demonstrated. In the PEN approach, a deposition substrate is translated under a stencil mask in an electron-beam evaporator between depositions of dissimilar materials. The piezoelectric translation defines the interembedded features that are later differentially etched to reveal the desired patterns. This technique is inherently clean, without resists, organics, and bakes. The masks are reconfigurable, since a single rectangular aperture mask can be used to batch fabricate a wide array of device structures in a single pump-down cycle of the evaporator.

As a first part of this project, the PEN system was designed and constructed. A stencil mask fabrication technique based on anisotropic etching of silicon was developed and square apertures as small as 1 micron on a side with edge uniformity on the order of 10 nanometers were demonstrated.

Several process attributes such as geometrical edge taper, mask clogging, thermal expansion due to radiative heat, and lateral material diffusion during deposition have been identified and characterized. The lateral spread of materials has been investigated in a series of experimental matrices enabled by the ability of the PEN system to perform multiple independent evaporations in the same run. The lateral diffusions were characterized by atomic force and scanning electron microscopy to show that material displacement under the stencil mask can range from approximately 0.1 to 2 μm even near room temperature (45 °C) with strong dependence on the deposited material and the vacuum conditions. It was shown that evaporation in N_2 or O_2 background pressure suppresses the spreading of Al, Cr, Pt, and Ti by slightly more than a factor of two.

In order to explore and develop the capability of this novel technique several structures have been fabricated. Nanometer-scale wires with minimum feature dimension of approximately 30 nm and nanowire pairs with nanometer-scale spacings have been created. Arrays of $Al/Al_xO_y/Ge$ metal-oxide-semiconductor (MOS) structures deposited with varying evaporation conditions have been formed for rapid material characterization. Finally, a poly-Ge channel thin film transistor structure was fabricated.

To C.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Nanoelectromechanical systems (NEMS) are a rapidly evolving area of research driven by interest in new physical phenomena in an experimental regime which is characterized by nanometer-scale dimensions. Nanoelectromechanical devices will enable new applications in electronics, sensing, medical diagnostics, molecular interfacing, displays, metrology, and data storage [1]. NEMS have been demonstrated based on carbon nanotubes [2, 3], metallic [4], or semiconductors [5], however, fabrication of such devices using conventional techniques based on optical or electron-beam lithography, or nanoimprint requires considerable effort.

Three-dimensional structures with nanometer-scale features are particularly challenging. The nanoelectromechanical tunneling transistor (NMTT) shown in Figure 1 is an illustrative example of the challenges associated with the construction of such structures; namely, the fabrication of multi-level three-dimensional structures, lines with varying thicknesses and nanometer-scale separation. The transistor consists of two nanometer-scale metal lines of different thicknesses separated by nanometers, and an overlying metal cantilever. In order to fabricate such a structure using optical or electron-beam

lithography one would need to perform a sequence of deposition, etching, lift-off, and alignment, multiple times.

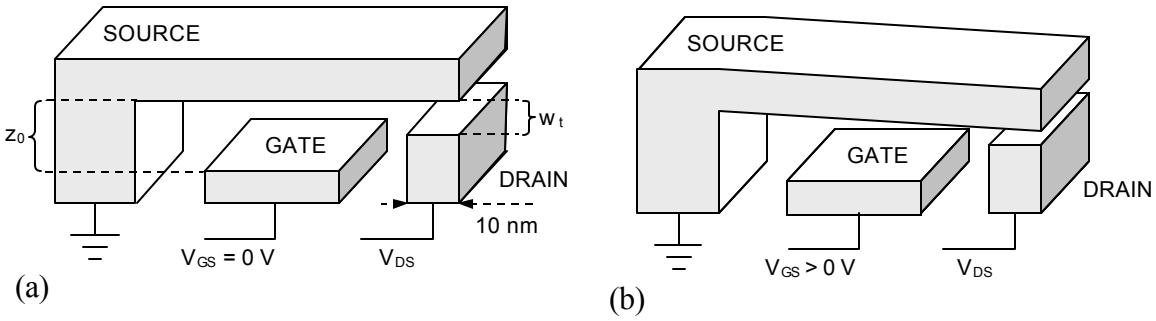

Figure 1. Schematic drawing of a vertical nanoelectromechanical tunneling transistor switch: (a) natural off position and (b) on position under positive gate bias.

In the NMTT, Figure 1(a), the gap between the cantilever source electrode and the drain electrode, w_t, is smaller than the gap between the source and the gate electrode, z_0. When a bias is applied between the gate electrode and the cantilever, V_{GS}, the cantilever is deflected due to electrostatic attraction. With appropriate bias, the cantilever is deflected close enough to the drain electrode to allow tunneling current to flow through the vacuum gap, thus, the device functions as a nanometer-scale switch. A simple model of the electrostatic behavior of an NMTT and performance estimates are given in Appendix 1. By choosing z_0 larger than w_t, the gate current can be made much less than the drain current and the device can function as a field-effect transistor, exhibiting both current gain and voltage gain. Because the electrostatic attraction is polarity independent, the device can operate with bias of either polarity.

In this dissertation a new nanofabrication technique, named *p*iezoflexure-*e*nabled *n*anofabrication (PEN), is explored for fabricating devices of this type. This technique is based on the lateral translation of a substrate underneath a rigid stencil mask between evaporations of different materials. This way interembedded features are created with widths defined by the piezoelectric translation of the substrate, and are subsequently revealed by a lift-off process [7]. With the PEN approach it is conceivable that three-dimensional devices such as the nanoelectromechanical tunneling transistor can be batch fabricated in a single pump-down cycle of an electron-beam evaporator. It also has the promise of enabling the production of wiring structures, connections, and probes with precise dimensional control for molecule characterization and sensing, and nanoscale device measurements.

1.2 Prior art

Stencil mask technology is a millennia old way to create multiple, reproducible patterns on a surface. The concept of stenciling goes back to prehistoric tribesmen who created images on cave walls and rocks by spraying paint around their hands [8]. Probably, the first ones to use stencil masks were natives of the Polynesian Islands who created artistic patterns by pressing vegetable dye through holes cut in banana leaves onto bark cloths [8]. Stenciling was perfected by Japanese and Chinese masters around a thousand years ago [9 – 11] and became an industrial technology in the early 20th century [11]. Stencil mask technology was introduced into the electronics industry in the 1940's in the silk screen printing of printed circuit boards, and later metallic stencils and vacuum deposition techniques were combined to pattern metals on semiconductor devices.

The ability to create mask apertures in a wide variety of shapes and sizes down to sub-10 nm and the availability of techniques to move and align with nanometer precision have made stencil mask technology an important tool in surface science research and nanoscale device fabrication. The modern applications of stencil mask technology for micro- and nanofabrication include selective material growth by deposition through stencil mask apertures [12 – 61], selective material removal by etching directed by stencil apertures [37, 47, 57], selective exposure of areas to ion-beam irradiation to change material properties [62] or for proximity lithography [63], and the creation of structure or material arrays, libraries, for surface science studies [52, 54, 64].

Since photoresist is not needed with stencil masks, high purity, as-grown structures can be formed without contamination by organics or damage by thermal stresses associated with resist application, baking and removal. These are key advantages for characterizing atomic growth processes on high-purity surfaces [58, 59], for patterning or contacting biologically or chemically-functional structures such as molecular circuits [36], carbon nanotubes [36], self-assembled monolayers [26, 46], and microscopic cellular cultures [31], and for device fabrication on substrates that are chemically incompatible with solvent-based lithography, such as poly(vinylidene fluoride-trifluoroethylene) (PVDF-TrFE) copolymer films [24]. Stencil mask technology is also capable of patterning curved, three dimensional, fragile, or mechanically-unstable surfaces such as atomic force microscope tips [16], cantilevers [44], and membranes [13].

Stencil masks need to be mechanically robust and continuous (i.e. isolated shapes such as rings cannot be made); therefore, aperture shapes are typically simple [65]. The position of the stencil mask relative to the substrate can be fixed (static mode [12, 14, 17,

19 – 27, 29-32, 34 – 40, 42 – 53, 55-58, 61-63, 66]) or variable (dynamic mode [12, 13, 15, 16, 18, 21, 29, 34, 47, 60, 64]). Stencil masks can be replaced under vacuum using a mask changing carousel [23] or removed by an air-to-vacuum manipulator [17, 29].

Static stencil techniques are typically used to create simple dot structures, e.g. Cr on Ge [12], Er on Al_2O_3 [14], $BaTiO_3$ on Si(100) [25], Au on octadecanethiol and 1,9-nonanedithiol [26], Pt on Si(001) [34], Au on Si [35], Co and Fe on Cu(100), and $Pb(Zr_{0.2}Ti_{0.8})O_3$ on $SrRuO_3/SrTiO_3$ [42], Au/Cr on Si(100) [44], Au on Si [49], Ni, NiO, and Au on $SrTiO_3$, and Au on $C_{18}SH$ [55]), or lines, e.g. Er on Al_2O_3 [14], Al on SiN [22], Si on Si(100) [38], Co on Cu(100) [39], Au on SiO_2 [41], Pb on GaAs [50], and Pd on Al_2O_3 [51], or gaps, e.g. Au on SiO_2 [41], or rectangles, Au on SiO_2 [30], or crosses, e.g. Au on PVDF-TrFE [24], or pads, e.g. Au on SiO_2 [36]. It should be mentioned that Tixier et al. developed a micron-scale method using suspension bars to construct masks with high pattern-flexibility including patterns with isolated islands [45].

The fabrication of more complex structures is possible by varying the deposition angle relative to the stencil apertures. Using a combination of a stencil mask and double angle evaporation, Cho et al. created a GaAs optical waveguide surrounded by $Al_xGa_{1-x}As$ [17], Ono et al. made a Ni/NiO/Fe junction array [21], Erbe et al. fabricated small area molecular junctions for molecule characterization [46], Masuda et al. reported bimetallic dot array [49], and Dolan demonstrated small area Josephson junctions and multilevel superconducting microbridges [53]. With three deposition sources at different angles, Döhler et al. demonstrated excellent *n*- and *p*-type selective contacts to GaAs *n*-i-*p*-*i* doping superlattices [66]. Another benefit of oblique angle evaporation is the ability to produce features, e.g. lines and gaps, that are significantly reduced in size

compared to the stencil mask pattern [53]. Similarly, Olson et al. developed a technique to deposit ultra-narrow Pd wires with widths less than 15 nm and lengths as long as 800 nm using 30 nm mask openings [51]. If changing the position of the deposition sources is not practical or feasible, multi-angle depositions can still be performed by tilting the mask/substrate arrangement [32, 40].

Dynamic mode techniques add another degree of freedom to stencil lithography by allowing the movement and repositioning of the mask relative to the substrate during or between the depositions. Typical applications include controlled movement of the mask apertures or the substrate during deposition producing directly written structures [12, 13, 15, 16, 18, 29], changing the mask position between consecutive depositions to create overlapping structures [21], to increase pattern density [34], or to perform a sequence of processes with various parameters using a pristine area of the substrate each time without breaking the vacuum [64], and changing the effective aperture size by changing the alignment of a fixed and a mobile mask opening [47]. The general characteristics of the direct pattern writing process using a moving stencil mask have been summarized by Tsang et al. [18].

Translation of the mask or the substrate can be accomplished by piezoelectric actuators [21], a piezoelectric flexure stage [13, 60], using integration with an AFM scanner [15, 16], or by using an integrated microactuator [47], or thermal expansion [12], or simply manually [18, 34]. Piezoelectric flexure stages and AFM scanners have the advantage of nanometer-scale positioning resolution and repeatability, however, they provide a limited range of motion, usually less than a few hundred microns. Egger et al. developed an instrument that extended the lateral range of a flexure stage to 5×5 mm^2

utilizing an inchworm and two inertial sliders [13]. Structures fabricated using a dynamic stencil mask technique include lines of Cu on mica, PdAu/Cr and PdAu/Cu/Cr on Si_3N_4 [13], Er on Al_2O_3 [15], and Cu on Si [47], rings of C_{60} [13] and Cu on Si_3N_4 [15], semicircles of PdAu/Cr on SiO_2 [13], $Al/Al_2O_3/Al$ tunnel junctions [21], and metal-oxide-semiconductor field-effect-transistors (MOSFETs) [64].

Stencil masks are made in a wide variety of ways. The simplest approach is to use an integrated mask that is formed by first growing the mask material on the substrate then creating openings with patterning and etching [29, 32, 33, 37, 38, 41, 47, 48, 50, 51, 53]. Many times a spacer/support layer is deposited before the mask layer to set the desired mask to substrate distance, to increase the mechanical stability of the mask, or to serve as an undercut layer. Typical integrated mask materials and material combinations include SiO_2 and GaAs [29], Mo [51], Si_3N_4/SiO_2 [38], Pt/SiO_2 [33], GaAs/AlGaAs [48], polymethyl-methacrylate (PMMA)/methyl-methacrylate (MMA) [50], photoresist (AZ1350J) [53], negative photoresist (SU-8) [32], and carbon nanotubes in combination with electron beam resist [41]. Integrated masks have the advantage of simple fabrication and accurate control over the separation between the mask and the substrate, however, since the mask is created on the substrate itself and must be subsequently removed, the applications are limited.

For applications that require the translation of the mask or employ substrates that are fragile, three dimensional, or curved, or cannot support the mask defining materials, or require ultra high purity, proximity masks are used. In this case, the pattern is formed separately on a free-standing mask which is then placed above the substrate either in contact [31, 36, 42, 49, 55] or close proximity [12 – 30, 34, 35, 39 – 41, 44 – 48, 52, 54,

62, 64, 66,]. The most commonly used free-standing masks consist of a membrane attached to a supporting frame or a Si wafer with holes.

Membranes can be made of Si [55, 62, 64], silicon nitride [12 – 16, 21, 22, 25, 27, 34, 36, 44, 46], metal foils [23, 29, 47], polyimide [63], or photoresist [24]. The achievable aperture sizes are primarily determined by the resolution of the lithographic technique (optical, electron-beam, or focused ion-beam) and the thickness of the membrane. Stencil masks must be thin to minimize geometrical aberrations due to shadowing. The mechanical robustness of the membrane depends both on the membrane thickness and the density of the aperture pattern. A common approach is to locally thin the membrane at the location of the apertures [21, 22]. Here, pattern density is traded off in favor of mask mechanical stability. To date, the smallest stencil apertures, reported by Deshmukh et al., are hole and line-shaped openings as small as 5 and 16 nm, respectively, made in a 50 nm thick silicon nitride membrane using electron-beam lithography [14]. If apertures smaller than the minimum feature size of available patterning capabilities are needed, aperture size reduction can be achieved by post-patterning layer growth [34, 35].

A silicon wafer can be micromachined to be used as a stencil mask by anisotropic wet etching [18 – 20, 29, 43, 66] or deep reactive-ion etching [45]. These masks are mechanically much more durable due to their thickness (50 – 500 μm), and due to the sloped sidewalls formed by the preferential etching the shadowing effect is reduced significantly. Mask openings with dimensions smaller than 1 μm and showing extremely smooth edges can be fabricated with this technique [20]. Although the mechanical strength of silicon wafers makes it possible to fabricate large area stencil masks, it is

difficult to achieve tight dimensional control over the whole mask because the aperture size depends on the wafer thickness [20].

A wide variety of alternative and unconventional stencil masks have been reported. Wire masks are used because of their simplicity [17, 61], while carbon nanotubes can shadow stripes of only a few nanometers which allows for the fabrication of nanogaps [40, 41, 56]. Porous alumina templates possess the unique combination of high pattern density and small aperture size [49, 57]. A stencil mask made of PDMS seals against the substrate which prevents dilute cell suspensions from spreading beyond the hole areas [31]. If a microscope tip is integrated with the mask [13] or serves as a mask [15, 59], *in situ* imaging and alignment are possible.

As illustrated by these results, stencil lithography has been widely explored. It is a simple, low cost, and rapid micro- and nanopatterning tool of use in a wide variety of applications with the capability to create thin film structures in a resistless process.

In this research, a piezoflexure-enabled nanofabrication method has been explored. Dynamic techniques capable of rapid and flexible nanostructure fabrication have been reported [13 – 16], however, these techniques lack the capability of batch device fabrication on a wafer scale. Employing 100 mm diameter Si stencil masks, PEN enables parallel device fabrication. Another important attribute of PEN over previous works is that the minimum feature dimensions are not limited by one's ability to make sufficiently small stencil apertures because in PEN the feature dimensions are defined by the piezoelectric translation of the substrate between depositions and not by the aperture size. As a result, nanostructures, orders of magnitude smaller than the stencil aperture size, can

be fabricated. This unique feature of PEN enables the creation of nanometer-scale devices and micron-scale contact pads and wiring in the same process.

In this research, the PEN system has been designed and constructed, and the capabilities and limitations of the method have been identified and quantified. A stencil mask fabrication technique has been developed. Nanometer-scale wiring structures have been demonstrated. A primary design consideration has been discovered. On SiO_2 surfaces, there is a large (even exceeding 1 micron for some elements) lateral diffusion of deposited metals under the stencil mask even near room temperature (45 °C). This motion can be retarded by evaporation in oxygen or nitrogen backgrounds. Finally, arrays of structures formed under varying deposition conditions for rapid material characterization have been created, and a thin film transistor structure has been designed and fabricated, formed in a single pump-down cycle of the evaporator.

CHAPTER 2

THE PEN APPROACH

2.1 Process outline

The piezoflexure-enabled nanofabrication technique with the self-aligned feature formation combines the techniques of dynamic stencil mask lithography and sidewall processing. It represents a new tool for simple and rapid fabrication of sub-50-nm features which is particularly useful for the construction of two and three dimensional nanometer-scale structures with nanometer-scale separations. This fabrication method can be used to produce connections and probes to nanoscale devices and single molecules, and enables the development of new nanoelectromechanical systems in a batch production format. The production of thousands of devices in a single process is possible since each opening in the stencil mask produces a device. The translation and deposition control can be automated.

The piezoflexure-enabled nanofabrication approach for achieving nanometer-scale features is outlined in Figure 2.

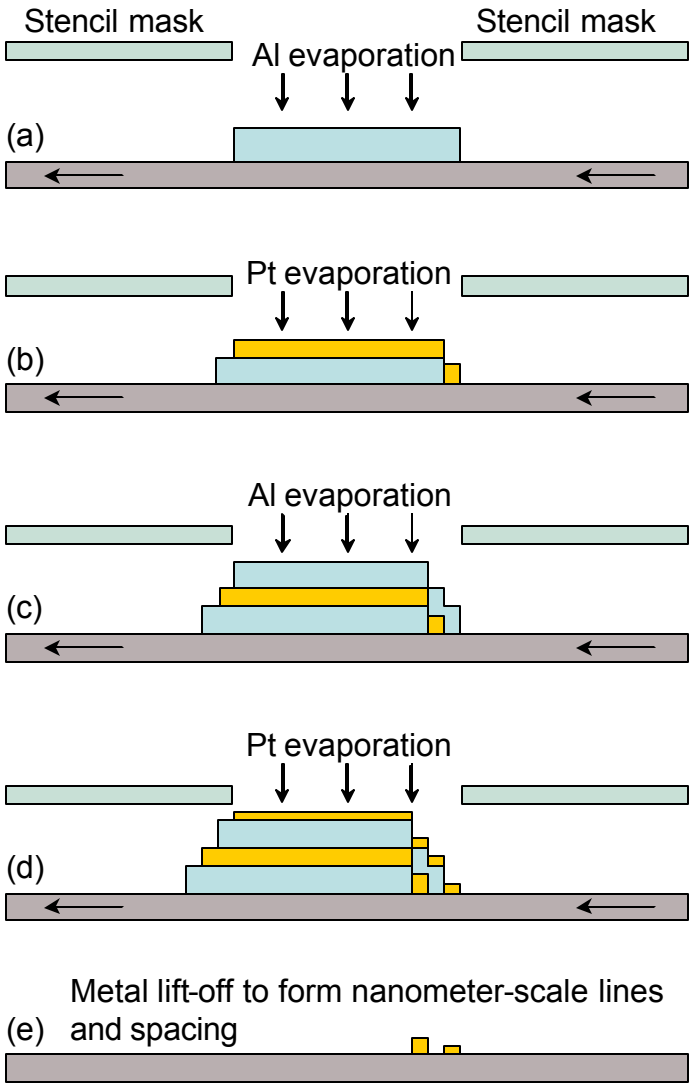

Figure 2. Schematic outline of the piezoflexure-enabled nanofabrication process steps: (a) Al is evaporated through a stencil mask onto a substrate (e.g. SiO_2), (b) the substrate is translated by a piezoflexure stage and Pt is evaporated, (c) and (d) the process is repeated, and (e) differential etching is used to reveal the desired structure.

A stencil mask is positioned above the surface of a substrate on which the structure is to be formed and a sequence of evaporations is performed in a single pump-down cycle of a conventional electron-beam evaporator, Figure 2(a) – (d). In this case, SiO_2 represents a thermally-grown oxide on a Si wafer. Translation of the substrate with

respect to the stencil mask between evaporations is used to create features whose sizes are determined by the areal difference between the two deposits. After each evaporation, the substrate is translated with respect to the mask to produce a set of nanometer-wide, inter-embedded features. Materials for evaporation are chosen based on their etch chemistry and physical properties. The principle is that one metal can be differentially removed with respect to the other by selective etching. In this example, Al is the sacrificial structure for Pt. The Al is removed by etching in AL-12 Al etchant (acetic acid and phosphoric acid mixture) or dilute hydrochloric acid. The aluminum etchant or the hydrochloric acid does not attack the underlying oxide or etch the Pt. After the Al dissolves, the portion of the Pt that was bonded to the Al is unsupported and removed, leaving a pair of Pt nanofeatures with controlled difference in height and precise separation, as shown in Figure 2(e).

This technique does not rely on lithographic processes since features are defined by creating an areal difference between the sacrificial layers and the device layers. The size of the stencil mask opening does not determine the size of the feature; the feature size is controlled by the translation of the substrate under the stencil mask and, using a closed-loop piezoelectric flexure stage, this translation can be 1 nanometer. Moreover, not only is this technique capable of making nanometer-scale features, it is also possible to achieve the same precise control over the separation. By utilizing the whole range of the nanopositioner, many different and spatially separated sets of depositions can be performed to explore multiple device geometries in a single pumping cycle. This allows the creation of device matrices where device properties are systematically varied e.g. in geometry, material, or layer thickness.

One important figure of merit in the creation of structure matrices is the feature density (patterns per unit area) [52] which is limited by the size of the stencil aperture, the range of substrate translation, and the inaccuracy of feature definition as a result of thermal expansion and lateral diffusion. With smaller than 3 μm stencil apertures demonstrated, assuming 2 μm as the necessary separation between features, and using the full range of the piezoflexure stage ($80 \times 80\ \mu m^2$), the PEN system presented in this work enables the production of a 17-by-17 structure array, thus, a maximum of 289 different structures can be formed in a single experiment.

In order to achieve nanometer-scale feature formation by PEN, the stencil mask must have a high degree of perfection since any defects are reproduced in the final device structure. The stencil mask can be either a membrane (e.g. suspended silicon nitride or polyimide) patterned by photo- or electron beam lithography, or an anisotropically-etched hard mask, e.g. potassium hydroxide (KOH) etched Si.

2.2 Materials selection

Materials with dissimilar etch behavior and the desired physical properties are selected for evaporation. Any pair of materials may be used to form nanostructures as long as there is an etchant that is selective to the sacrificial layer, i.e. does not attack either the other layers or the substrate, and the material properties (grain size, continuous layer formation thickness, surface roughness, miscibility, adhesion and mechanical stability) make the formation of the desired feature dimensions possible.

The appropriate material for nanostructures is determined by the intended application of the device. The basic physical properties of materials of particular interest in this work are listed in TABLE 1. This table is useful in narrowing down the possible selection of materials for the device layer.

TABLE 1

PROPERTIES OF SELECTED MATERIALS OF PARTICULAR INTEREST IN THIS WORK [67]

	C	Al	Si	Ti	Cr	Ni	Cu	Ge	Mo	Ta	W	Pt	Au
Atomic number	**6**	**13**	**14**	**22**	**24**	**28**	**29**	**32**	**42**	**73**	**74**	**78**	**79**
Weight [g/mol]	**12.0**	**27.0**	**28.1**	**47.9**	**52.0**	**58.7**	**63.6**	**72.6**	**95.9**	**180.0**	**183.8**	**195.1**	**197.0**
Density [g/cm^3]	**2.27**	**2.7**	**2.33**	**4.51**	**7.14**	**8.91**	**8.92**	**5.32**	**10.28**	**16.65**	**19.25**	**21.09**	**19.3**
Melting point[°C]	**3527**	**660**	**1414**	**1668**	**1907**	**1455**	**1084**	**938**	**2623**	**3017**	**3422**	**1768**	**1064**
Thermal expansion coefficient [10^{-6} K^{-1}]	**7.1**	**23.1**	**2.6**	**8.6**	**4.9**	**13.4**	**16.5**	**6**	**4.8**	**6.3**	**4.5**	**8.8**	**14.2**
Thermal conductivity [Wm^{-1}K^{-1}]	**140**	**235**	**150**	**22**	**94**	**91**	**400**	**60**	**139**	**57**	**170**	**72**	**320**
Electrical resistivity [10^{-8} W m]	**1000**	**2.65**	**10000**	**40**	**12.7**	**7**	**1.7**	**50000**	**5**	**13**	**5**	**10.6**	**2.2**
Young's modulus [GPa]	**4.8***	**70**	**47**	**116**	**279**	**200**	**130**	**130***	**329**	**186**	**411**	**168**	**78**

** Source: [68]. For carbon, the value of Young's modulus is for graphite.*

Molecular interconnects and wirings to nanostructures require materials with low electrical resistivity, therefore Al, Cu, and Au are good candidates. For high temperature applications high melting-point materials are Cr, Mo, Ta, Pt, and W. For oxidative environments the noble metals, Au and Pt, are favorable. Young's modulus and the coefficient of thermal expansion must be considered for nanoelectromechanical devices. Young's modulus determines the stiffness of structures; therefore, it is a primary factor in

the determination of the natural oscillation frequency of a cantilever or the electrostatic force required to deflect a suspended wire.

The melting point is typically directly related to the emission power required to evaporate a material, thus, to the radiative heat generated during the deposition. Materials with high evaporation temperatures require more power (i.e. higher electron-beam current) to evaporate, and because of the heat radiated during the deposition, temperatures of the PEN components must be controlled to avoid thermal expansion shifts.

After the appropriate material that meets the application requirements is selected, the material for the sacrificial layer needs to be identified. Here the main consideration is that the differential etchant should attack neither the device layers nor the substrate. Because Al can be removed in a number of acids (e.g. HCl, H_2SO_4, H_3PO_4) or bases (e.g. NaOH, KOH) and Pt has excellent chemical resistance (e.g. not attacked by any single mineral acid), the Al/Pt material system was identified as a good candidate and studied in detail.

CHAPTER 3

SYSTEM DESIGN AND PROCESS CHARACTERIZATION

3.1 Overview

A system for performing PEN has been designed and constructed in a commercial Airco/Temescal (Berkeley, CA) FC-1800 electron-beam evaporator. The evaporator features a 50.8 cm diameter × 28 cm height stainless steel bell jar and a 45.7 cm diameter stainless steel source chamber with a six-pocket turret and a tungsten filament electron gun. The two chambers are pumped by a mechanical pump and a water-cooled cryopump. One thermocouple gauge for each chamber and one ionization gauge in the source chamber monitor the vacuum. During operation, the pressure in the chambers is typically $0.5 – 2 \times 10^{-6}$ Torr. A direct viewing port facilitates the inspection of the sources during deposition and a quartz crystal monitors the deposition rate and thickness. A 100 mm diameter manual shutter is used to control the deposition start and stop times. The shutter closes in approximately 1.5 seconds giving deposition control at the nanometer scale or below, for deposition rates which are typically below approximately 10 Å/s. A schematic diagram of the evaporator is shown in Figure 3 indicating the geometry of the system and the location of the piezotranslator in the deposition chamber.

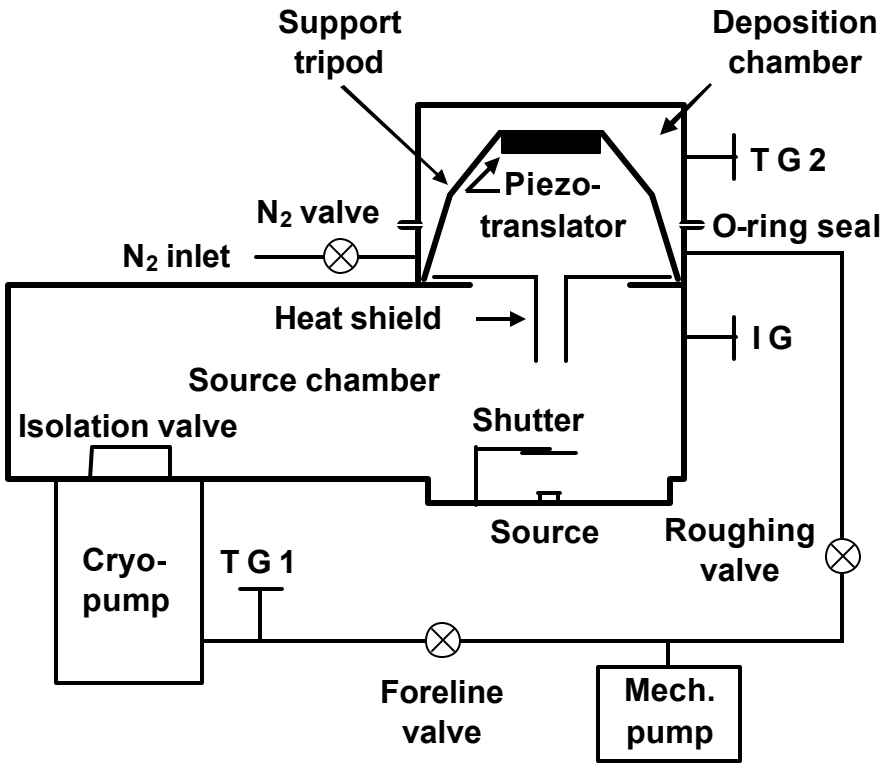

Figure 3. Schematic diagram of the Airco/Temescal FC-1800 electron-beam evaporator with piezoflexure *x*-*y* translator (T G – thermocouple pressure gauge, I G – ion gauge).

The translation of the substrate under the stencil mask is achieved using a commercial piezoelectric *x*-*y* nanopositioner (Type P-731, Physik Intstrumente (PI) L. P., Karlsruhe, Germany) with built-in capacitive sensors and a closed-loop feedback controller. The nanopositioner provides an 80 μm × 80 μm positioning range with 1 nm resolution and 0.03% typical full-range linearity.

A mask-substrate fixture, shown in Figure 4, has been constructed with interconnects to the controller via vacuum feedthroughs. The 100 mm oxidized Si deposition substrate is fixed to the wafer holder on the flexure portion of the *x*-*y* stage using binder clips. The stencil mask, an anisotropically etched double-side-polished (DSP) Si wafer, is placed in

direct contact with the substrate and the mask holder is affixed to the stationary portion of the *x*-*y* stage by three spacers (one shown in Figure 4) that maintain a submillimeter gap between the stencil mask and the mask holder. Upon assembly, the mask is fixed to the mask holder by a low-shrinkage, non-outgasing polymer adhesive (Norland Optical Adhesive 63 (NOA63) by Norland Products Inc., Cranbury, NJ). This high viscosity, 2500 cP (1 centipoise = 1 mPa·s = viscosity of water at 20 °C) adhesive provides a strong bond (~3500 N/cm^2) up to 60 – 90 °C after curing with a 4.5 J/cm^2 long wavelength UV light exposure.

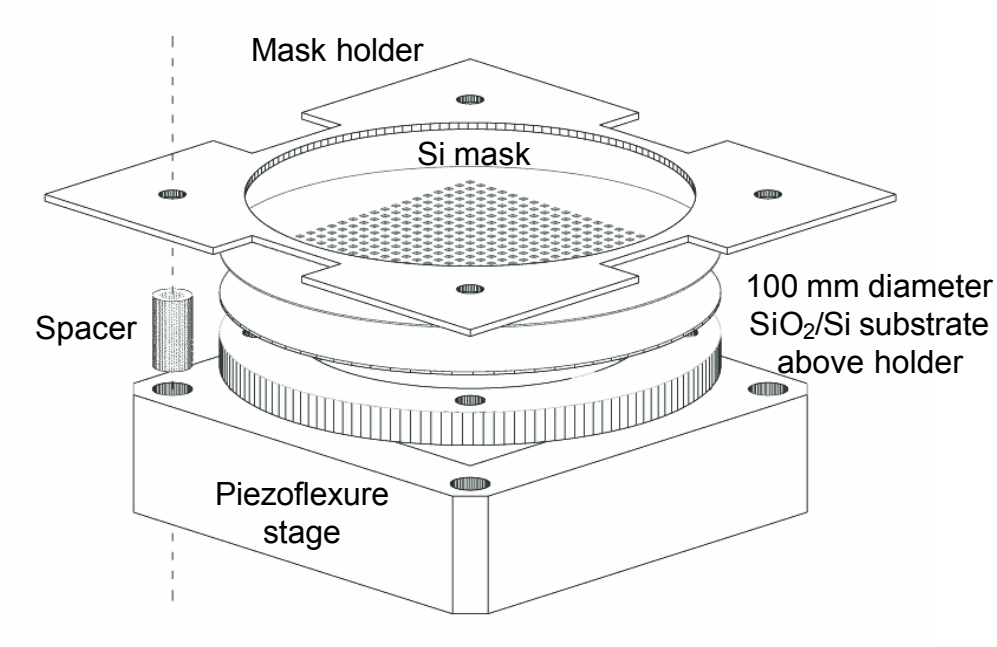

Figure 4. Schematic diagram of the mask – substrate fixture assembly. The wafer holder ring is mounted on the moving middle part of the piezoflexure stage whose motion is controlled by low voltage (0 to 100 V) piezoelectric drives. The mask holder plate is mounted on the stationary frame of the stage at a distance set by spacers.

The entire mask-substrate fixture is mounted onto a stainless steel support tripod which is placed on the rim of the FC-1800 evaporator separating the source and the deposition chambers. The apparatus is shielded from the radiative heat of the deposition sources by a 12.2 mm thick stainless steel plate, heat shield, located on the same rim. A custom designed temperature-controller unit was built using a high accuracy proportional-integral-derivative (PID) temperature controller (Type 3216, Eurotherm Inc., Leesburg, VA) and a silicon-controlled-rectifier power controller (Type 7100A, Eurotherm Inc.). This controller unit drives a 300 W quartz lamp to keep the mask holder at a constant temperature. A self-adhesive, fast-response, type K thermocouple probe (Model SA1, Omega Engineering, Inc., Stamford, CT) is mounted onto the surface of the mask holder to provide closed-loop feedback for the temperature controller. An identical thermocouple probe is used to monitor the temperature of the *x*-*y* stage. After stabilizing at the setpoint temperature, the maximum precision of this active temperature control system, without the deposition source turned on, was measured to be ±0.03 °C.

The entire mask-to-evaporation source distance is 43.3 cm and the mask-to-aperture distance is 29.8 cm. These values determine both the geometrical profile of the sidewall features and the amount of radiative power from the evaporation materials reaching the mask holder during deposition. Figure 5 shows the schematic arrangement of the main components of the PEN system with their relative distances. Within the constraints of the FC-1800 evaporation chamber, these distances are chosen to maximize the steepness of the sidewall slope and minimize the uncontrolled heating of the mask holder and the stage.

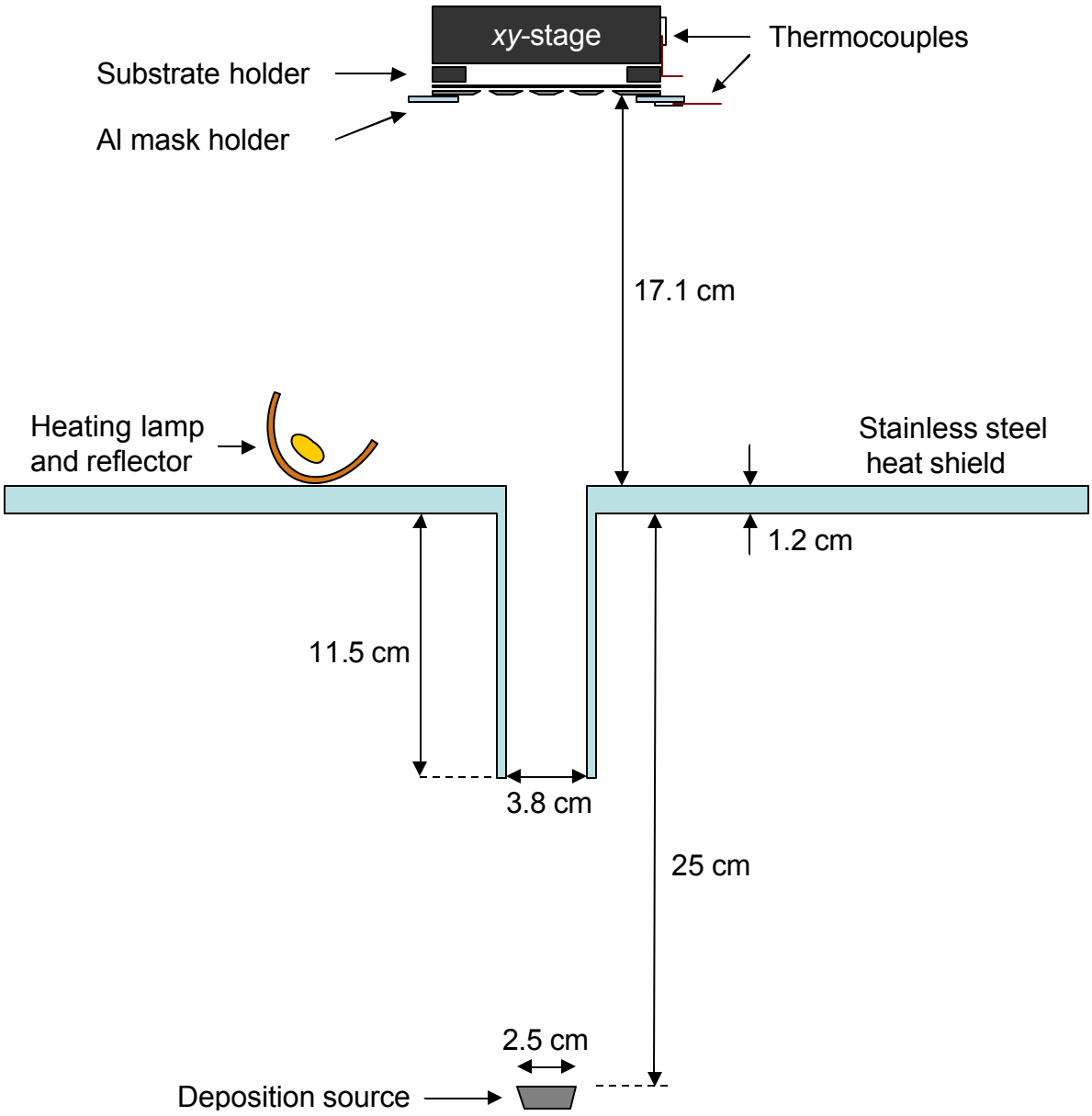

Figure 5. Cross-sectional diagram of the main components of the PEN system with relative distances.

Evaporation in gaseous (e.g. O_2 or N_2) ambient is possible by bleeding gas into the deposition chamber through a stainless steel inlet valve connecting to a gas cylinder. The inlet valve consists of three parts. Two pin valves provide rough and fine control of the gas flow rate and a shut off valve isolates the line when vacuum conditions are required.

Photographs of the Airco/Temescal FC-1800 electron-beam evaporator and the PEN system are shown in Figure 6. The mask-substrate fixture assembly mounted on the support tripod is shown in Figure 6(a) as it appears outside the system during wafer unloading. Deposited metal (the circular region with a dark edge) can be seen on the mask and the mask holder. On close inspection, the four beads of polymer adhesive that attach the mask wafer to the mask holder can also be seen. The mask holder assembly is aligned to the metal deposition source located near the geometrical center of the source tray. Figure 6(b) is a photo taken looking down into the evaporator toward the metal source. Also visible is the manual shutter (in the open position). The heat shield insulating the mask-substrate fixture from the radiative heat of the sources is shown in Figure 6(c). The center opening provides the deposition path from the source to the substrate and the larger circular opening in the heat shield provides line of sight to the crystal monitor located adjacent to the nanopositioner assembly. A custom-built, six-connector, vacuum feedthrough (EWV.00.250.NTLPV and HGP.00.250.CTLPV, LEMO USA, Inc., Rohnert Park, CA), labeled as control feedthrough in Figure 6(c), is used to connect the nanopositioner to the closed-loop position controller unit. In order to maximize positioning accuracy, the controller is driven by PI's PZT Control^{TM} software running on a personal computer.

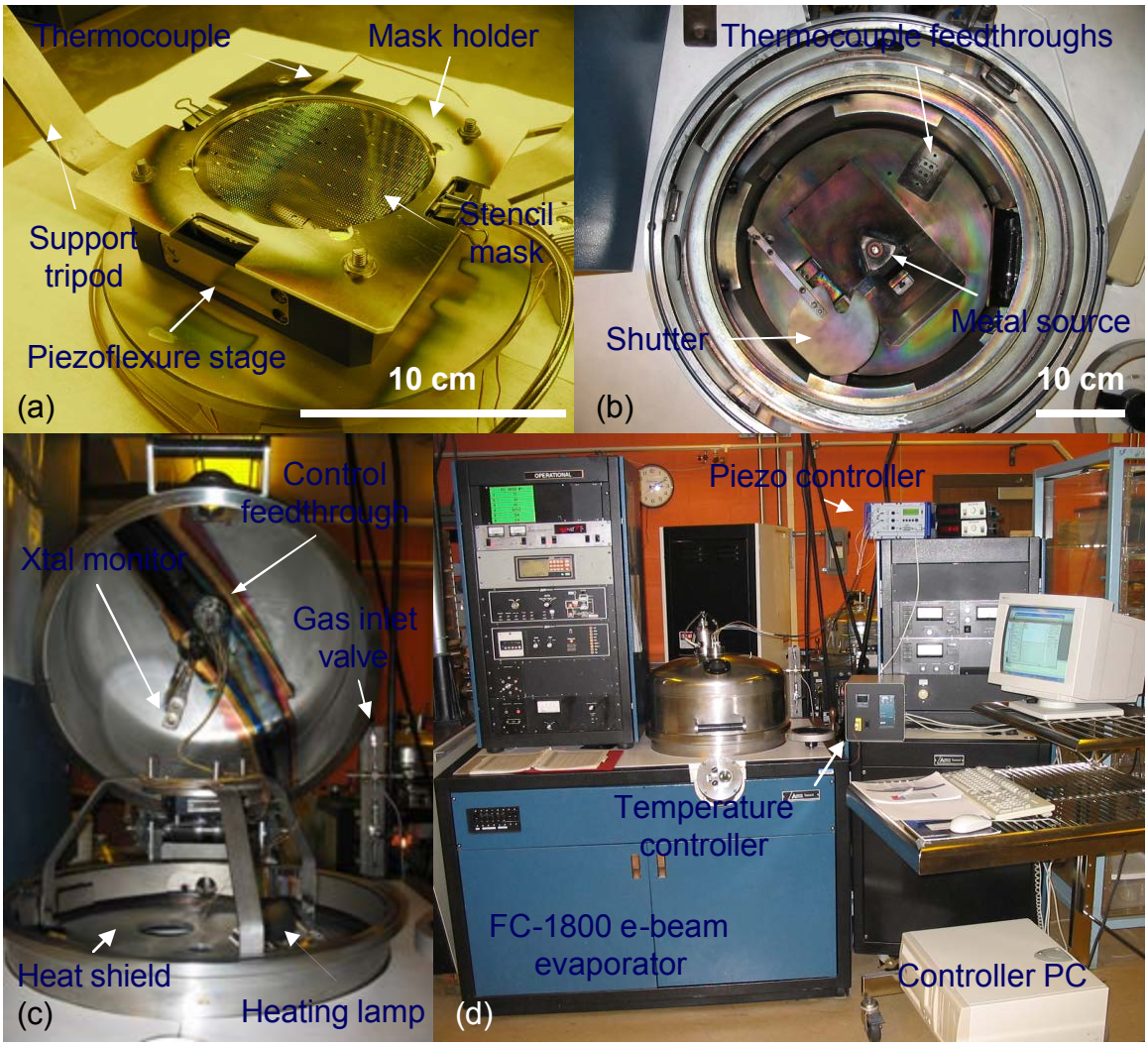

Figure 6. Airco/Temescal FC-1800 electron-beam evaporation system with the piezoflexure-enabled nanofabrication apparatus: (a) mask – substrate fixture assembly mounted on a support tripod, (b) top view of the source chamber, (c) deposition chamber with heat shield, heating lamp, and nanopositioner assembly installed, (d) FC-1800 evaporator with control units.

These units are located adjacent to the FC-1800 evaporator, Figure 6(d). The controller unit has three major modules. The E-509.C2A PZT (Lead-Zirconate-Titanate) servo controller and the E-503 LVPZT (Low Voltage PZT) amplifier control the position and motion of the stage, and the E-516 display/interface module shows the position and provides connection to the personal computer. A Eurotherm temperature controller is also shown in Figure 6(d). This unit receives temperature reading from the low-thermal-inertia thermocouple attached to the mask holder through a thermocouple feedthrough, Figure 6(b), and controls the 300 W quartz lamp mounted on the heat shield. Operation of the temperature controller is directed by the personal computer and temperature readings are recorded throughout the PEN processes. The temperature of the *x-y* stage is monitored in a similar manner by a separate digital thermometer unit (FLUKE 2168A Multi-type Digital Thermometer, John Fluke Mfg. Co., Inc., Everett, WA).

3.2 Source collimation and feature edge taper

Piezoflexure-enabled nanofabrication requires steep sidewalls. The edge sharpness of the sidewalls is determined, at least in part, by the evaporation geometry as illustrated in Figure 7. The width of the edge taper, w, of a deposited feature through a stencil mask due to the geometry of the arrangement is approximately

$$w \cong \frac{h+t}{H} d \tag{1}$$

where h is the substrate-to-mask separation, t is the effective thickness of the mask, H is the mask-to-evaporation source distance, and d is the effective diameter of the evaporation source.

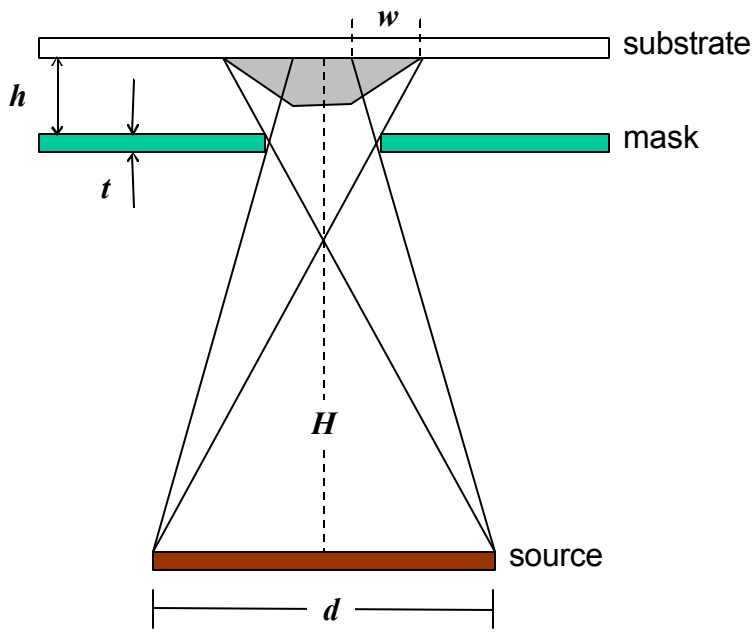

Figure 7. Schematic diagram defining the geometrical relationship between evaporation source, stencil mask, and deposition substrate. The sidewall taper (w) is determined geometrically by the source size (d), the distance between the source and the substrate (H), the mask thickness (t), and the separation between the mask and the substrate (h).

Sharp sidewalls require thin masks, large source-to-substrate distance, and a small or collimated evaporation source which can be achieved by evaporating without beam rastering or by placing an aperture in the deposition path. For the system constructed here, $h+t$ is estimated to be less than 1 μm with the mask in contact mode, the source-to-substrate throw, H, is approximately 43 cm, and the effective source size, d, is 3 mm, therefore the edge taper is expected to be less than 6 nm.

3.3 Piezonanotranslator performance

The accuracy of the piezoactuator sets a dimensional limit on the PEN technique. Physik Instrumente, the manufacturer of the *x*-*y* nanopositioner used in this work, characterizes the stage linearity by supplying control input values to the stage controller and measuring the position of the stage using laser interferometry that has 0.3 nm accuracy. The results of these measurements are provided in TABLE 2.

This data shows that although the nanopositioner has 1 nm resolution, the target positions and the actual positions of the stage differ by 9 nm on the average and by as much as 12 nm for channel 1 and 16 nm for channel 2. According to PI, this deviation can arise from misalignment, the imperfect parallelism of the capacitive sensors, or from friction between the actuator and the flexure stage. Channel 1 has the smaller nonlinearity of the two channels; therefore, this channel is more suitable for nanoscale feature control. Figure 8 shows the measured positions and the translation error for channel 1 and 2 for closed-loop operation with a full range repeatability of ±5 nm according to PI. For shorter ranges, the repeatability is significantly better [69].

TABLE 2

NANOPOSITIONER CALIBRATION DATA PROVIDED BY PHYSIK INSTRUMENTE L. P. CHANNEL 1 AND CHANNEL 2 REFER TO THE *X* AND *Y* AXES OF THE PIEZOFLEXURE STAGE.

	Channel 1		**Channel 2**	
Control input [µm]	**Output [µm]**	**Nonlinearity [nm]**	**Output [µm]**	**Nonlinearity [nm]**
0.000	0.000	0	0.000	0
4.706	4.714	8	4.700	-6
9.412	9.421	9	9.400	-12
14.118	14.126	8	14.104	-14
18.823	18.829	6	18.807	-16
23.529	23.535	6	23.515	-14
28.235	28.241	6	28.221	-14
32.941	32.947	6	32.929	-12
37.647	37.654	7	37.637	-10
42.353	42.364	11	42.348	-5
47.059	47.067	8	47.054	-5
51.765	51.775	10	51.777	12
56.471	56.483	12	56.474	3
61.176	61.188	12	61.182	6
65.882	65.894	12	65.890	8
70.588	70.599	11	70.595	7
75.294	75.305	11	75.301	7
80.000	80.009	9	80.004	4

Note: For a given stage input, the output position is measured by laser interferometry. The nonlinearity is the difference between the desired and the actual position.

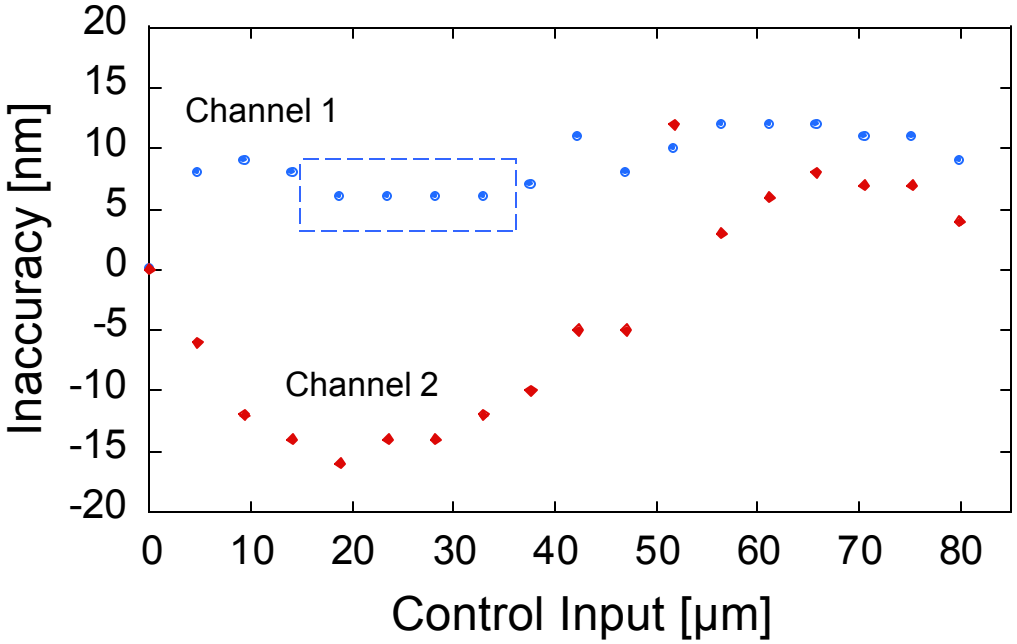

Figure 8. Position vs. nonlinearity curve for channel 1 and channel 2 of the nanopositioner. Markers indicate the measured data of TABLE 2. The dashed box indicates the most linear range of the nanopositioner.

Using the data in TABLE 2, it is possible to calculate the setpoints for the desired positions. Alternatively, the stage can be operated in its most linear range. For example, channel 1 between positions 18 and 38 µm, dashed box in Figure 8, gives an inaccuracy of 3 nm, therefore, with a 3 nm offset, nanometer scale positioning can be achieved at the expense of shorter stage travel.

3.4 Temperature control and thermal expansion

Electron-beam or thermal evaporation of materials is accompanied by electromagnetic radiation from the evaporation source. This energy heats the source and the deposition chamber causing thermal expansion and unintended motion of the source, mask, and deposition substrate. The effect of this heat can be estimated assuming that the evaporating metal sources are black-body radiators at their equilibrium temperature at a given vapor pressure. According to the Stefan-Boltzmann Law, the radiated power emitted by a non-ideal radiator object at temperature T is

$$P = e\sigma A_e \left(T^4 - T_s^4\right) \approx e\sigma A_e T^4 , \tag{2}$$

where e is the emissivity (the ratio of radiation energy emitted by an object relative to that of a black body at the same temperature), σ is Stefan's constant (5.6703×10^{-8} $Wm^{-2}K^{-4}$), A_e is the surface area of the emitting body (9.8×10^{-4} m^2 for a 25 mm diameter hemisphere-shaped deposition source) and T_s is the temperature of the surroundings (294 K).

The energy, E, radiated from a metal source onto and absorbed by a surface, A_a, with reflectivity, R, in a distance, r, during a deposition interval, t_{dep}, based on geometrical considerations is

$$E = (1 - R)\frac{A_a}{4r^2\pi} P t_{dep} . \tag{3}$$

The relation between this energy and the increase in the temperature of the mask holder is

$$E = Cm\Delta T = C\rho V\Delta T = C\rho A_a l\Delta T\,, \tag{4}$$

where C is the specific heat, ρ is the density, and l is the thickness of the aluminum mask holder. Therefore, the temperature of the mask holder will be

$$\Delta T = \frac{(1-R)Pt_{dep}}{4\pi r^2 C\rho l}. \tag{5}$$

For example, consider the evaporation of Ti with $r = 0.43$ m, t_{dep} = 60 s, l = 1.35 mm, and the deposition source at 1940 K. The hemispherical liquid phase total emissivity of Ti is 0.34 [70]. To estimate the reflectivity of the mask holder, it is assumed that during most of the deposition it is covered by titanium. The reflectivity of titanium is a function of the wavelength of the incident radiation, and the value corresponding to the maximum intensity wavelength of radiation curve is used. Based on Wien's Displacement Law, the maximum intensity wavelength of an object at 1940 K is 1.49 μm and the corresponding reflectivity of titanium is 0.596 [71]. For such a deposition, the estimated temperature increase due to radiation during the deposition is 0.85 K. This is in good agreement with experimental observations with the temperature increasing at approximately 0.7 °C per minute of evaporation. The picture in reality is more complicated because the radiation reflected off the deposition chamber walls is ignored. This reflected radiation is known to be significant since the mask holder temperature increases even when the source is blocked by the shutter. Also, the temperature and the material phase of the deposition source were assumed to be uniform, and surface roughness of the mask holder and the source was not included in the reflectivity and emissivity values.

Another source of heat is from the kinetic energy, E_k, of the evaporated atoms as they condense on the deposition substrate, the mask, and the mask holder. This can be readily

shown to be negligible. The average kinetic energy for a Ti atom is $E_{avg} = 3kT/2$, therefore, the total kinetic energy is

$$E_k = NE_{avg} = \tfrac{3}{2}NkT, \tag{6}$$

where N is the number of atoms condensing on the surface. Assuming that all the kinetic energy is converted to heat, similarly to Eq.(4), the temperature increase due to evaporated atoms condensing on a 1 cm^2 surface is

$$\Delta T = \frac{E_k}{crl}. \tag{7}$$

Again, as an example consider the deposition of 100 Å of Ti. From the density and molar mass values for Ti, 4.51 g/cm^3 and 47.48 g/mol respectively, the number of atoms per unit area and the atomic diameter can be estimated to be 1.48×10^{15} atoms/cm^2 and 2.6 Å respectively. Thus, during the deposition of 100 Å Ti, $N = (100\text{ Å}/2.6\text{ Å})1.48\times10^{15}\text{atoms/cm}^2\,(1\text{cm}^2) = 5.69\times10^{15}$ Ti atoms condense on a surface area of 1 cm^2 which results in a 5.4 mK temperature rise, a negligible amount in comparison with the radiative contribution.

An increase in temperature causes thermal expansion in most materials. Since the cornerstone of the PEN technique is the translation of a substrate relative to a fixed mask (mounted on a mask holder), drift caused by the thermal expansion impacts the resolution and accuracy of the technique and must be minimized.

The impact of mask drift due to thermal expansion became obvious when consecutive layers of different metals were deposited without the heat shield or active temperature

control installed. A four-layer structure was created by successive depositions of Al, Pt, Al, and Pt. Each deposition was followed by the translation of the substrate. First 88 nm Al was deposited at a rate of 2.4 Å/s. After a 5 minute delay, the substrate was translated by 5 μm in the horizontal and 0.025 μm in the vertical direction and 33 nm Pt was deposited at 1.1 Å/s. After a 10 minute delay, the substrate was translated by 1 μm in the horizontal and 0.050 μm in the vertical direction and a second layer of 88 nm Al was deposited at 2.3 Å/s. Finally, following a 5 minute delay and the translation of the substrate by 5 μm in the horizontal and 0.025 μm in the vertical direction, 33 nm Pt was deposited at 1.1 Å/s. The corners of the expected structure to be formed are shown in Figure 9.

Scanning electron microscope images of the actual structure that was formed are shown in Figure 10. The adverse effects of the thermal motion of the stencil mask are easily recognizable. The translation targets for the first Pt layer was 5 μm horizontally and 25 nm vertically, for the second Al layer 6 μm horizontally and 75 nm vertically, and for the second Pt layer 11 μm horizontally and 100 nm vertically relative to the upper left corner of the first Al deposition. The dashed lines show where the corners of each consecutive layer had been designed to be formed. Since the mask holder and the mask were not allowed to cool down to the starting temperature, their thermal expansion due to radiative heat introduces absolute inaccuracies in the positioning of the features.

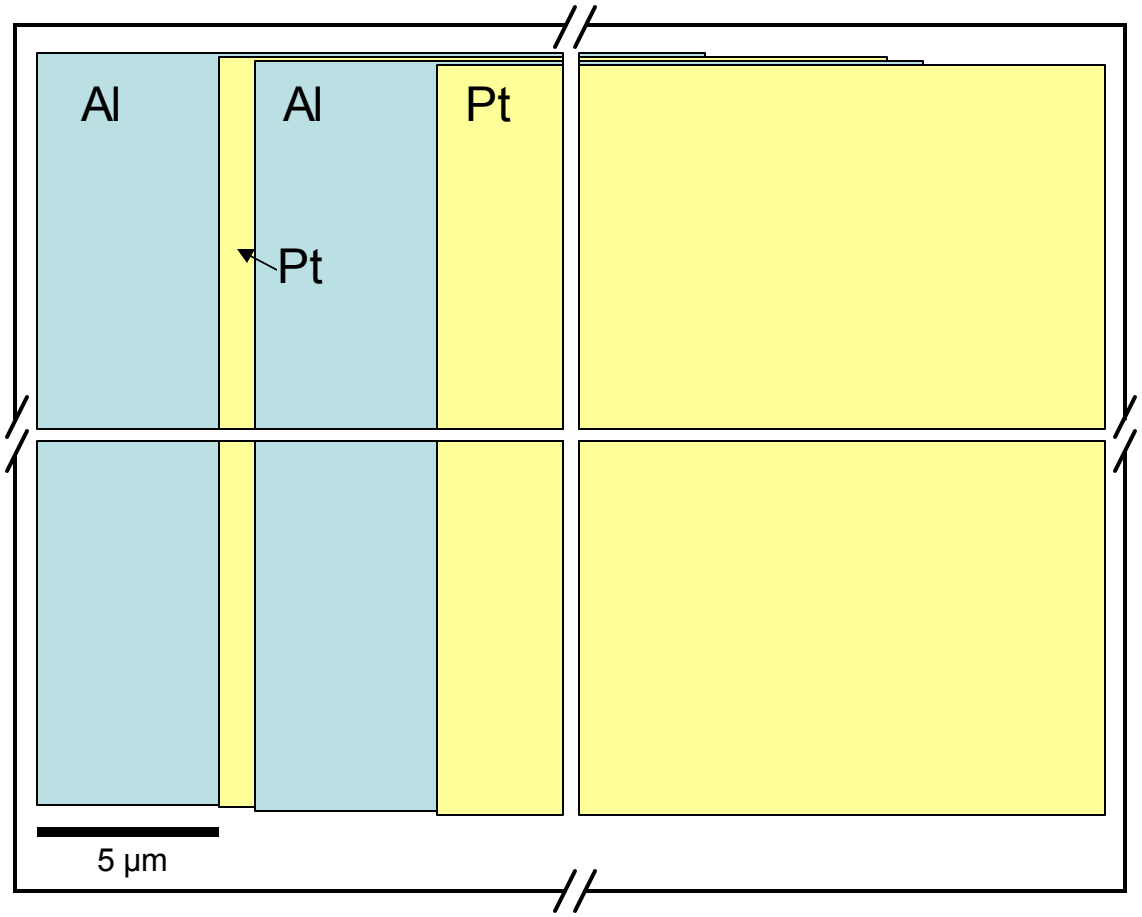

Figure 9. Schematic drawing of the corners of the structure expected to be formed after a sequence of Al, Pt, Al, and Pt depositions through a rectangular stencil aperture.

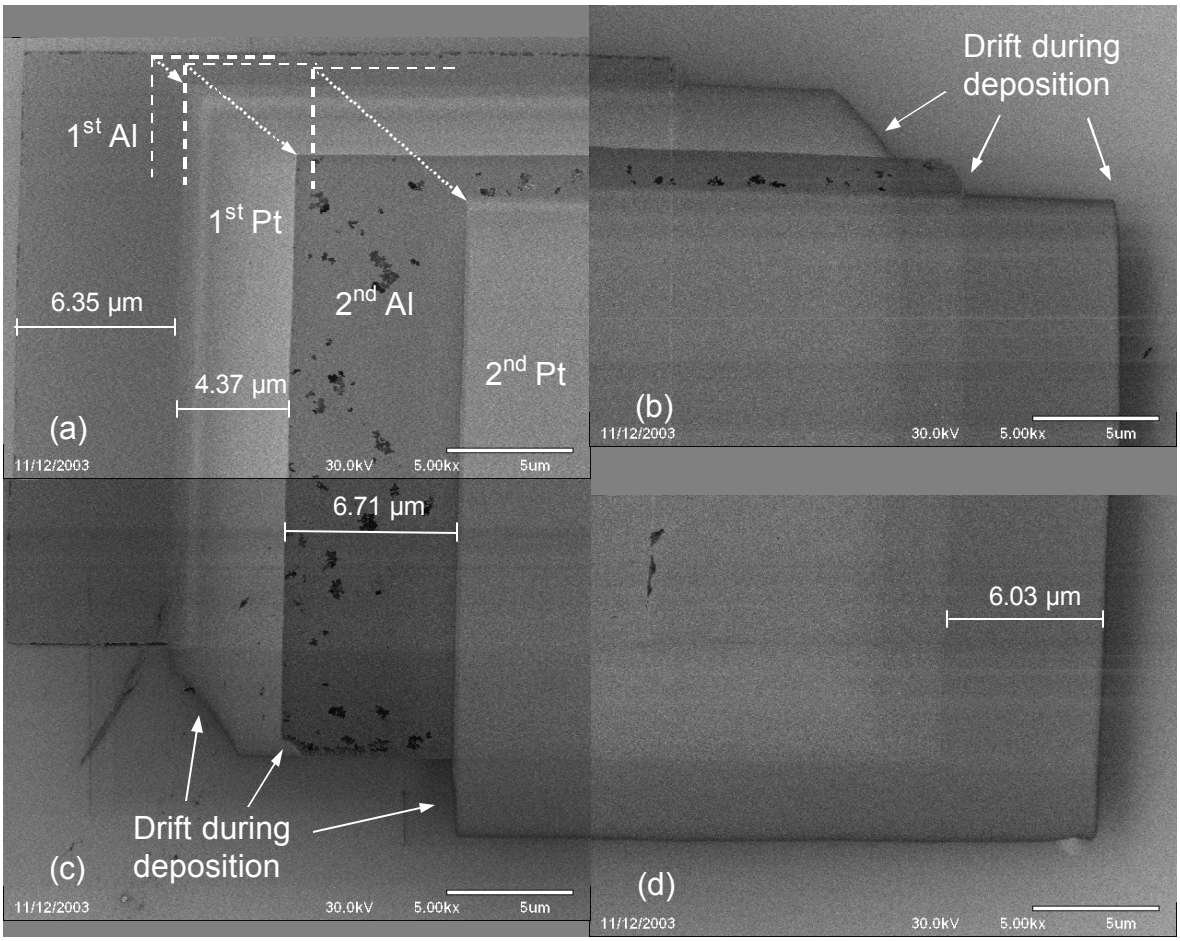

Figure 10. Composite picture comprised of four scanning electron microscope images of the four corners of a Pt/Al/Pt/Al/SiO_2 structure illustrating the effect of thermal expansion of the mask and the mask holder during depositions: (a) upper left corner of the structure, dashed lines indicate the target positions of the corners of the different layers, dotted arrows point in the direction of offsets caused by the increased temperature of the apparatus, (b) upper right corner of the structure, solid arrows show the effect of mask drift during depositions, (c) lower left corner of the structure, solid arrows show the effect of mask drift during depositions, (d) lower right corner of the structure.

The dotted arrows show the direction of these offsets. In this particular case, the inaccuracies in positioning caused by the increased temperature of the apparatus at the start of each deposition range from 1.17 to 3.37 μm.

In addition, a second undesired effect arises. As the temperature of the mask and the mask holder increases during the depositions, additional undirected translations are introduced due to the thermal expansion of the mask and the mask holder. The smearing of the corners of the deposited rectangles, indicated by the solid white arrows in Figure 10(b) and (c), is a direct result of this mask drifting during deposition. The extent of this effect ranges from 2.3 to 4.2 μm for Pt and from 0 to 0.7 μm for Al. The higher drift values for Pt can be attributed to its higher melting point resulting in greater radiative emission. By calculating the thermal expansion of the mask holder, the temperature increase due to radiation during deposition that would produce these shifts can be estimated. The change in the length of an object, Δl, due to a change in its temperature, ΔT, is

$$\Delta l = l_0 a\ \Delta T, \tag{8}$$

where l_0 is the initial length of the object and a is the coefficient of thermal expansion. The mask holder in this experiment is a 10×10 cm^2 Al plate with the mask located in the center. Assuming that the mask holder can expand in only one direction, the temperature change required to cause a 4.2 μm shift at a point located at the center of the mask holder is 3.6 ℃.

The heat generated during the Pt deposition can be calculated by substituting the corresponding constants for Pt in Eqs. (2) – (5). The emissivity of Pt is 0.288 [72], its reflectivity at the maximum intensity wavelength, 1.42 μm, at the melting point, 2040 K, is 0.763 [73], and the deposition time is 300 s. Thus, the estimated temperature increase is approximately 2.6 ℃ which is in quantitative agreement with the expected value calculated from the thermal expansion of the mask holder.

Thermal effects of this proportion show the necessity for thermal shielding and closed-loop temperature control of the mask-substrate assembly.

It is interesting to note in Figure 10 that around the first Al layer and on the surface of the second Al layer, irregular dark spots are visible. Aluminum films deposited on Pt are known to develop voids after annealing between 200 and 300 °C for 30 minutes or at room temperature after storage for 6 months [74]. Formation of the voids is related to Al/Pt compound formation at the interface and surface tension driven mass transport. Although not as high as in [74], the elevated substrate temperature during deposition may be related to the formation of voids seen in Figure 10.

Based on these findings a 1.2 cm thick stainless steel heat shield was installed to limit radiative heating. The positioning accuracy was significantly improved and mask drifting during deposition was essentially eliminated as it can be seen from the results of the following experiment performed with the heat shield installed. The objective of the experiment was to form five 400, 200, 100, 50, and 25 nm wide Ti nanowires between Ti contact pads on SiO_2 using Al as the sacrificial layer. The target PEN structure is shown

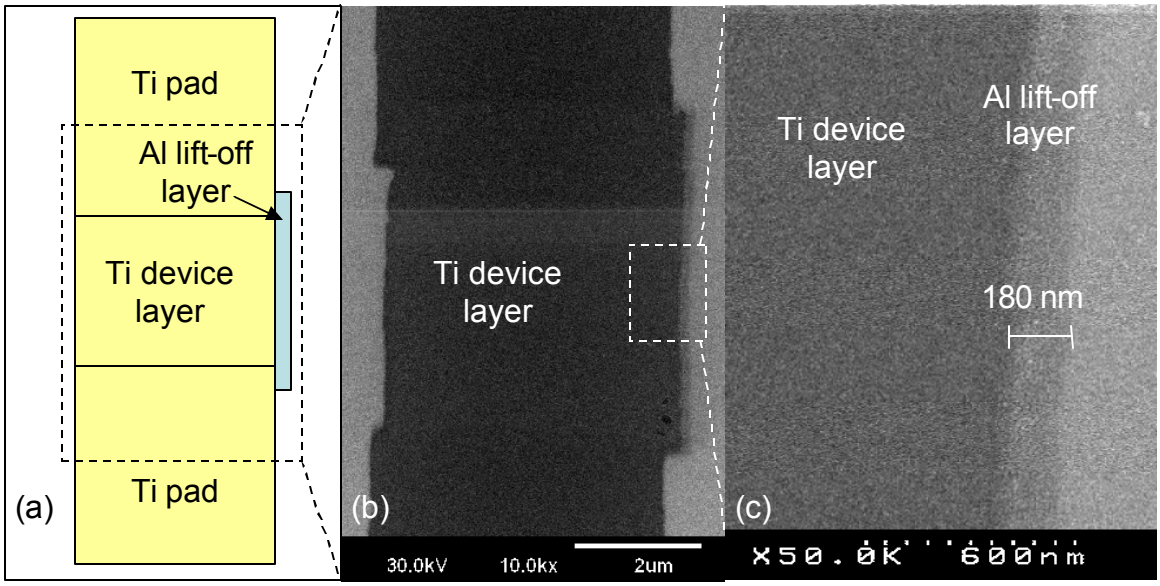

Figure 11. (a) Schematic drawing of the target structure created by a sequence of Al and Ti depositions designed to form a Ti wire between two Ti pads, (b) scanning electron microscope image of the actual Ti/Al structure after deposition, (c) magnified view of the right central edge of the same structure, indicated by the dashed box. The difference between the Ti and the Al layer is ~180 nm instead of the expected 400 nm.

in Figure 11(a). Five of these structures were created by the following deposition sequence.

First, the five 22 nm thick Al sacrificial layers were deposited at a deposition rate of 4 Å/s, followed by the five 11 nm Ti device layers at 2 Å/s. Finally, 11 nm thick Ti pads were deposited at 3 Å/s, five at the top and five at the bottom, overlapping the device layers. Figure 11(b) shows the SEM micrograph of the PEN structures after deposition created to form the 400 nm nanowire. The target areal difference between the Al and the Ti layers was 400 nm, however, the magnified image of the edge of the middle structure, Figure 11(c), reveals that the dimension defined by the translation of the mask is only

180 nm. For the other structures, the target values were 200, 100, 50, and 25 nm, and the measured dimensions were 160, 100, -70, and -240 nm respectively, negative values indicating that the Al layer was overlapped by the Ti layer on the right side of a structure. These differences are attributed to the temperature related motion of the mask during deposition.

This inaccuracy in translation is also visible at the position of the Ti pads relative to the Ti device layer. As shown in Figure 11(a), the three Ti layers should align vertically, however, there is a 200 nm offset for the top pad and a 300 nm offset for the bottom pad. The larger misalignment for the bottom pad can be attributed to the fact that the top pads were deposited first and the temperature increase during these depositions increased positioning inaccuracy for the bottom pads.

The temperature of the mask holder was measured using a washer terminated thermocouple (Model WT, Omega Engineering, Inc., Stamford, CT) mounted onto the surface of the mask holder adjacent to the stencil mask. Similarly, the temperature of the heat shield at its lowest point, approximately 10 cm above the deposition source, was measured using a metal-sheathed adjustable-depth thermocouple probe (Model ADR, Omega Engineering, Inc., Stamford, CT). The measured temperature vs. deposition number profile,

Figure 12, shows the temperature of the mask holder and the heat shield for each deposition.

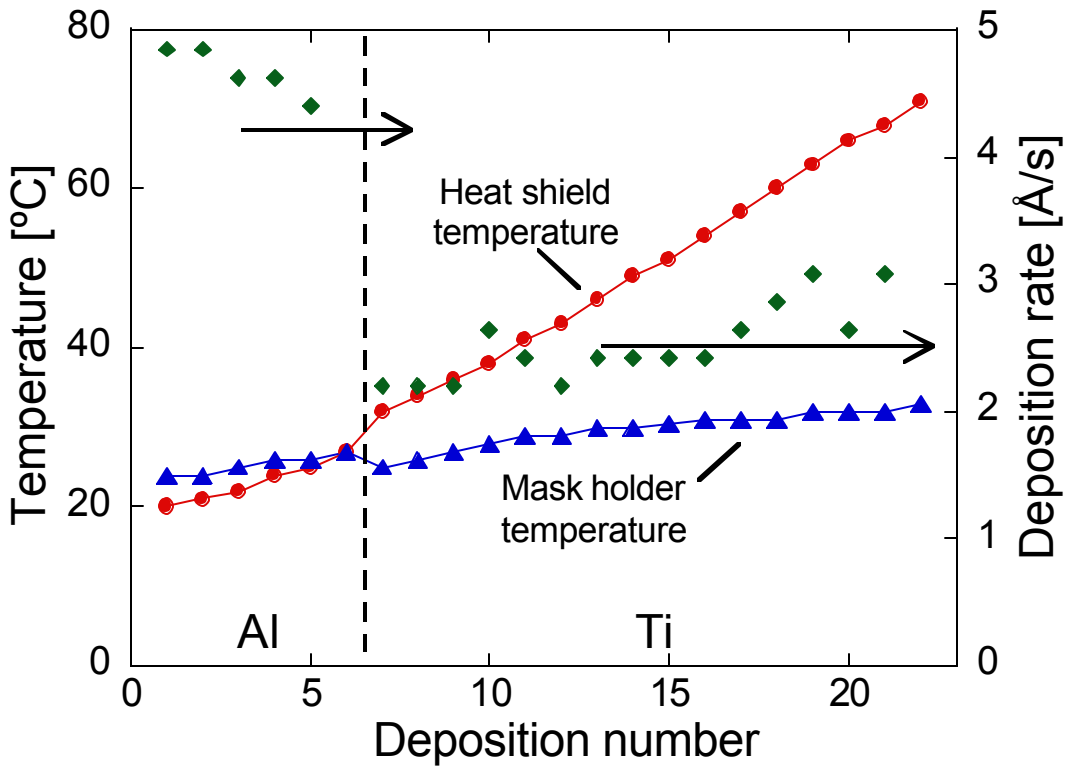

Figure 12. Temperature vs. deposition number (time) profile of a sequence of Al and Ti depositions. Deposition rates are indicated by solid diamond markers.

The sources were continuously operated for all of the depositions, i.e. the electron-beam was not turned off, and the metal beam was shuttered on and off. The temperature increased by 3 °C (from 24 °C to 27 °C) during the five Al depositions (236 s total deposition time) and by 8 °C (from 25 °C to 33 °C) during the deposition of the fifteen Ti layers (661 s). The measured 0.7 °C/min temperature rise is in good agreement with estimates of 0.85 °C shown in Section 3.4.

The structures created in this experiment showed that by blocking the reflected radiated heat using a heat shield, thermal drift during deposition is eliminated and the positioning precision is improved compared to depositions performed without a heat

shield. It is also evident that thermal shielding cannot totally eliminate the problem of radiation because radiative heat can still reach the mask holder and the mask through the deposition aperture.

A possible way to eliminate the positioning inaccuracies is to perform each deposition at the same starting temperature. For this a time delay (10 – 20 minutes) was inserted between depositions to allow the assembly to cool back to the system ambient temperature. The previously described experiment aimed at forming five Ti nanowires of varying widths with Ti contact pads was repeated with each deposition starting at 22 °C mask holder temperature. The deposition rate for the Al layers was approximately 5 Å/s and 1.5 Å/s for the Ti layers.

During the deposition sequence, the temperature of the mask holder and the heat shield was measured, Figure 13. During each Al deposition the mask holder temperature increased by approximately 1 °C (from 22 °C to 23 °C). The mask holder temperature returned to 22 °C in 11 min on average during which time the electron-beam was turned off. During each Ti deposition, the mask holder temperature increased by 2 °C (from 22 °C to 24 °C) and it took 20 minutes on average for the mask holder to cool back to the starting temperature. In the final deposition of the Ti measuring pads the electron beam gun was constantly on and during the translation of the substrate, the shutter was closed to block the beam of metals. The mask holder was not allowed to cool down between depositions and the temperature increased from 22 to 30 °C in approximately 12 minutes.

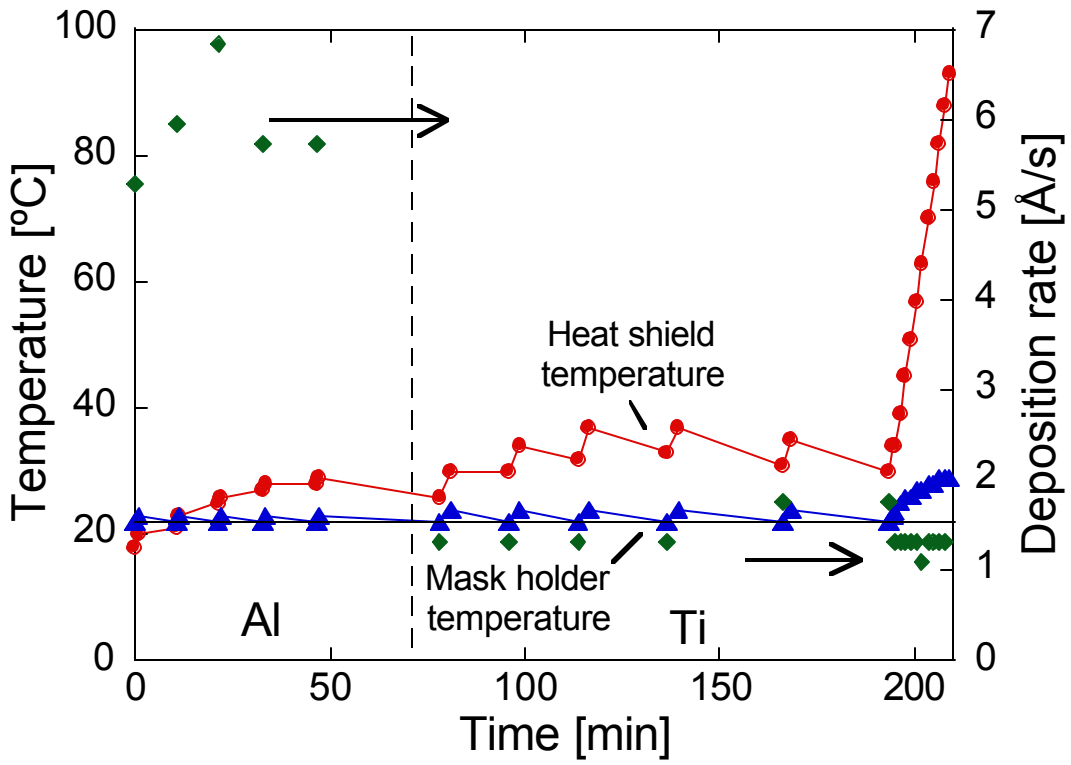

Figure 13. Temperature vs. time profile of a sequence of Al and Ti depositions where the mask holder was allowed to cool back to its starting temperature after each evaporation. The solid vertical line indicates a change in source metals. The dashed horizontal line indicates the starting temperature of the assembly, 22 °C. Deposition rates are shown by solid diamond markers and the scale is on the right axis.

The target structure and the right central edges of the five structures are shown in Figure 14(a). Scanning electron microscope images of the right central edges of the structures, Figure 14(b), show that the target areal differences of 400, 200, 100, 50, and 25 nm were very precisely formed, with a maximum inaccuracy of 27 nm.

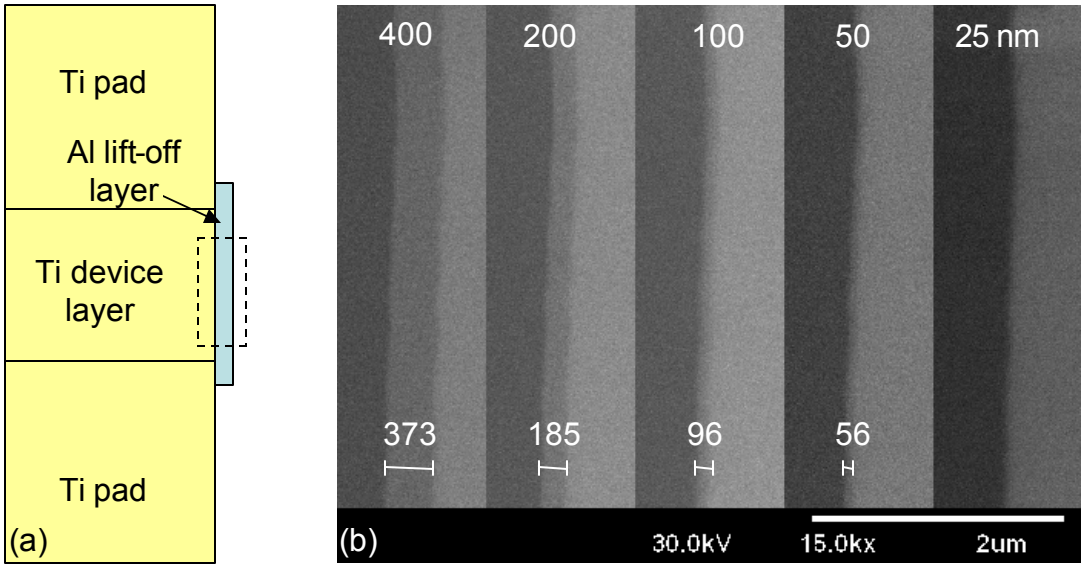

Figure 14. (a) Schematic drawing of the target structure created by a sequence of Al and Ti depositions designed to form a Ti wire between two Ti pads, (b) scanning electron microscope image of the right central edge of five Ti/Al structures after deposition, designed to form a 400, 200, 100, 50, and 25 nm Ti wire between two Ti pads. The maximum positioning inaccuracy is 27 nm.

Although this passive temperature control reduces the positioning inaccuracy caused by thermal expansion, it has two drawbacks. It increases the deposition time for each structure by approximately 20 minutes which limits its usefulness for creating arrays of devices, and it does not prevent the mask from flexing during the thermal cycling which could produce random errors associated with stick and slip of the mask on the substrate. Furthermore, it works best for low melting point metals such as Al and Ti. For high melting point metals, Pt and W, longer cool-down delays and greater temperature excursion can be expected.

As discussed in Section 3.1, a closed-loop active temperature control system consisting of a high-accuracy temperature controller, a quartz heating lamp, a low-

thermal-inertia thermocouple and a personal computer was incorporated into the PEN system to keep the mask-substrate fixture at constant temperature during and between depositions. The method used is to preheat all components to a given temperature using a quartz lamp driven by a PID temperature controller. Once a deposition starts, the power output of the quartz lamp is lowered by the PID controller by the amount of radiative heat reaching the mask holder from the deposition source. The mask holder temperature vs. deposition time profile during sequential depositions of Al, Ti, Pt, Cr, and Ge at a temperature setpoint of 45 °C is shown in Figure 15.

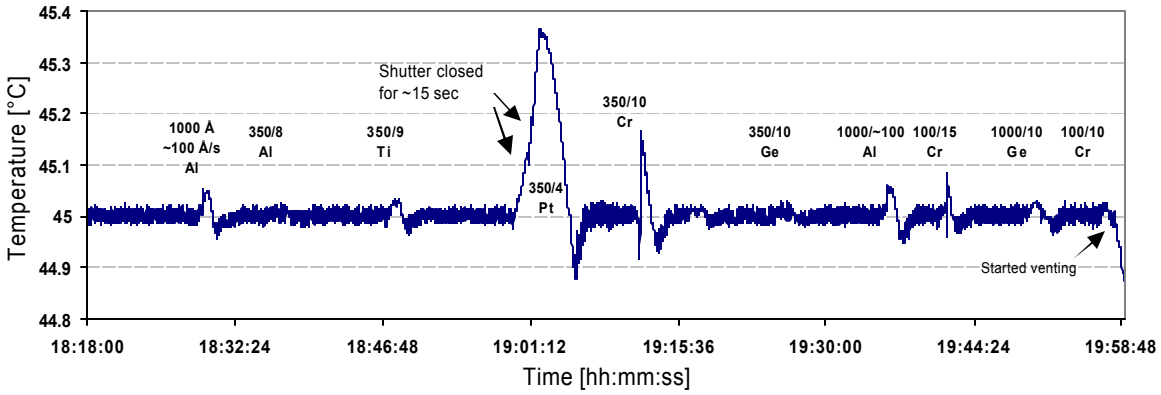

Figure 15. Measured temperature at the mask holder vs. time profile during subsequent depositions of Al, Ti, Pt, and Cr. For Al, Ti, and Ge depositions the temperature increase was less than 0.05 °C, however, Pt and Cr depositions caused the mask holder temperature to increase by as much as 0.36 °C.

The temperature before starting the depositions is held very tightly at the setpoint (45 ± 0.02 °C) as shown in Figure 15. This precision was achieved using the automatic tuning function of the Eurotherm 3216 controller to set the PID parameters (Proportional Band: 1.7826 °C, Integral Time: 44.142 s, Derivative Time: 7.3570 s). For most depositions the temperature increase was less than 0.09 °C, however, it can be seen that

for an approximately 90 second deposition of Pt the temperature of the mask holder increased by more than 0.36 °C. The reason for this temperature increase during deposition is that since active temperature control is based on switching a radiative heat source on and off (i.e. active cooling is not present), this method can only compensate for radiative heat coming from a deposition source that does not exceed the power output of the quartz lamp that is necessary to maintain a given temperature setpoint. To lower this temperature rise, a higher temperature setpoint would need to be used or the Pt deposited in two depositions with a brief cool period.

Increasing the temperature setpoint improves the temperature stability. This is supported by measurements showing that during Pt deposition the temperature of the mask holder increased 2.1 times faster when the temperature setpoint was 35 °C instead of 45 °C (5.5×10^{-3} and 2.6×10^{-3} °C/s, respectively). However, while the translator stage is rated for operation in the temperature range of -20 to 80 °C, the stage translation range decreases with temperature. As the mask holder is preheated, the temperature of the nanopositioner stage increases as well and is not held at the same temperature as the mask. Measurements show that after three and a half hours, the temperature of the stage reaches approximately 90% of the temperature of the mask holder. At 40 °C stage temperature, the range of motion of the piezoactuators was measured to decrease by approximately 12%. A 45 °C mask holder temperature appears to be a good compromise enabling close temperature control (+0.36/-0.12 °C) without greatly compromising the translation range for multiple structure formation.

3.5 Mask alignment relative to translation axes

During mask mounting, the stencil mask is approximately aligned, by eye, to the translation axes of the *x*-*y* piezotranslation stage with an estimated alignment accuracy of ±2°. Misalignment of these two axes can introduce unintentional edge features in sidewall processing, which are illustrated in Figure 16. Top views of 2 metal depositions separated by a single horizontal translation are shown in Figure 16(a) for a perfectly aligned mask and stage. On differential etching, the edge feature shown in Figure 16(b) is expected. If the mask is misaligned relative to the stage by an angle, α, Figure 16(c), a pure horizontal translation forms an "L-shaped" polygon, Figure 16(d). The dimensions of the "L-shaped" structure are given by $\Delta x' = \Delta x \cos\alpha$ and $\Delta y' = \Delta x \sin\alpha$. For an alignment error of 2° and a 100 nanometer translation the deviation, $\Delta x - \Delta x' = \Delta x(1 - \cos\alpha)$, is less than 1 Å, therefore, misalignment is not a significant factor in the formation of nanometer-scale edge features. Because of this small expected shift due to misalignment we interpret the formation of unintentional "L" features as arising from thermal shifts, sticking, or diffusion under the stencil mask. While misalignment errors have little bearing on nanoscale device fabrication, it does work against precise location of a nanodevice in the 80 μm × 80 μm *x*-*y* translation range of the stage, e.g. an *x*-translation of 80 μm with a 2° misalignment results in an absolute *y*-positioning error of 2.8 μm.

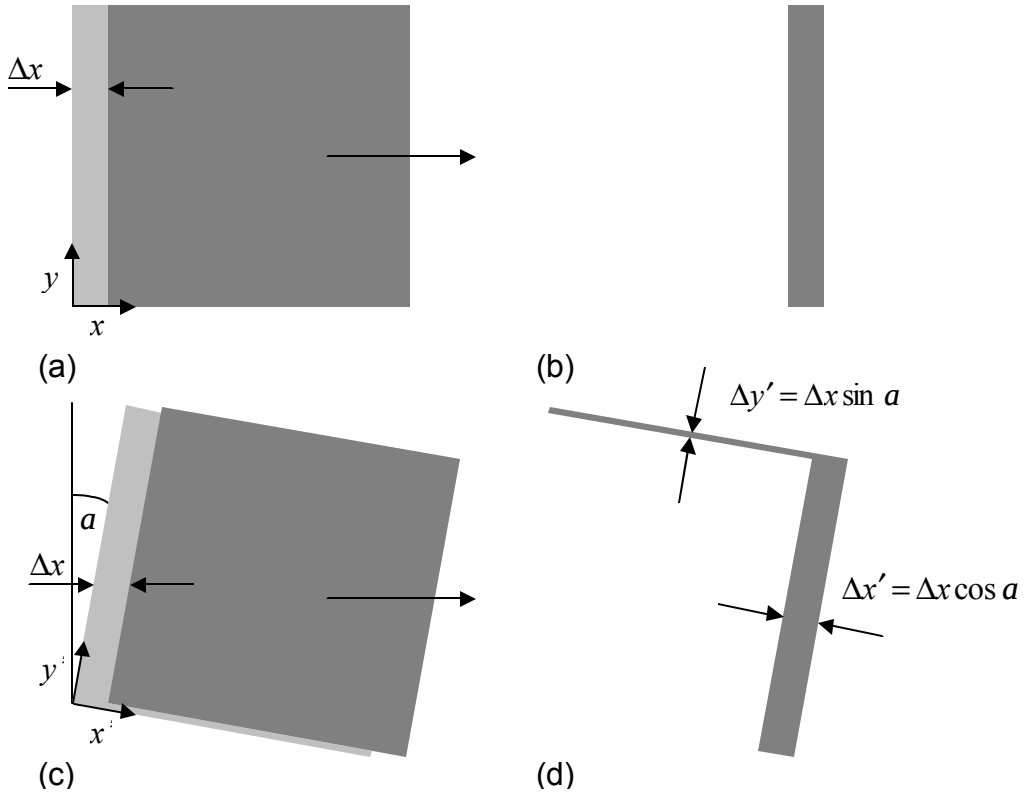

Figure 16. Illustration depicting how misalignment of a rectangular stencil mask changes the final geometry of a structure created with piezoflexure-enabled nanofabrication, where a is the angle of misalignment.

3.6 Stencil mask clogging

An inherent property of evaporation through a stencil mask is the gradual clogging of the mask due to evaporated atoms condensing on the side of the mask openings. The amount of material adhering to the wall of a mask aperture is determined by the cross-sectional size and shape of the aperture, the deposited material, the mask material, and the rate of atomic diffusion in the vicinity of the aperture; thus all of these properties are related to the temperature of the mask. It has been shown by Deshmukh et al. [14] that through Si_3N_4 stencil masks with 20 and 40 nm diameter apertures, Er depositions with a thickness of approximately 1.5 times the hole diameter, and Au features with a thickness

of approximately 3 times the hole diameter can be achieved before the complete closing off of the mask. Kölbel et al. have shown that the effects of clogging can be reduced by coating stencil masks with self-assembled monolayers [35]. Alkyl and perfluoroalkyl self-assembled monolayer coatings proved to remarkably reduce the adhesion of gold inside the apertures of silicon nitride nanostencils, thus, increasing the amount of deposited material through the holes by more than 100% [35].

Analysis of SEM images taken of rigid Si masks in this work shows that during the deposition of a 92 nm thick Pt/Al layer, a 67 nm wide layer of Pt/Al builds up on the (111) face of the aperture opening, resulting in an approximately 21 nm decrease in the size of the mask opening. Figure 17 is a set of cross-sectional SEM images of KOH-etched Si used as a stencil mask with the stencil aperture at the top. Aluminum of 92 nm nominal thickness and a few angstroms of Pt for better SEM contrast were deposited on the mask. The layer thickness of the deposited metal was measured on the horizontal area of the front side of the mask as shown in Figure 17(b). The anisotropically etched (111) slopes of the Si mask that form the mask apertures are also covered by this layer causing a 67 nm horizontal broadening of the slopes which is very close to the expected amount of deposition on a Si(111) slope of 54.74°, since $92\ \text{nm}/\tan 54.74^{\circ} = 65\ \text{nm}$. Figure 17(c) and (d) show that this material build-up translates to between 19 and 22 nm of clogging from each side of the aperture. Based on this data, it can be estimated that a 92 nm deposition closes off an approximately 42 nm aperture. This means that depositions are limited in thickness to approximately 2 times the aperture opening. For 2 μm square apertures, this restricts the number of depositions, at approximately 0.1 μm/deposition, to roughly 40.

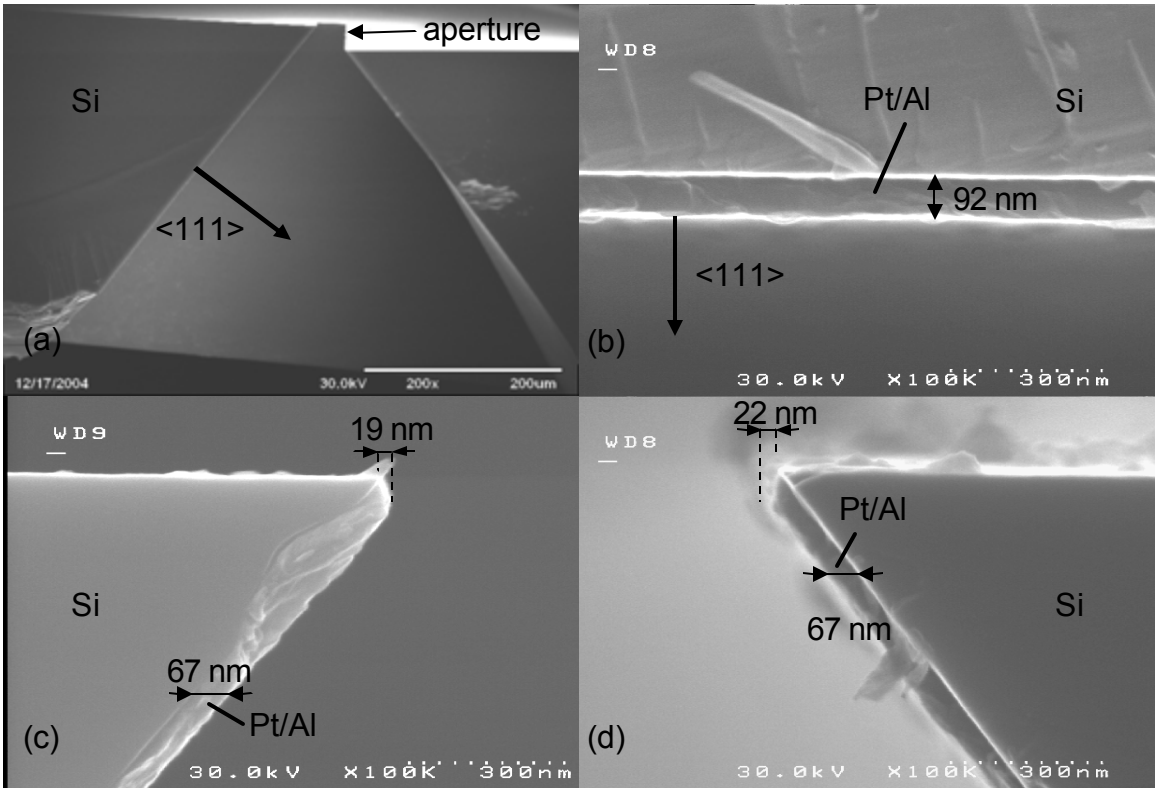

Figure 17. (a) Cross-sectional scanning electron microscope image of a KOH-etched Si stencil mask, (b) with 92 nanometer Al and a few Å Pt deposition, (c) and (d) of the mask aperture edges showing material build-up leading to aperture clogging.

Since nanometer-scale feature-formation using PEN requires knowledge about the position of the stencil mask edge, clogging affects the accuracy of this technique. However, it is relatively simple to compensate for the closing off of the stencil apertures. Provided that the clogging rate is known (e.g. approximately 1/4 for each edge of an aperture in Figure 17), it is possible to approximately compensate for the change in the position of the mask edge due to clogging by incorporating this known change into the translation coordinates for the device being constructed.

The cross-sectional SEM images also show that the apex width of the mask edges, thus the effective mask thickness, is less than approximately 10 nm.

3.7 Differential etching

As outlined in the process overview, a vital part of the PEN technique is the ability to etch the lift-off layer selectively to the device layer and the substrate. Since the lift-off layer is etched laterally starting from the feature edge, it is important to find etchants that do not attack, or only weakly etch the feature which is to remain (called the device layer). For example, a 5 nm thick device layer created by evaporation through a 2 μm stencil aperture would need to withstand the lateral undercut etching of an almost 1 μm sacrificial layer, which would require a better than 1:1000 etch selectivity. Appendix 2 lists selected chemical wet etchants for all the materials of current interest for PEN. This compilation proves helpful for selecting material systems for differential etching. It is especially useful when more than two materials are used to create nanostructures (e.g. an adhesion layer is added to the device layer).

While the bulk etch properties of materials are known, electrochemical effects may affect the etch properties of materials. The PEN apparatus provides a way to create arrays of deposits that can be used to characterize the etch properties of a number of different materials at the same time. The optical microscope image of an example for such an array created to measure the etch rates of the deposited materials in different etchants is shown in Figure 18. A sequence of depositions of 105 nm Al, 100 nm Ti, 100 nm Ge, and 100 nm Cr was executed followed by the deposition of a Cr/SiO_2 (100/20 nm) and a

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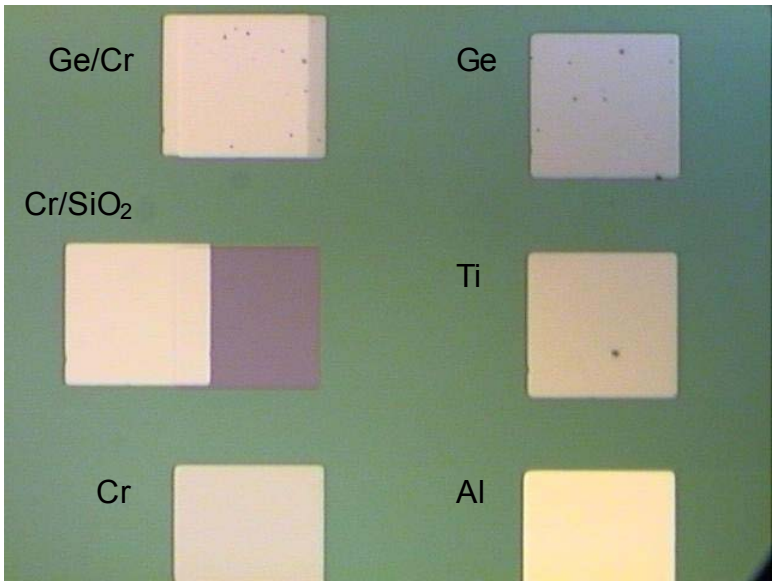

Figure 18. Optical microscope image of structures created by a sequence of Al, Ti, Ge, Cr, Cr/SiO_2, and Cr/Ge depositions.

Ge/Cr (100/20 nm) bilayer on a thermally-oxidized Si wafer. After each deposition, the substrate was translated to a pristine area.

These structures were etched in AL-12 etchant (Mix of HNO_3, H_3PO_4, CH_3COOH, and H_2O by Cyantek Corp., Fremont, CA) at room temperature and at 50 ℃ for varying times. Before and after etching, the film thicknesses were measured for each material by step-profiling. Figure 19 shows the etched layer thicknesses as a function of etch time for all materials. The slopes of the linear curve fits are the etch rates for a given material. The measurements showed that only the Al and Ge features were etched by the Al-12 etchant. The etch rates for Al are 37 nm/min at room temperature and 140 nm/min at 50 °C. For both temperatures, AL-12 does not etch Al for the first approximately 13 seconds. This is

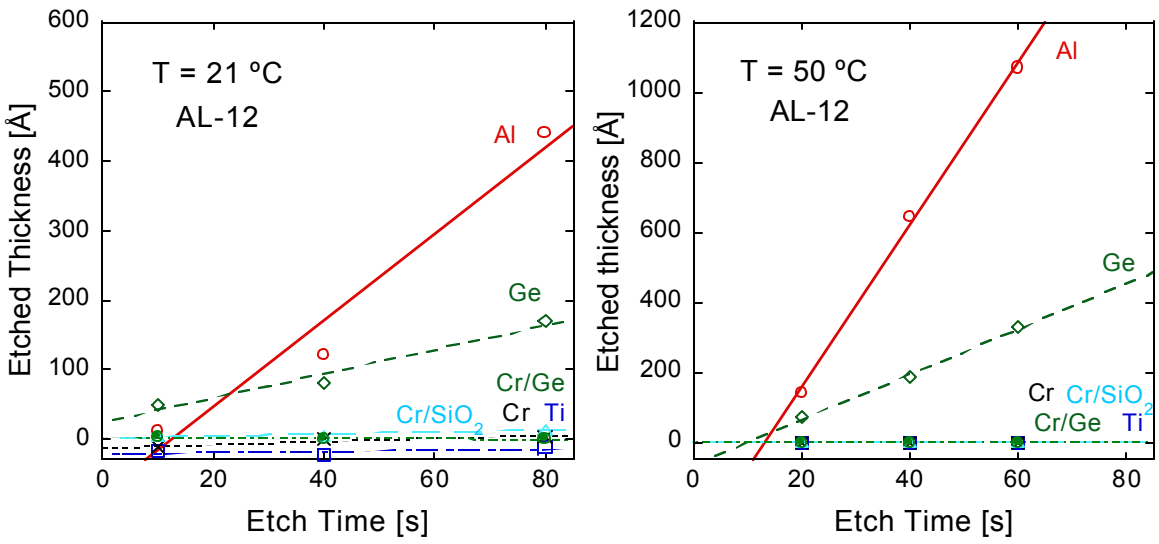

Figure 19. Etched thickness vs. etch time in AL-12 etchant at different temperatures for Al, Ti, Ge, Cr, Cr/SiO_2, and Cr/Ge features.

probably because of the presence of a native oxide layer on the Al surface. For Ge, the etch rates are 11 nm/min at room temperature and 39 nm/min at 50 °C.

After the appropriate etching solution is identified for a material system, lift-off by differential etching completes the PEN process. Figure 20 shows the results of differential etching of a Pt/Ti/Al PEN structure on SiO_2 designed to form a 200 nm Pt/Ti nanowire using Al as the sacrificial layer. After etching in hydrochloric acid, Pt/Ti deposited on the underlying Al started separating from Pt/Ti on the SiO_2 substrate, Figure 20(a). After the completion of the differential etching, all the Pt/Ti deposited on the sacrificial layer is removed leaving an approximately 400 nm wide, several microns long Pt/Ti wire, Figure 20(b).The wire shows greater irregularities along the lift-off edge

(lower edge) while the other edge is still relatively straight and smooth. This irregularity is attributed to the tearing of the top Pt layer during the lift-off process.

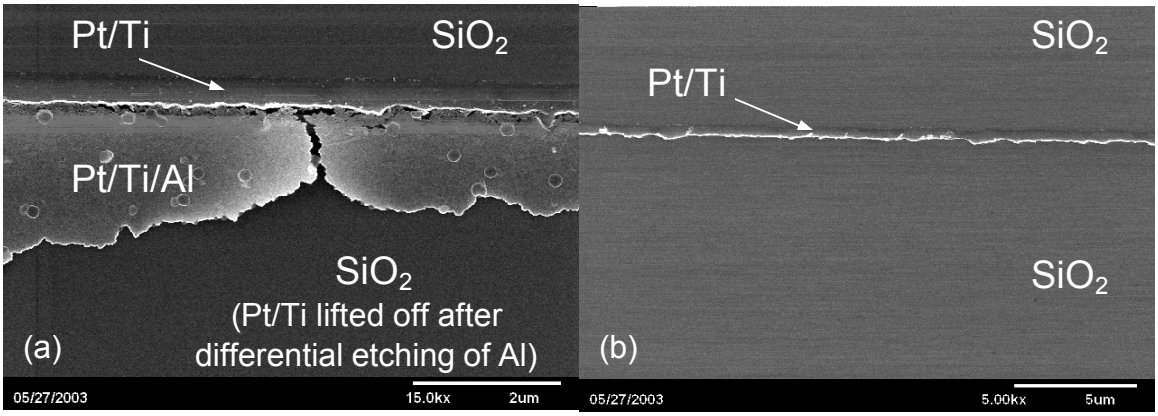

Figure 20. Scanning electron microscope images of a Pt/Ti nanostructure after (a) incomplete and (b) complete lift-off in 50 °C hydrochloric acid.

CHAPTER 4

STENCIL MASK FABRICATION USING ANISOTROPIC KOH-ETCHING

4.1 Introduction

In stencil lithography, material deposited through a stencil mask replicates the shape of the apertures, both the intended pattern and any defects. For this reason, it is essential to have a mask fabrication process which is able to produce apertures with a high degree of perfection. Submicron apertures are often fabricated by focused-ion-beam milling or a combination of electron-beam lithography and reactive-ion etching (RIE). Masks used for PEN can be microns in dimension because the feature size is defined by the lateral translation of the mask, and, as will be discussed, lateral diffusion (see Section 5), however, the edge roughness must be small with respect to the intended minimum feature size since this will be directly replicated in the deposited feature.

To achieve steep sidewalls on deposited structures with PEN, thin stencil masks are required. According to Eq.(1), with the stencil mask in contact with the deposition substrate, the edge taper due to the geometry of the system becomes zero as the stencil mask thickness goes to zero. Suspended membrane masks are on the order of one micron in thickness and can be patterned with submicron apertures, therefore, they are suitable for PEN. Another possibility is to etch a rigid mask of greater thickness anisotropically to create sloped aperture sidewalls which make the effective mask thickness nearly zero. In

the course of this research a process for anisotropic KOH-etching was developed to create stencil masks.

4.2 Anisotropic KOH-etching of silicon

Anisotropic etching of Si is widely used to create shapes bounded by crystal planes [75]. The most common etchants are KOH, ethylene diamine pyrocatechol (EDP), tetramethyl ammonium hydroxide (TMAH), and hydrazine-water (N_2H_2) [76]. The most popular etchant is the water-based KOH solution [77] because of its relative safety (EDP is toxic and O_2 must be excluded, N_2H_2 is toxic and explosive), high (100) to (111) etch selectivity, and fast etch rate of the (100) crystal plane (up to 1.4 μm/min at 85 °C) [78].

For KOH-etching of Si, if openings in the masking material (e.g. silicon nitride) are aligned to the {110} planes, the {100} planes will be etched and {111} planes will be revealed as sloped sidewalls as a result of the slower etching of Si in the [111] direction. Due to the etch resistance of the {111} planes, KOH-etched features tend to deepen as the etching proceeds but widen at a much slower rate. The ratio of the etch rates of different crystal planes is the anisotropy ratio and it can be as high as 400/200/1 for (110)/(100)/(111) in 50 wt% KOH/H_2O at 85 °C [79]. If the maximum etch rate of the {100} planes is 1.4 μm/min, from this anisotropy ratio the etch rate of the {111} planes is 7 nm/min.

Schematic diagrams of anisotropic KOH-etched features in a (100) oriented Si wafer are shown in Figure 21. Geometrical analysis shows that the width of the bottom (100)

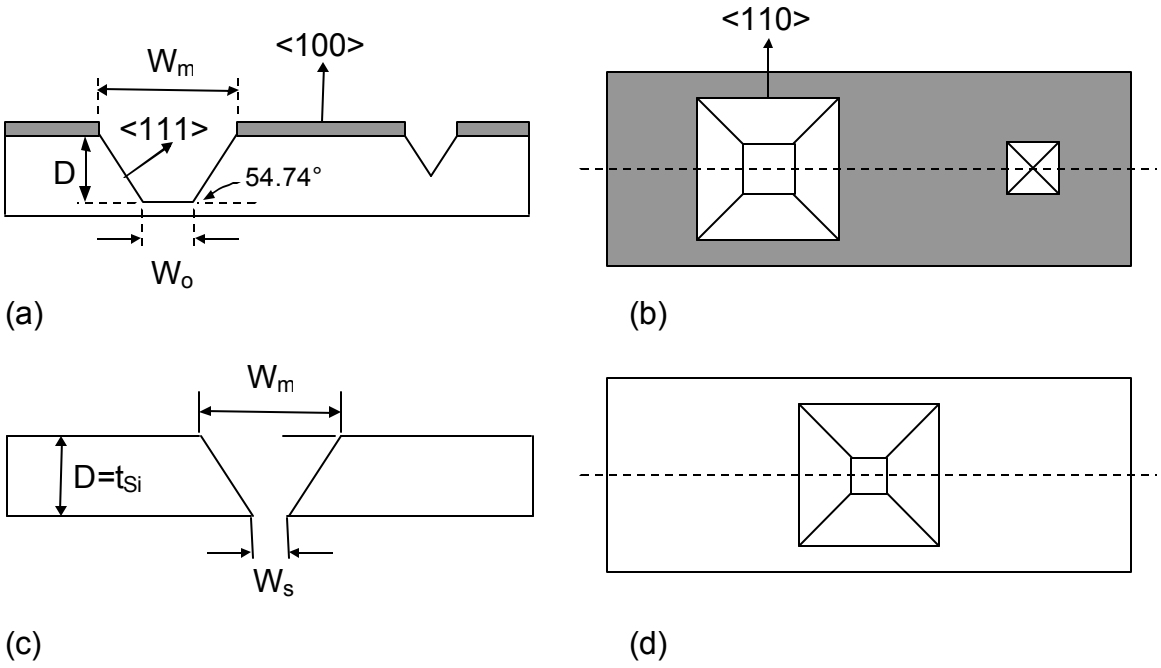

Figure 21. Schematic diagrams of anisotropically etched features in a (100) silicon wafer. (a) Silicon wafer with two KOH-etched features, adopted from [80]. Darker regions indicate Si_3N_4 mask layer. (b) Schematic top view of the same structures. (c) Silicon wafer that has been etched all the way through. (d) Top view of the structure in (c). Dashed lines in the top view diagrams indicate the view plane of the cross-sectional diagrams.

plane of the etched feature, W_o, is determined primarily by the size of the initial aperture, W_m, the etch depth, d, and the slope angle of the (111) plane relative to the (100) plane (54.74°),

$$W_0 = W_m - 2D\cot(54.74°) = W_m - \sqrt{2}D\,. \tag{9}$$

If $W_m > \sqrt{2}D$, the result of etching through a square opening in the masking layer is a truncated pyramid. If $W_m \le \sqrt{2}D$, the (100) bottom plane is etched away and the etching slows down on the {111} planes resulting in the formation of a V-shaped structure as illustrated by Figure 21(a). When etching a wafer all the way through, the etch depth is

equal to the thickness of the silicon wafer, t_{Si}, Figure 21(c). Using Eq. (9), the initial mask aperture size necessary to create a stencil aperture of given dimensions, W_s, can be calculated:

$$W_m = W_s - \sqrt{2} t_{Si} . \tag{10}$$

For example, in order to etch a 2 × 2 μm square aperture in a 350 μm thick Si wafer, the mask opening needs to be a 497 × 497 μm^2 square. This calculation assumes that the very slow etching of the {111} planes can be ignored. In reality this plane also etches with an etch rate determined by the anisotropy ratio. Also, when etching a full wafer, the thickness variation across the wafer also needs to be taken into account as the produced aperture size is directly related to the wafer thickness.

4.3 Stencil mask fabrication process

The process of making Si stencil masks using KOH-etching is outlined in Figure 22.

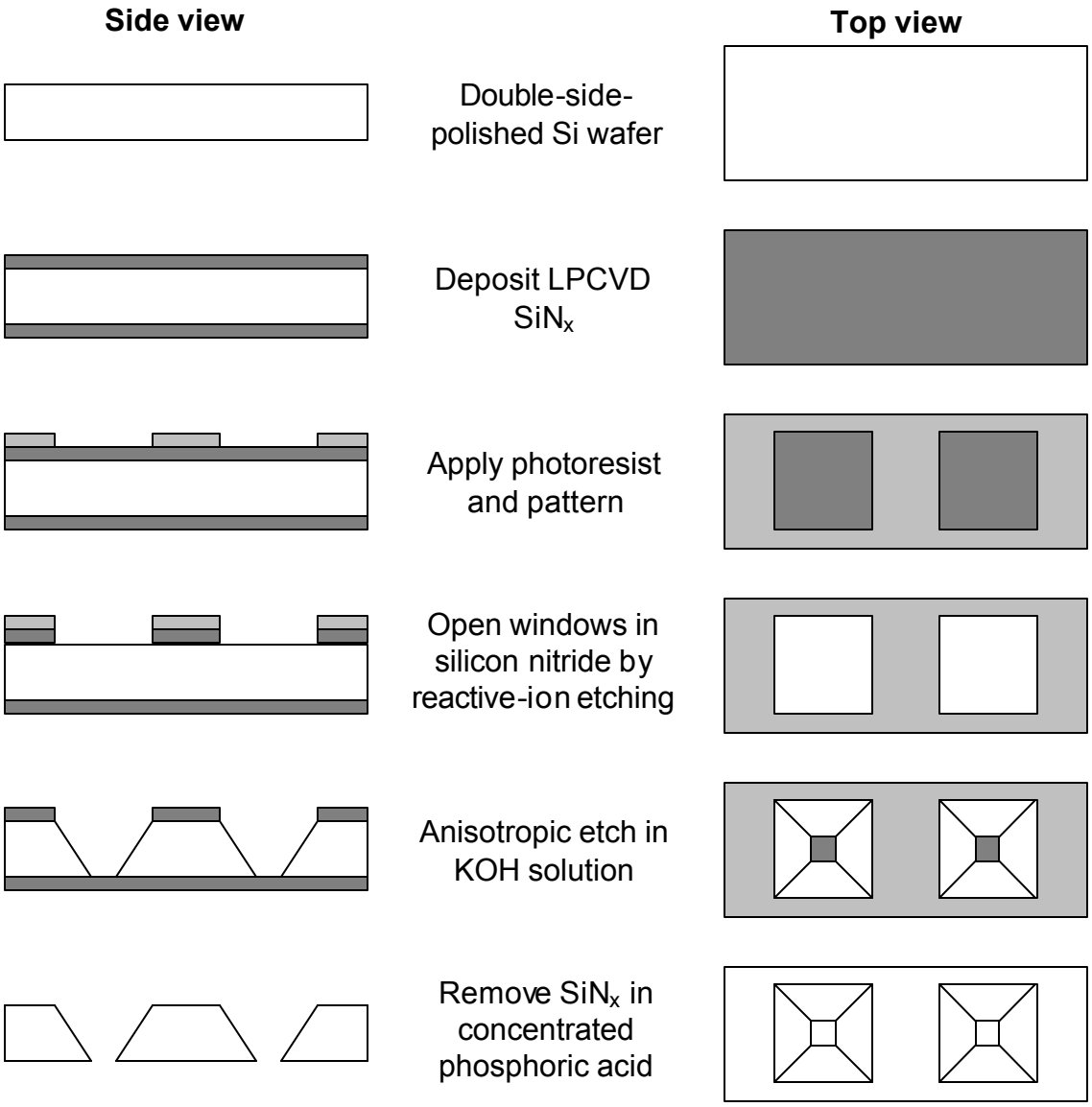

Figure 22. Process for stencil mask fabrication using anisotropic KOH-etching. The left column shows the stencil mask in cross-section during the process. The right column shows a corresponding top view. White features are silicon, light grey features are photoresist, and dark grey indicates silicon nitride. The view plane for the cross-sectional diagrams is always at the horizontal center of the structures showed in the right column.

The Si wafers used in this research are 350 ± 25 μm thick (according to the manufacturer), 100 mm in diameter, and of (100) orientation. First, the wafers are cleaned in a 70 °C $H_2O : NH_4OH : H_2O_2$ (40 – 50 : 1 : 1) bath for 10 minutes, rinsed in deionized water, then cleaned in a 70 °C $H_2O : HCl : H_2O_2$ (40 – 50 : 1 : 1) bath for 10 minutes and rinsed in deionized water. An 800 – 1200 Å SiN_x layer is deposited by low pressure chemical vapor deposition (LPCVD) to serve as the mask layer during the KOH-etch process as described in Appendix 3(a). Hexamethyldisilizane (HMDS) adhesion promoter and AZ5214 photoresist is applied to the front side of the wafers. The spinner recipe of 30 s at 4000 RPM speed created a 1.5 μm photoresist layer. Before patterning, each wafer is pre-baked for 1 minute at 90 °C. The photoresist is patterned by exposing to 160 mJ/cm^2 UV light through a chromium emulsion plate mask. After UV exposure, the wafers are developed in AZ327 photoresist developer for 45 s, followed by reactive-ion etching of the nitride in a $CF_4 + O_2$ gas mixture (26.2 sccm CF_4, 3.8 sccm O_2, 60 mTorr, 250 W) for 5 minutes. Once the openings in the silicon nitride layer are created, the photoresist is removed by rinsing in acetone and methanol for 1 minute, stripping in an oxygen plasma for 15 minutes, and then rinsing in acetone and methanol for 1 minute again. The process traveler for creating these stencil masks is attached as Appendix 4.

4.4 Silicon nitride characterization

The most common masking materials during anisotropic KOH-etching of Si include SiO_2, silicon-nitride, and Au with a Cr adhesion layer [81]. Since SiO_2 etches at a relatively fast rate, 1.4 to 3 nm/min [81], silicon nitride is preferred, because of its less

than 0.1 nm/min etch rate in KOH [81], and the relative ease of LPCVD and subsequent removal in hot phosphoric acid.

An LPCVD system (Type PXJ-100, ASM International N.V., Bilthoven, The Netherlands) was used to deposit silicon nitride using a recipe that was designed to produce an approximately 1000 Å layer on both sides of the wafers. A table showing the process settings is included in Appendix 3.

Seven 100 mm DSP wafers were loaded in the furnace in a typical deposition run. Following suggestions of other users [84], dummy Si wafers were placed in front of the first and behind the last DSP wafer to increase the thickness uniformity of the deposition. The spacing between the wafers was approximately 3 mm. In later runs it was decreased to approximately 1.5 mm to further increase the thickness uniformity. The thickness of the deposited nitride layer for a batch of seven DSP wafers was measured using a Woolam variable angle spectroscopic ellipsometer. Both sides of each wafer were measured at the center and approximately 25 mm from the center in four directions (up, down, right, and left). Figure 23 shows the measured average silicon nitride thicknesses for the whole batch (except for the first wafer which was not measured because it was already patterned by the time of the thickness characterization). The wafer numbers indicate the order of the wafers in the furnace tube, the first wafer being the closest to the front of the furnace. The direction of the gas flow during deposition is from the back of the furnace tube towards the front as indicated on Figure 23(a).

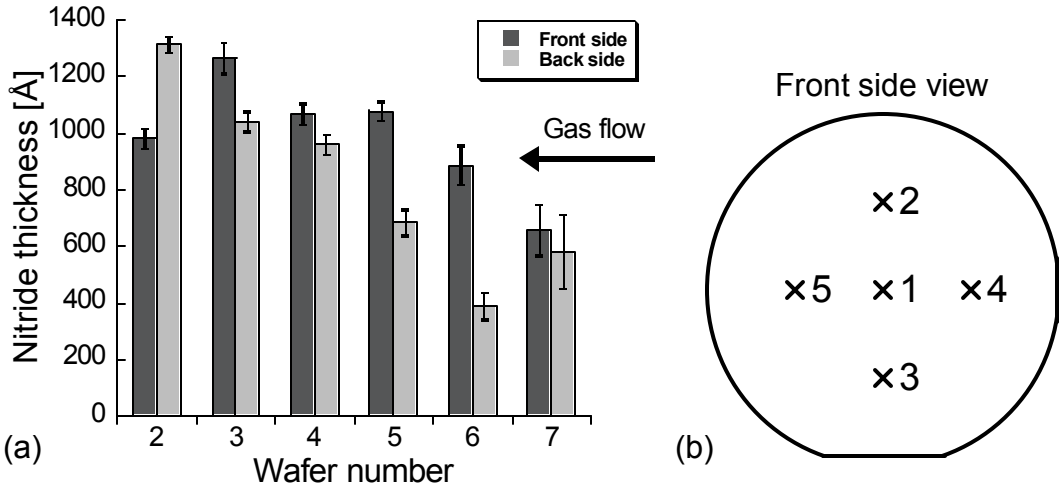

Figure 23. Thickness measurement of LPCVD silicon nitride deposited on a batch of silicon wafers using a recipe designed to produce 1000 Å silicon nitride layers on both sides of the wafers. (a) Averages of the silicon nitride thicknesses measured at 5 points on the front side (facing the furnace door) and the back side (facing the back of the furnace) of each wafer. The error bars indicate the standard deviation of the measurements. The arrow shows the direction of the process gas flow. The process produced 20% thicker layers on the front side of the wafers. (b) Location of thickness measurements.

The ellipsometer measurements show that although the average silicon nitride layer thickness is close to the target 1000 Å (988 Å on the front side and 827 Å on the back side), the thickness values vary significantly for each wafer. On each wafer, very uniform silicon nitride layers are produced on both sides (the standard deviation is typically 4% of the average thickness with a maximum of 22% for the back side of wafer 7).

Information about the maximum silicon nitride thickness is important because the reactive-ion etching process needs to be calibrated to etch through even the thickest nitride layer. After patterning by RIE and photoresist removal, the step profile of the patterns showed that 5 minutes of reactive-ion etching produces approximately 4200 Å

deep features, therefore this etch process etches all the way through the thickest silicon nitride.

During etching all the way through a Si wafer, even the thinnest silicon nitride layer must hold up against the etching solution. To determine how resistive silicon nitride is in KOH, a wafer covered with a 685 Å thick silicon nitride layer was kept in a KOH solution for 12 hours. The nitride layer was not visibly attacked which shows that the etch rate during anisotropic KOH-etching must be much less than 0.1 nm/min. Even if using this conservative estimate for the etch rate, the thinnest, 388 Å, nitride layer is expected to protect the Si wafer for at least 6.5 hours which is more than the typical time necessary to etch through a 325 μm Si wafer.

4.5 Apparatus

The anisotropic KOH-etching of the patterned Si wafers is performed using the chemical reactor shown in Figure 24. In the reaction kettle, a 7 M KOH/H_2O etch solution is prepared by dissolving 400 g of KOH pellets in enough deionized water to make 1000 ml solution. The solution is preheated to 75 – 90 °C using a stir/hot plate and 40 ml isopropanol alcohol is added as surfactant to impede bubble formation during etching [85]. The temperature of the solution is monitored by a Teflon-coated thermocouple and maintained constant under feedback control. In order to minimize etchant inhomogeneity, the solution is stirred by a Teflon-coated magnetic bar. After the etching is complete the masking silicon-nitride layer is removed in concentrated phosphoric acid in 180 °C.

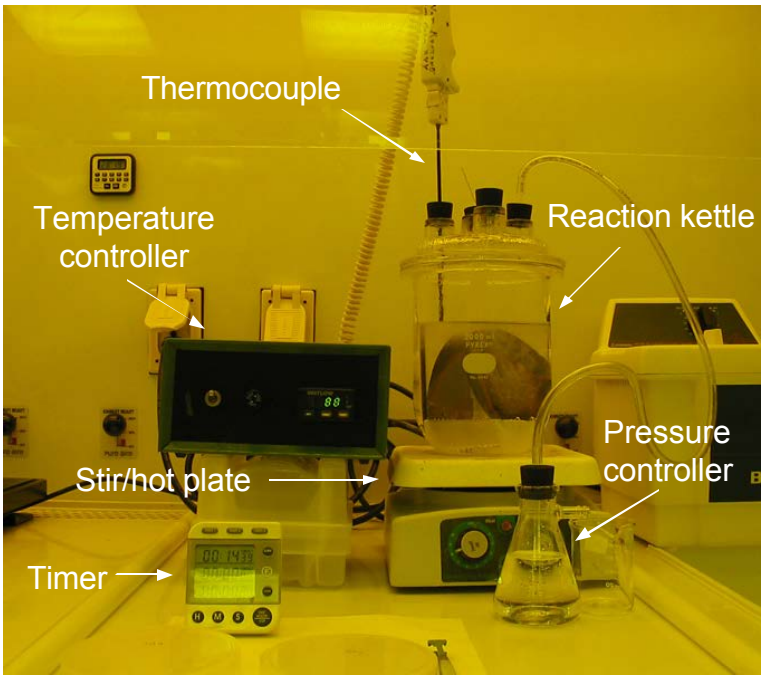

Figure 24. Photograph of the chemical reactor used for KOH-etching Si wafers.

4.6 KOH-etch process

The following general statements are valid for most aqueous KOH-etching systems. The etch rate is controlled by the reaction rate of the solution at the Si wafer, therefore, it is temperature dependent [79]. The result of increased temperature is higher etch rate for all planes and decreased surface roughness, however, the non-uniformity of the etch rate increases dramatically above 80 ℃ [77]. Increasing KOH concentration decreases surface roughness while the etch rate does not depend strongly on the concentration, therefore, highly concentrated, e.g. > 7 M, KOH solutions are preferred [77]. During etching, hydrogen bubbles develop and serve as micromasks on the surface of the wafer increasing the surface roughness. Stirring the etch solution can improve the surface quality and the uniformity of the etch by increasing hydrogen bubble detachment [77]

and by maintaining uniform concentration and temperature throughout the entire etch bath.

The KOH concentration of the etch solution was chosen to be 7 M (400 g KOH pellets dissolved in H_2O to make a 1000 ml solution). According to [82] this concentration gives 60 nm surface roughness which is close to the minimum surface roughness of 50 nm at 80 °C. Also, the etch rate non-uniformity, 0.2 %, is close to the minimum, 0.12 %, while etch rate, 1.1 μm/min, is close to the maximum, 1.2 μm/min, for an 80 °C KOH-solution. Experiments were performed with 78 – 90 °C 7M KOH solutions to optimize the etching temperature. The speed of the magnetic stir bar for each experiment was the maximum possible before it started to jolt from the bottom of the reaction kettle. Visual examination showed that high temperatures (85 – 90 °C) produce shiny surfaces and smooth aperture edges across the entire wafer, but the non-uniformity of the etch rate is significant as can be seen from the fact that some areas the wafer etch through while in other areas the apertures are incompletely etched. Ultimately, the effect of this non-uniformity is an array of apertures across the wafers that vary in size from one edge of the wafer to the other. Lower temperatures (below 80 °C) produce apertures of uniform sizes, however, surface roughness increases as indicated visually by the matte surface of the apertures which is a result of (111) planes being revealed. As a result of increased roughness, many apertures do not open up completely at the end of the etch. Figure 25 shows a mask aperture created with anisotropic KOH-etching at (a) 85 °C and at (b) 78 °C. The sidewalls in Figure 25(a) are apparently smooth and the opening is a perfect square. On the other hand, Figure 25(b) shows more roughness on the slopes and the opening is blocked by a piece of silicon.

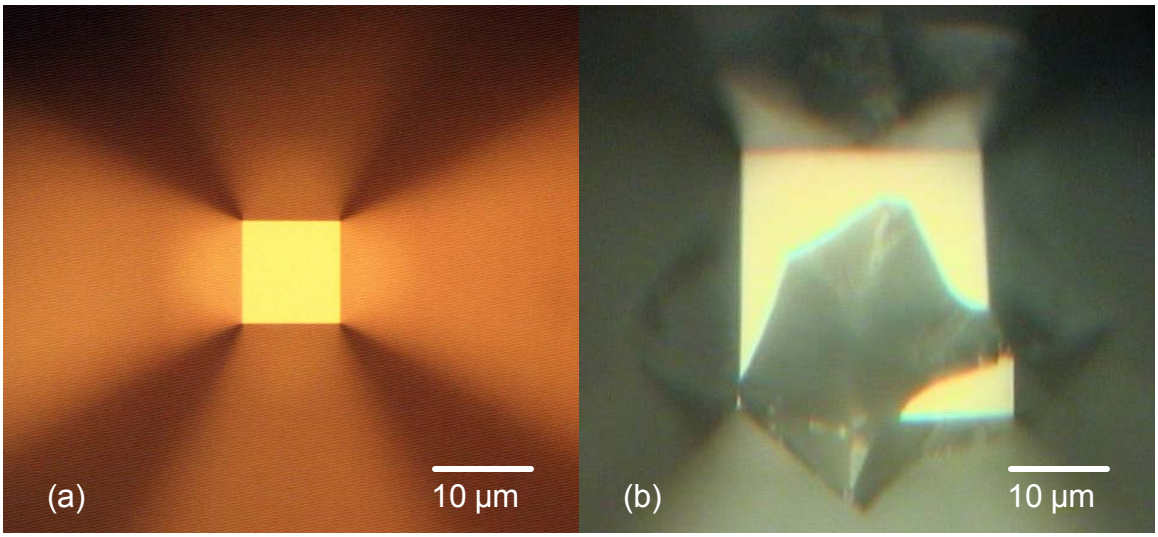

Figure 25. Silicon stencil mask apertures fabricated using anisotropic KOH-etching at (a) 85 °C, and (b) 78 °C.

This kind of blockage is observed on many apertures formed by KOH-etching below 80 °C. The formation of these structures bound by high-index crystal planes may be a result of the increased surface roughness associated with decreased temperature [79] or possibly, due to slower hydrogen bubble detachment, higher index planes are revealed in the course of the etching. These high index planes have much higher etch resistance, therefore, structures defined by these planes grow gradually as the (100) plane is etched around them.

Based on KOH-etching at temperatures of 78, 80, 82, 85, and 90 °C, a temperature of 82 °C produced the best looking surfaces with the least blocking of apertures by Si pieces. The dimension variation of the apertures at 82 °C was greater than at for 78 °C as a result of increased etch non-uniformity, ±17 and ±10 µm, respectively.

The etch rate and etch selectivity for the anisotropic KOH-etching can be determined from measuring the structures created during etching. A schematic drawing of the result

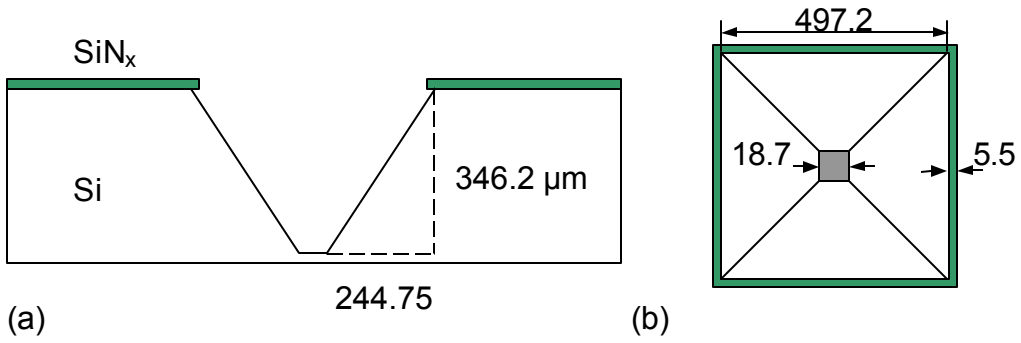

Figure 26. Schematic cross-sectional and top view diagrams showing the result of a 355 minutes long KOH-etching of a silicon wafer after opening a square shaped pattern in the silicon-nitride masking layer. The measurements shown are used to determine the etch rate and the etch selectivity. The dimensions (in microns) of the gray regions in (b) were obtained from optical microscope measurements.

of etching a Si wafer through a square mask opening in an 80 °C KOH solution for 355 minutes is shown in Figure 26.

The size of the window opened in the Si masking layer, the extent of the undercut under the silicon-nitride layer and the size of the bottom feature was measured using an optical microscope. Since the angle of the slope is 54.74°, the depth of the etch can be calculated:

$$D = \frac{\left(497.2 \pm 0.2 + 2 \times 5.5 \pm 0.2\right) - 18.7 \pm 0.2}{2} \times \tan 54.74^{\circ} = 346.1 \pm 0.6\ \mu\text{m} \qquad (11)$$

While approximately 346.1 µm was etched in the direction normal to the (100) plane in 355 minutes, the etching progressed approximately 4.5 µm normal to the (111) plane ($5.5\ \mu\text{m} \times \sin 54.74^{\circ}$). Thus, the calculated etch rate for the (100) plane is approximately

0.98 μm/min and the etch selectivity between the (100) and the (111) planes is approximately 77:1. These numbers are in good agreement with results reported by Shikida et al. who measured 1 μm/min etch rate of the (100) plane in an 80 °C 34 wt% (8.2 M) KOH solution and the anisotropy ratio of the (100)/(111) planes calculated using the reported data is approximately 71:1 [83].

4.7 Stencil mask results

In order to accurately measure the sizes and edge sharpness of the stencil apertures, Si masks fabricated by KOH-etching were examined using SEM. In early experiments only small pieces of a 4" wafer containing 15 different size apertures were used for PEN, therefore, etch uniformity across the wafer was not a concern. For this reason, high etch solution temperatures, providing smooth edges, were used.

A Si wafer was etched in 90 °C 34 wt% (8.2 M) KOH solution after the silicon nitride masking layer was patterned using a chromium plate mask that had rectangular openings with widths varying from 455 to 525 μm in 5 μm increments and lengths of 1 mm. This pattern of 15 openings is designed to produce 7 stencil apertures with widths ranging from 0 to 30 μm in 5 μm increments in a 350 ± 25 μm thick wafer. Scanning electron microscope images of the apertures formed by the KOH-etch are shown in Figure 27. The widest, 525 μm, rectangular mask opening produced a 26.5 μm wide aperture on the back side of the wafer, Figure 27(a). The 520, 515, and 510 μm openings were also wide enough to produce apertures on the back side. The corresponding aperture widths are 20.5, 15.0, and 7.2 μm, Figure 27(b), (c), and (d), respectively. The 505 μm and smaller

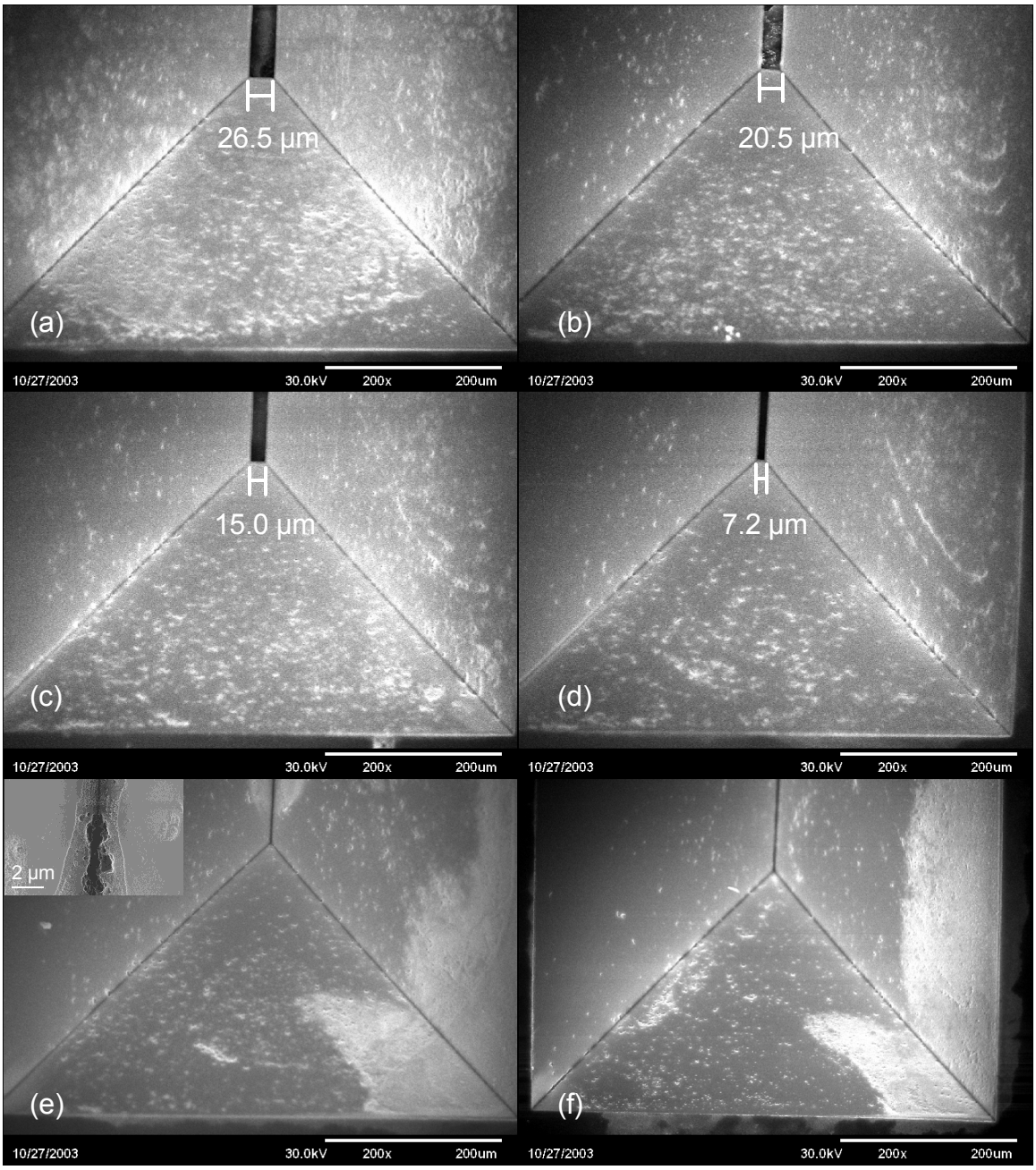

Figure 27. Scanning electron microscope images of apertures formed by a 90 °C anisotropic KOH-etch process in a Si wafer. (a) – (d) Apertures were formed through rectangular patterns with widths of (a) 525, (b) 520, (c) 515, and (d) 510 µm. (e) Etching through a 505 µm wide pattern did not produce an aperture with smooth sidewalls, however, at points along the trench, irregularly shaped apertures appeared (inset). (f) Etching through a 455 µm opening also did not produce an aperture.

openings were too narrow to allow the formation of apertures. Figure 27(e) and (f) show the structures created by the 505 μm and the 455 μm wide openings, respectively.

In combination with the PEN technique, these rectangular openings were used to produce several hundred micron long metallic lines which result was published in the Journal of Vacuum Science and Technology in 2004 in a paper entitled Nanofabrication using nanotranslated stencil masks and lift off [60].

For the purpose of creating device arrays and material libraries, a mask pattern was designed to produce uniform sub-5 μm apertures to maximize the number of devices that could be formed in a single evaporation sequence and to allow development of devices. Figure 28 shows SEM images of a 3.5 μm square aperture formed by anisotropic etching in a 7 M KOH solution for 5 hours at 82 ℃.

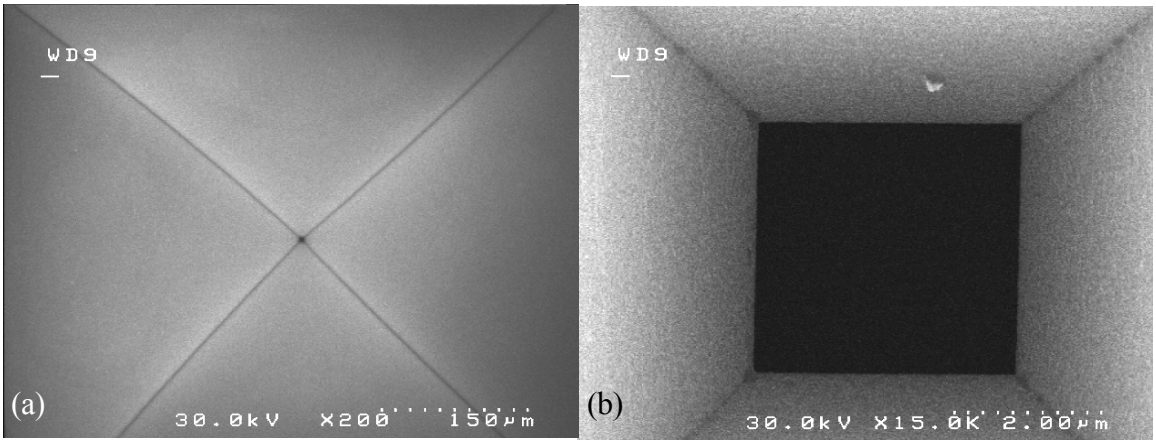

Figure 28. Scanning electron microscope images of an aperture formed in a silicon wafer by anisotropic KOH-etching for 5 hours. (a) Low magnification scanning electron microscope image of the same aperture shows that the aperture is an approximately 3.5 μm square with uniform edges.

The KOH-etch produced visibly smooth sidewalls as can be seen in the low magnification SEM image of the inverted pyramid shaped etch feature, Figure 28(a). The higher magnification SEM image of the same aperture, Figure 28(b), shows uniform edge features and a square shape.

The uniformity of the aperture edges is an important attribute since the aperture is replicated in the depositions. High resolution SEM images of the edges of apertures formed at different KOH-etch temperatures are shown in Figure 29. Taken on the same scale the edges and (111) surfaces show some differences in edge and surface roughness. The sidewall of the 90 ℃ KOH-etched aperture, shown in Figure 29(a), is smoother than the 82 °C KOH-etched, Figure 29(b), which may be the result of the higher etch temperature.

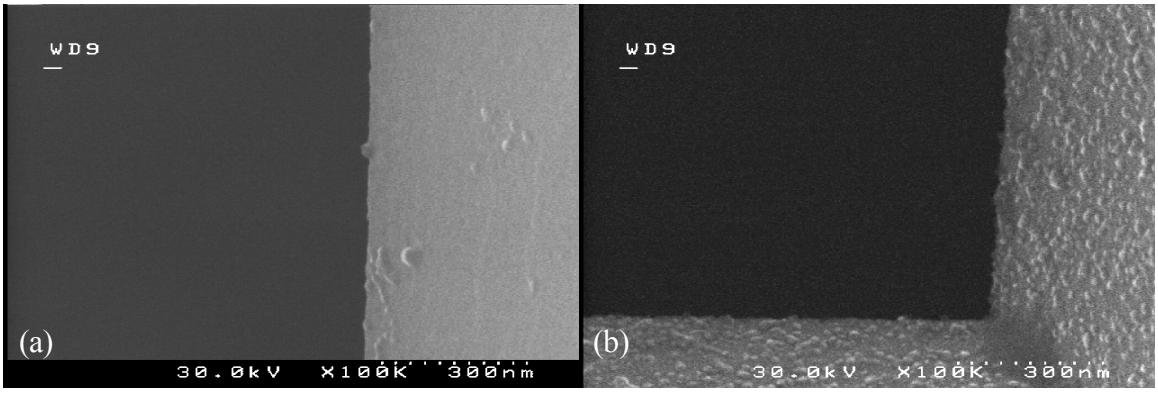

Figure 29. High resolution scanning electron microscope images of the edge of a rectangular aperture (a) and a square aperture (b). Both aperture edges are very uniform with irregularities smaller than 30 nm.

CHAPTER 5

LATERAL DIFFUSION DURING DEPOSITION

5.1 Introduction

Features formed by evaporation through stencil masks have an edge taper which is controlled by the deposition geometry and by the reduction in the aperture size during deposition, Sections 3.2 and 3.6. The deposition of 92 nm Al through a Si stencil aperture at room temperature produced features with edge taper on the order of 500 nm with an approximately 10° sidewall slope as seen in the cross-sectional SEM images of the left and right edge profiles, Figure 30. The expected edge taper due to the combined effect of shadowing and clogging is less than 30 nanometers resulting in an approximately 72° sidewall slope.

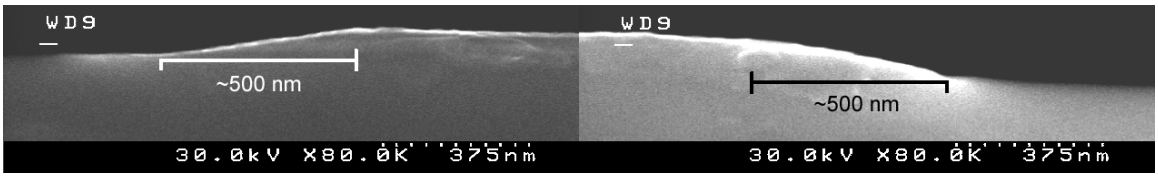

Figure 30. Composite cross-sectional scanning electron microscope images of the left and right edges of a 92 nm thick Al feature created by PEN.

The possible reasons for this unexpectedly large edge taper include thermal drifting of the mask during deposition, wicking of the Al between the substrate and the mask due to capillary forces, and lateral diffusion. Thermal drifting would produce different edge tapers at the two sides of the deposited feature, and since both edges show similar slopes, thermal drifting can be ruled out. As a result of wicking, material would be pulled in between the mask and the substrate producing material build-up on the mask which has not been observed in optical microscope and SEM images of the mask. Also, the sloped edges of the deposit would not be formed if the material motion were due to capillary forces by the mask. For these reasons, lateral diffusion was proposed as the most likely reason for lateral material spreading

Since lateral spreading of material under the stencil mask determines the profile of the edge taper, experiments were designed to allow the characterization of the edges as a function of deposited material, layer thickness, and deposition rate. Using the PEN apparatus materials were deposited on the same surface, in the same pumpdown, and through the same aperture. A comparative study was performed on thermally-oxidized Si surfaces. As will be shown, this lateral spreading is driven by at least two mechanisms: a concentration-dependent diffusion process which governs the translation of the half-height of the deposited film, and a surface diffusion process which feeds the growth of a thin surface layer under the stencil mask. The lateral surface diffusion is then shown to be suppressed by evaporation in oxygen and nitrogen background pressures.

Near room temperature surface diffusion during evaporation through stencil apertures has been previously reported for several materials and substrates: Er and Au on oxidized Al and Si [14], Sb and Si on Si (111) [59], Al on Si, SiO_2, and Si_3N_4 [86], and Au on

SiO_2 [30]. However, a comparative study of the lateral spreading of a set of different materials on the same substrate during a single electron-beam deposition has not been previously performed. Atomic force microscopy (AFM) and scanning electron microscopy (SEM) are used to characterize the deposition profiles.

5.2 Experiment

Silicon (100) substrates, 100 mm in diameter, were thermally oxidized at 1000 °C for 360 minutes to grow an oxide with a thickness of approximately 1 μm. A sequence of depositions of Al, Ti, Pt, Au, Cr, and Ge was executed through a KOH-etched Si mask with micron scale apertures. Between depositions, the stencil mask was translated to a pristine area of the substrate by the piezoflexure stage. During the experiment the apparatus was shielded from the radiative heat of the deposition sources and the mask holder was kept at a constant temperature (45 ºC) by a closed-loop temperature controller driving a 1 kW quartz lamp.

The evaporations were performed under vacuum at 1.8×10^{-6} Torr with deposition rates in the range of 2 – 8 Å/s. Aluminum was also evaporated at a high deposition rate (HDR) to see how the deposition rate affects the lateral spread. Figure 31 shows SEM images of the 21 depositions through two different apertures, a 3 μm square aperture in Figure 31(a) and a 7 μm star aperture in Figure 31(b). The star-shaped apertures form occasionally at lower KOH bath temperatures (78 °C); because of the sharp angles, the difference between the lateral diffusion of different materials is amplified in the star patterns.

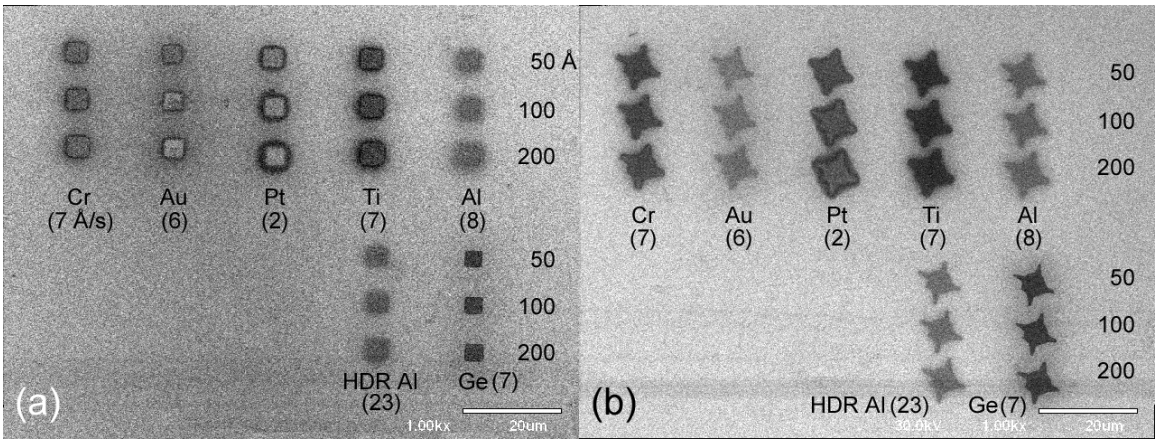

Figure 31. Scanning electron micrographs of a sequence of depositions through the same stencil aperture which is translated between depositions: (a) approximately 3×3 μm^2 squares, (b) approximately 7 μm length star features. These two aperture openings were present on the same stencil mask. Deposition rates are given for each feature and for each material and three different deposition thicknesses were made as labeled on the right hand side of the micrograph. HDR means high deposition rate.

For each material, three layer thicknesses were deposited, nominally 50, 100, and 200 Å. The substrate was translated between each elemental deposition by 9 μm in the vertical direction in Figure 31. After each deposition sequence (three depositions of the same material), the substrate was translated by 18 μm in the horizontal direction and the deposition sequence was repeated with a different element. The order of the evaporations was from right to left by material and from thin to thick depositions. The nominal thicknesses and deposition rates for each material are also indicated in Figure 31.

5.3 Analysis and discussion

The scanning electron micrographs of Figure 31 show that the size and sharpness of the deposited materials vary significantly even though they were all deposited through the same apertures. This is especially apparent for the star structures of Figure 31(b) where

the Pt and Ti features are notably larger and less distinct (blurrier) than the Ge features. Examination of the thickness dependence for the same element shows that the lateral dimensions increase with increasing layer thicknesses.

Atomic force microscopy images of the deposited layers were obtained using a Digital Instruments MultiMode Scanning Probe Microscope with a NanoScope IV controller in tapping AFM mode with a resolution of ≤ 20 nm. Each of the images in Figure 32 shows a central bright square formed under the approximately 3 μm aperture. With the exception of germanium, each square is surrounded by a 'halo' consisting of materials which spread out on the surface in a thin surface layer. The extent of this lateral zone is different for each metal and varies with deposition thickness. For Au, Al, and Pt, nanocrystalline features are clearly observed; for Au these are dispersed about the central deposition square, while for Al the crystal formation begins about a micron from the deposition edge.

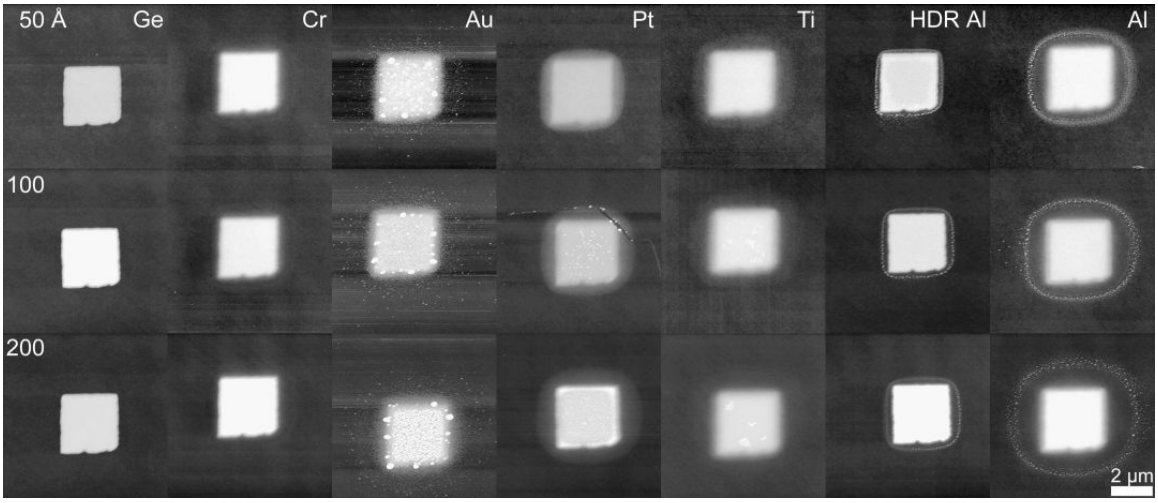

Figure 32. Top-view atomic force microscope images of the deposited materials of Figure 31. These images show that the blurry feature edges observed in the scanning electron micrographs are the results of lateral particle diffusion during deposition.

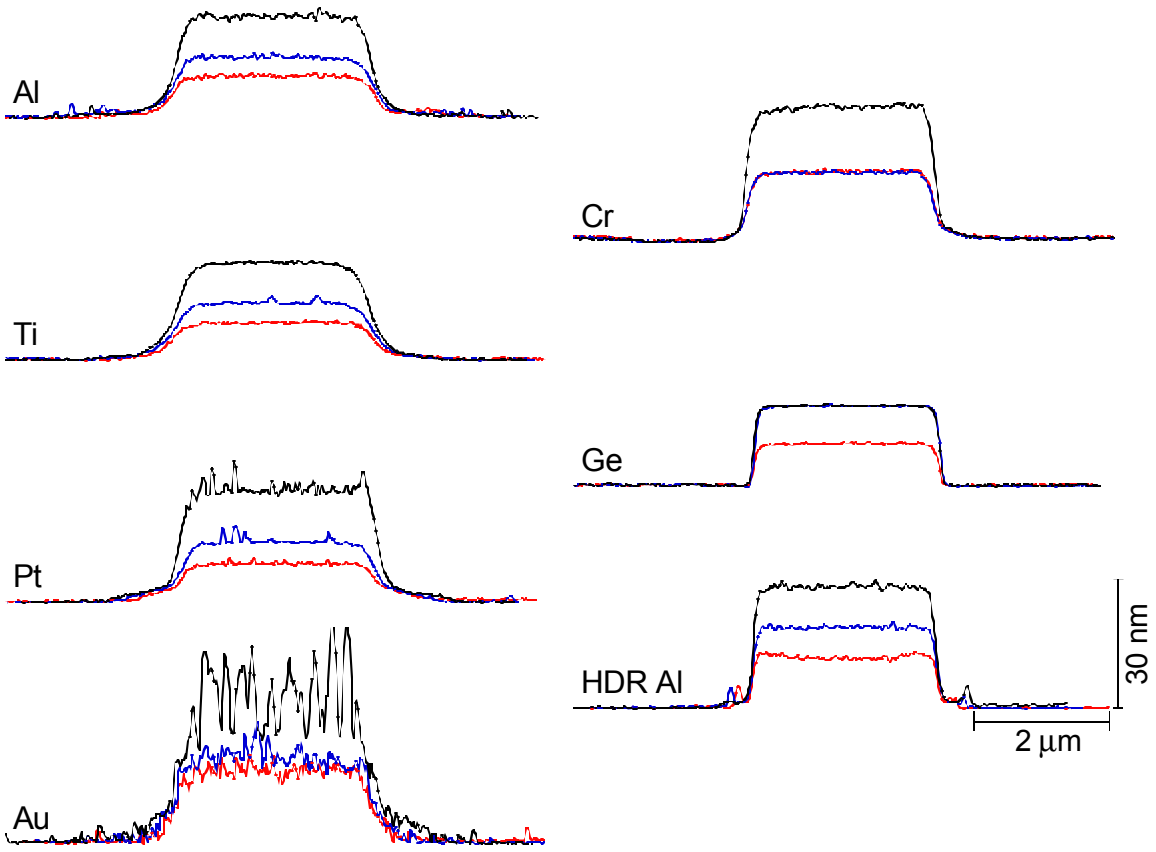

Figure 33. Cross-sectional atomic force microscope linescans of the deposited structures grouped by element. It can be seen that changes in layer thickness change the extent of lateral diffusion.

The lateral dimensions are compared by overlaying linescans from the AFM images, Figure 33. The Au and Al microcrystal formations apparent in the AFM micrographs of Figure 32 are also apparent in the linescans. The three nominal deposition thicknesses of 50, 100, and 200 Å are overlaid for each element from which the actual thicknesses can be measured. These cross sections show that as the layer thickness increases, with the exception of Ge, the lateral dimensions increase as well.

Figure 34 compares the linescans of all the elements at the nominally 100 Å thick deposition thickness. It is apparent that materials that produced a blurry SEM edge (Al, Ti, and Pt) have tapering sidewalls, while materials with well-defined SEM edges (Ge and HDR Al) have apparently abrupt sidewalls. The apparent abruptness of the sidewall is greatly exaggerated in Figure 34, as the scale of the *y*-axis is expanded by more than 100× relative to the *x*-axis. The actual angles of the edge taper are all small, TABLE 3, less than 10°, where 90° would be an abrupt, perpendicular edge.

TABLE 3

MEASURED ANGLE OF THE EDGE TAPER FOR NOMINALLY 10 NM THICK DEPOSITIONS ON SiO_2 AT 45 °C, FROM THE AFM LINESCANS OF FIGURE 34

	Edge taper angle (°)		Deposition Rate (Å/s)
	Left	Right	
Al	1.6	1.6	8
Ti	1.8	1.7	7
Pt	1.4	1.7	2
Au	2.8	2.5	6
Cr	3.8	3.4	7
Ge	9.0	8.5	7
HDR Al	8.3	8.4	23

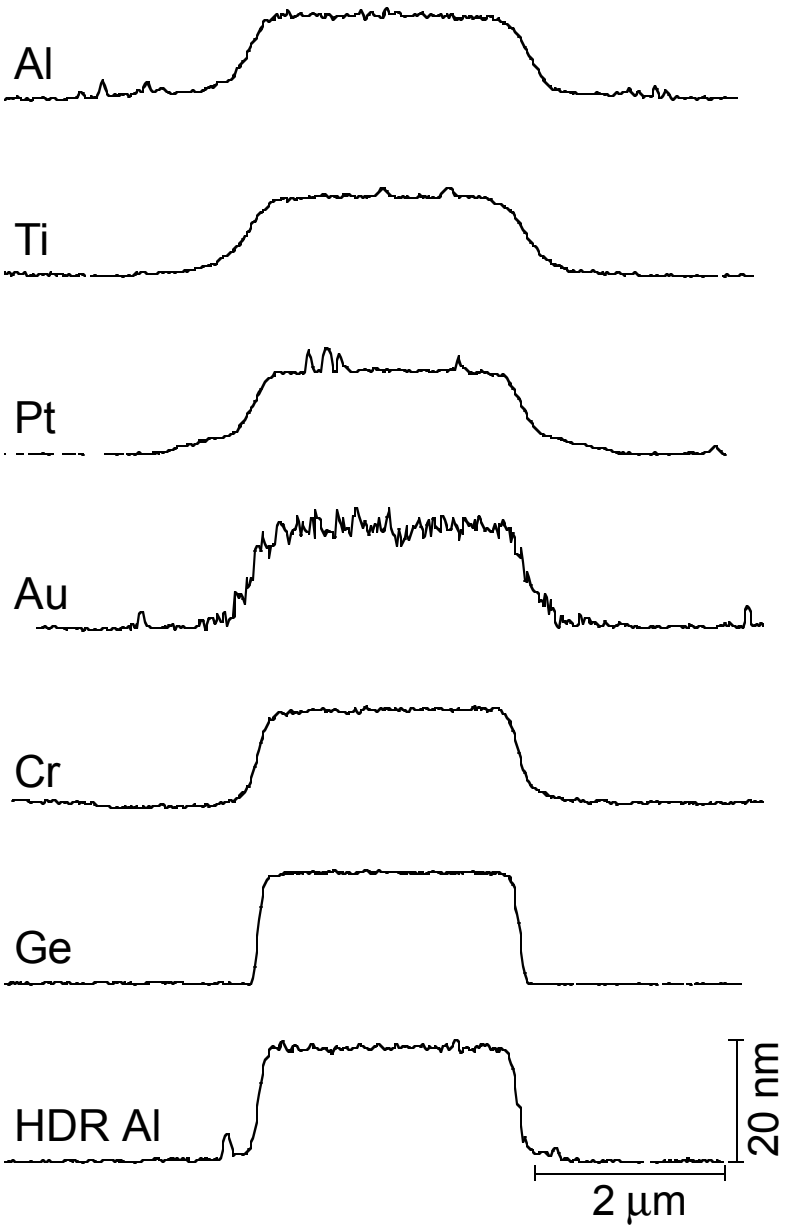

Figure 34. Cross-sectional atomic force microscope linescans of depositions with 100 Å nominal layer thickness. The varying extent of lateral diffusion of different materials is apparent.

By determining the aperture size, the lateral spreading of all elements relative to the same stencil aperture can be directly measured. The principle of mass conservation is used to determine the deposition edge and estimate the aperture size [59]. According to the SEM images, Ge is the least-diffusive element, therefore, the cross-sectional AFM image of the nominally 100 Å thick Ge feature was used to estimate the aperture size, Figure 35.

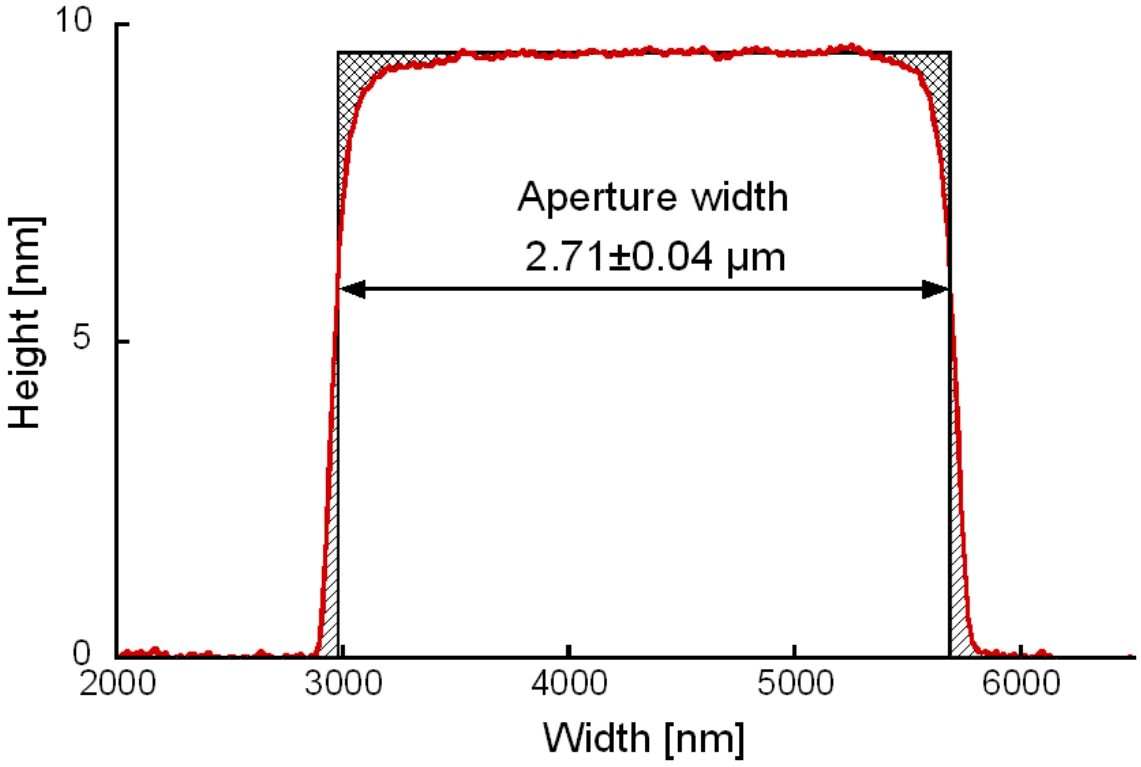

Figure 35. Cross-sectional atomic microscope image of a 95 Å germanium deposit used to determine the size of the stencil mask aperture. The initial interfaces are positioned on both sides of the feature to make the cross-hatched area equal to the hatched area.

The amount of Ge that moved under the stencil mask (hatched area) is set to be equal to the amount of material missing from the region of deposition (cross-hatched area) [87]. The equal mass point defines the aperture edge and the size of the stencil mask aperture is then measured between the two equal mass interfaces. As indicated in Figure 35, the aperture size for the nominally 100 Å Ge deposition is approximately 2.71 μm. Because clogging of the aperture can be expected, a clogging factor of $1/4^{th}$ of the deposition thickness times 2, for the two edges, is used to correct the aperture size for each deposition. This factor of $1/4^{th}$ was measured for Al from cross-sectional SEM measurements of the masks, and this factor was applied to all elements in this study. The total correction is small; for example, during the Al, Ti, Pt, Au, and Cr depositions, the aperture size is decreased by only 0.06 μm.

To quantify the lateral diffusion length for a given deposition, the difference between the full-width-at-half-maximum of the deposited feature and the mask aperture size is computed. This diffusion length is extracted for each structure and plotted as a function of the square root of time in Figure 36.

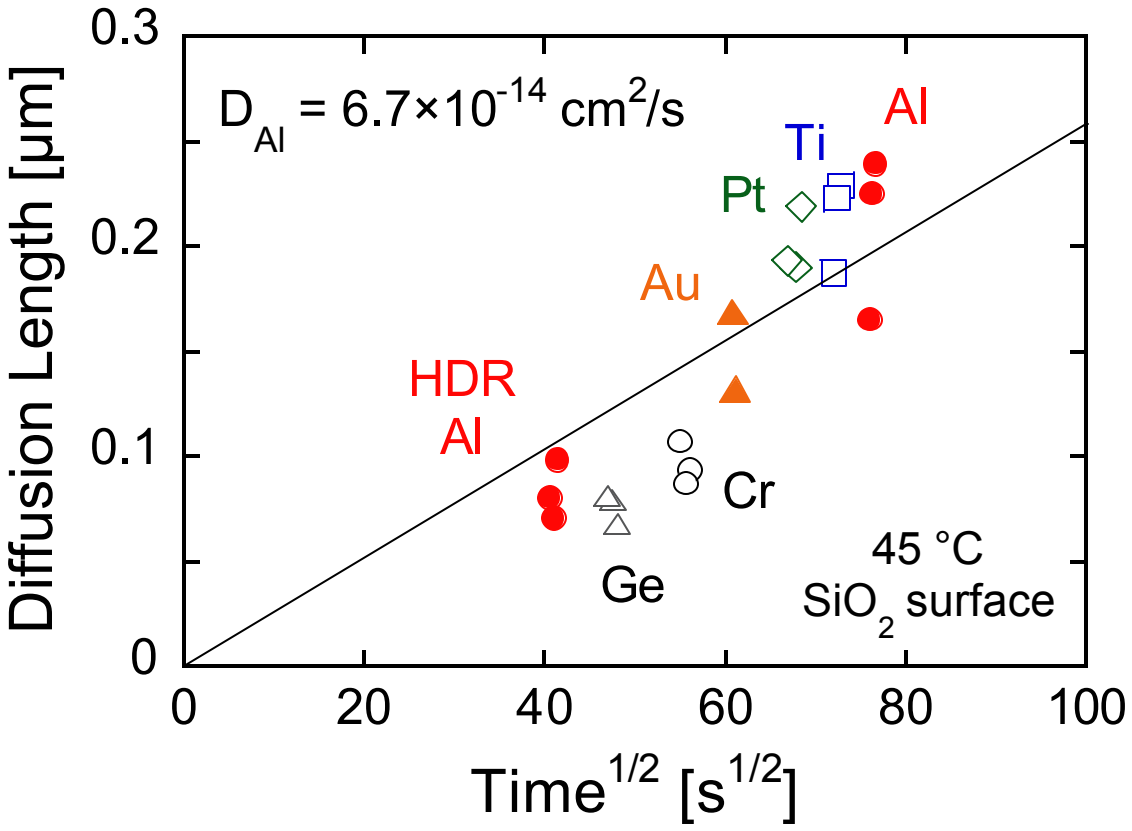

Figure 36. Lateral diffusion length vs. square root of the annealing time and vs. deposited element in vacuum on SiO_2 at 45 °C.

Elements that were deposited first had the longest diffusion time and elements deposited last received the shortest diffusion. The order of depositions can be read from right to left. The diffusion length shows an approximately linear dependence on the square root of time as expected for Fick's law diffusion and this diffusion appears to be roughly independent of the element. Since two Al deposition sequences were performed, the diffusion coefficient of Al on SiO_2, D_{Al}, can be estimated from $L = \sqrt{D_{Al} t}$, where t is the diffusion time. The line fitted to the Al data points is shown in Figure 36 with the

corresponding diffusion coefficient of 6.7×10^{-14} cm^2/s. A linear fit using all data points gives a diffusion coefficient that is only 5% less than D_{Al}. Reported values for D_{Al} for surface diffusion at similar temperatures vary from 6.4×10^{-15} cm^2/s [88] and 7.2×10^{-12} cm^2/s at 45 °C [92] in good agreement with this result. Also of note in Figure 36 is that for each element three different thicknesses were deposited giving rise to the three points per element shown. A difference between diffusion length and thickness of the deposition can be seen which is not explained by Fick's law diffusion. This dependence of lateral spread on deposited layer thickness but not on time is evidence of a second diffusion mechanism.

The existence of a thickness dependent diffusion mechanism is also evident in Figure 32, where the halo extent increases with increasing film thickness although the time between each deposition of the same material was approximately 1 minute. This conclusion is further supported by the observation that in an experiment where 5 sets of Al structures of varying thickness (50, 100, and 200 Å) were deposited in a similar manner to the one described in Section 5.2, deposits of the same thickness produced qualitatively the same halo extents.

This second mechanism is consistent with the following model. First, the sticking probability of the impinging molecules is assumed to be unity, since near room temperature desorption is negligible [89]. Second, adatoms reaching the oxide surface are in a mobile, weakly adsorbed phase [90, 91, 92], with the first monolayer of atoms becoming immobilized by bonding with the oxide surface. Adatoms landing on this first monolayer remain in the mobile state and diffuse to an energetically favorable step edge, increasing the lateral size of the layer, or contribute to the thickening of the film by

forming new stable islands after colliding with other atoms. Adatoms landing close to the aperture edge have a higher probability of diffusing into the shadow region, and since this region does not receive impingement flux, adatoms are less likely to be immobilized by other atoms. Thicker depositions provide more adatoms for diffusion under the mask and produce larger halos.

The halo extent is defined as the difference between the geometrical deposition edge and the maximum observable edge of the halo from the top view AFM images in Figure 32.

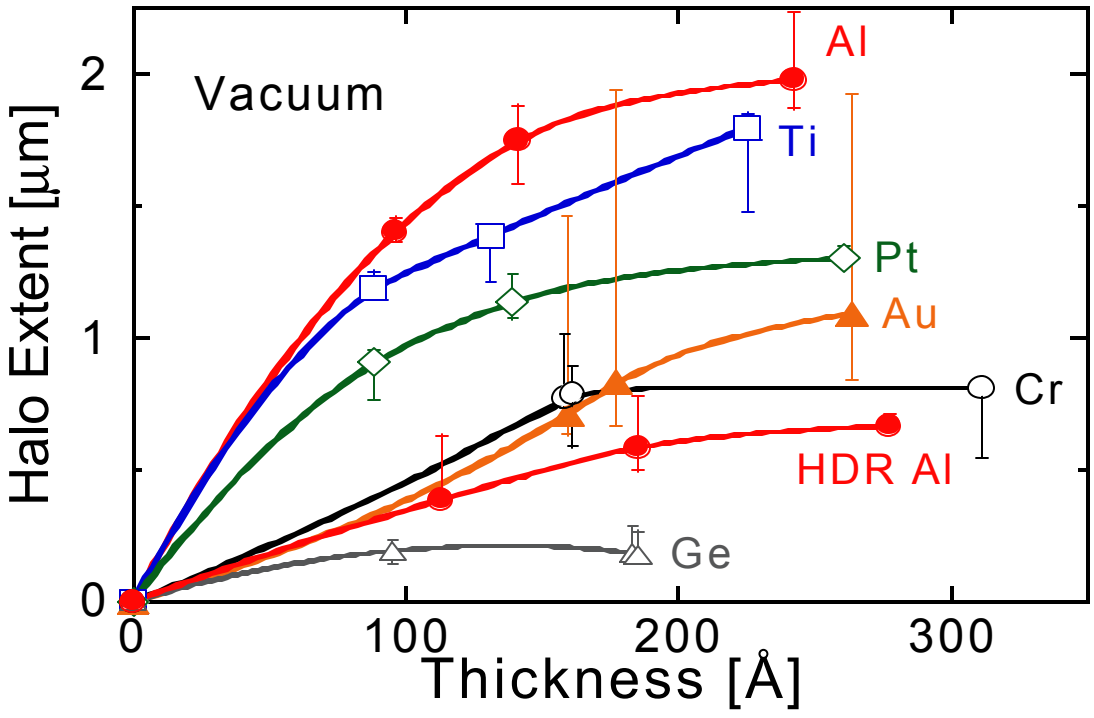

Figure 37. Halo extent (distance from deposition edge to edge of halo) vs. deposition thickness for materials deposited on SiO_2 at 45 °C: in vacuum at 1.8×10^{-6} Torr. Germanium has the smallest lateral diffusion length, while Al, Ti, and Pt can diffuse over hundreds of nanometers.

Shown in Figure 37 is a comparison of the halo extent vs. the deposition thickness for each deposited film. The error bars represents the uncertainty in selecting the edges. This uncertainty varies for each deposition and depends both on the element and on the quality of the image. The lower error bar indicates the minimum possible dimension, the upper error bar, the maximum dimension, and the data symbols, the most likely edge positions. The halo extent correlates both with deposition thickness and with the time at 45 °C. With the exception of the HDR Al, the longer the time, the greater the halo extent. Increasing the Al deposition rate by approximately 3× in the HDR Al deposition decreases the extent of the halo by approximately 4×. This is consistent with the idea that higher deposition fluxes lower the surface mobility, enhance the nucleation of islands, and provide fewer adatoms to the regions shadowed by the stencil mask. The greatest halo extent is seen for Ti, Al, Pt, and Au, Figure 37 which all spread out over one micron. The halo for Ge is significantly less, but still can exceed 0.1 μm. There appears to be a saturating trend to the halo extent which is consistent with the idea that the edge growth rate decreases as the edge moves away from the aperture opening.

5.4 Evaporation in oxygen and nitrogen ambients

Diffusion can be suppressed by lowering the substrate temperature. Deshmukh et al. [14] reported that vacuum deposition onto a substrate cooled to liquid nitrogen temperature decreased the spreading of Er dots on SiO_2 by a factor of 2 compared to room-temperature. Surface diffusion can also be suppressed by deposition in a mobility-inhibiting gas ambient [93 – 95]. Oxygen pressures of 10^{-4} - 10^{-5} Torr decrease the mobility of deposited atoms [93] by either forming an oxide layer that prevents diffusion

[94] or by being incorporated into the layer interstitially [95]. Chopra [93] shows that some gases (e.g. O_2 or N_2) adsorb epitaxially and may increase the desorption energy of surface adatoms, thus, decreasing their mobility.

A repeat of these experiments was performed in O_2 and N_2 ambients to see if surface diffusion could be retarded and these results are plotted in Figure 38(a) and (b).

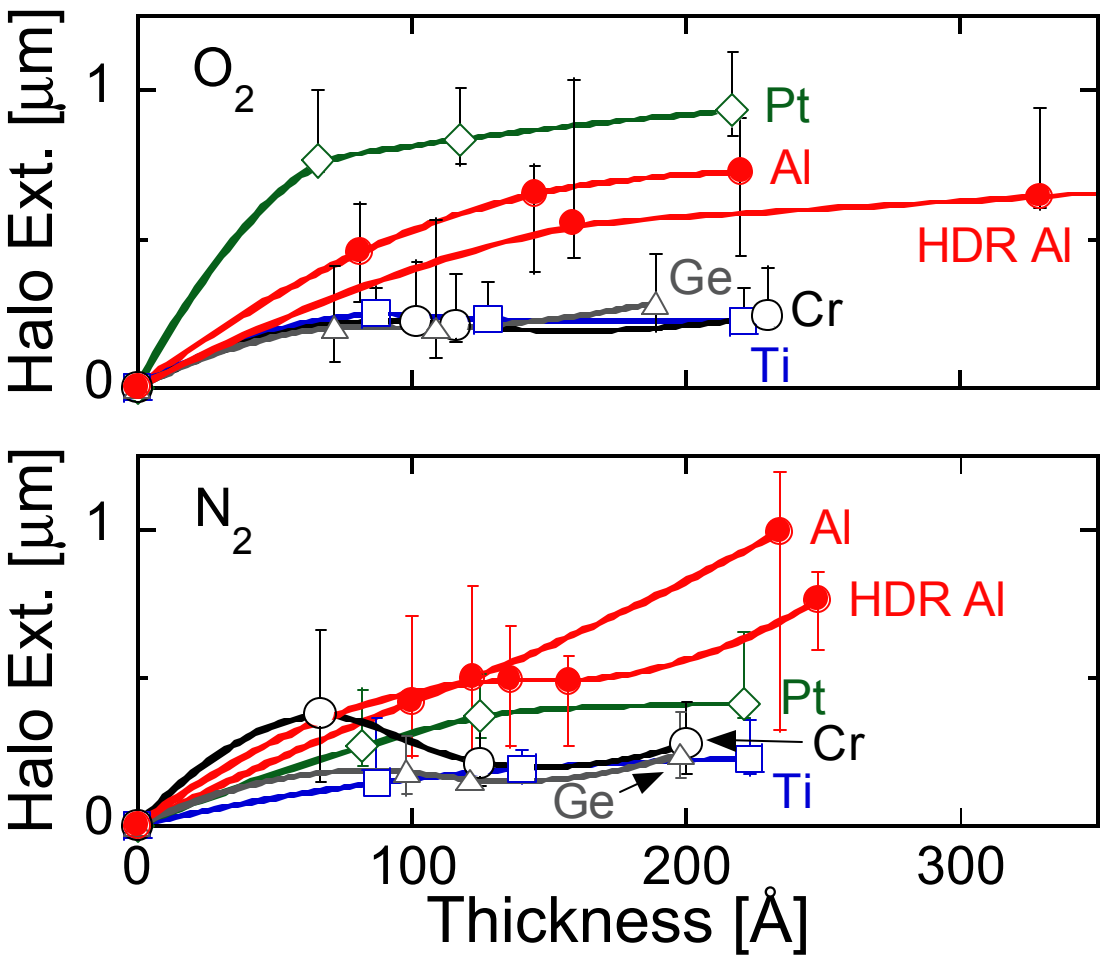

Figure 38. Halo extent (distance from deposition edge to edge of halo) vs. deposition thickness for materials deposited on SiO_2 at 45 °C: (a) with oxygen background pressure of 5×10^{-5} Torr and (b) with nitrogen background pressure of 5×10^{-5} Torr.

A pressure of 50 μTorr was selected. At this pressure and for a deposition rate of 10 Å/s the ratio of gas molecules striking the substrate to metal atoms adhering to the substrate is approximately 3:1 as can be calculated from the monolayer formation time of gas molecules [96]. Thus, at this pressure and deposition flux, there are comparable numbers of gas molecules and deposited atoms available for reaction and incorporation. A detailed discussion of calculating the hit ratio of the gas molecules versus the deposited molecules can be found in Appendix 6. The decrease in the halo extent for depositions in O_2 and N_2 are shown in Figure 38(a) and (b), respectively. For all the metals the extent of the halo was reduced by evaporation at the higher pressure in both ambients. In the vacuum experiments it was observed that in the case of Au, instead of continuous layers, microcrystalline islands form and diffuse on the surface. The presence of these scattered islands made measuring the extent of the halo and the thickness of the deposit too uncertain to include in the plots of Figure 38(a) and (b). The halo extent of Ti, and Cr became comparable to the Ge on evaporation in the gas ambient. The changes in the already low surface diffusion of Ge and HDR Al were small and within the error of the measurement.

The decrease in surface diffusion in O_2 and N_2 ambient is consistent with the following physical description. At 50 μTorr pressure, approximately 3 monolayers of gas molecules arrive at the deposition surface for each monolayer of metal, therefore there is an abundance of gas molecules on the surface that serve as nucleation centers. These impurity molecules immobilize adatoms by either forming a chemical bond [94] or providing a surface diffusion barrier in the diffusion path of a mobile adatom. The difference between the effects of ambient gases on the two sets of Al features can be

explained by the fact that the second sequence of features was deposited at a much higher rate; hence, the ratio of mobility-inhibiting gas molecules striking the surface is not enough to significantly influence the adatom movement during deposition.

5.5 Conclusions

Translated stencil masks have been used to deposit and compare the lateral diffusion of Al, Au, Cr, Ge, Pt, and Ti on SiO_2 near room temperature. The motion of the deposition edge of a film deposited through an aperture appears to be consistent with Fick's law diffusion, however the movement of the deposition edge out under the stencil mask as the deposition thickness increases suggests that the thicker film is feeding more adatoms into the region shadowed by the mask. Increasing the deposition rate of the deposited material retards the motion of material into the shadow region by decreasing the adatom surface mobility. By performing depositions in O_2 and N_2 ambients, the lateral motion was shown to be suppressed by a factor typically more than 2 and as much as $7 - 8\times$. A paper summarizing these results entitled Characterization and control of unconfined lateral diffusion under stencil masks has been accepted for publication by the Journal of Vacuum Science and Technology in 2007.

5.6 Diffusion at room temperature over 16 months

The metal structures deposited in vacuum were reexamined to see if any changes of the film morphology are observable 16 months after deposition. Over this time period the wafer was stored at room temperature in a 1" natural polypropylene wafer shipper (Fluoroware brand by Entegris, Inc., Chaska, MN). The same area of the sample imaged earlier was located and new SEM images were taken to assess the differences between the

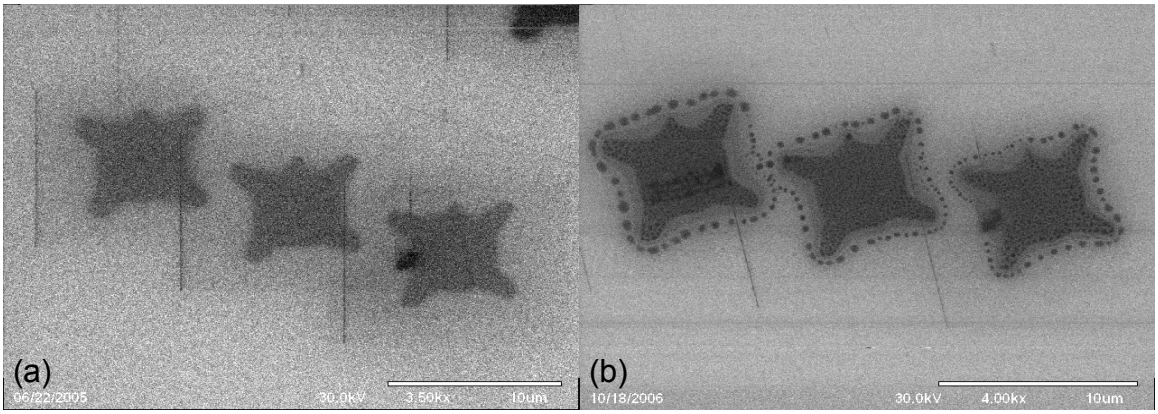

Figure 39. Scanning electron micrographs of structures created by a sequence of Al depositions through an approximately 7 µm length star-shaped aperture (a) immediately after deposition and (b) 18 months after deposition.

characteristics of the structures immediately after deposition and 18 months later, Figure 39.

The SEM micrographs show that around the Al structures 50 – 500 nm islands formed and spaced themselves in single file about the deposited feature. This island

formation can be observed on the surface of the deposits as well, with smaller (approximately 100 nm) islands that are more uniform in size. The rearrangement of material over the course of 16 months is direct evidence that Al atoms do not stop moving on the surface after the sample is removed from vacuum even at room temperature.

CHAPTER 6

DEVICE FABRICATION

6.1 Single nanowires

As the first demonstration of the ability of the PEN technique to create nanometer-scale features, single nanowires were fabricated. At the time of the early experiments [60] and the measurements to be discussed in Sections 6.1 and 6.2, the adverse effects of radiative heat, Section 3.4, and lateral diffusion during deposition, Section 5.3, were not known.

The smallest single wire demonstrated is shown in Figure 40. On a SiO_2/Si substrate, 88 nm Al was deposited at 1 Å/s rate as the sacrificial layer, then the substrate was translated by 200 nm, and a bilayer of 11 nm Ti and 33 nm Pt was deposited, both at 1 Å/s. The Ti layer served as an adhesion promoter because in earlier experiments Pt features were removed during lift-off without the Ti underlayer. Observations regarding adhesion of Pt on SiO_2 are described in Appendix 7. Differential etching was performed in room temperature HCl for 15 minutes. Shown in Figure 40 are three successive magnifications of a Pt/Ti nanowire.

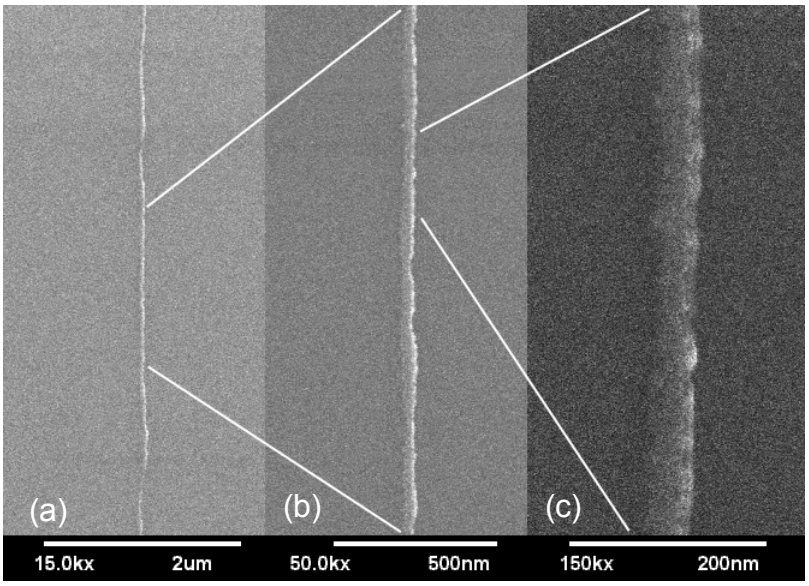

Figure 40. Scanning electron microscope image of a 40 nm Pt/Ti wire created by PEN. Moving from left to right successive expansions of the nanowire are shown. The highest magnification image (c) shows that the wire has a width of 40 nm.

Over the extension of several microns the wire has an average width of 40 nm and no observable breaks, Figure 40(a). In fact, this kind of continuity is observable over millimeter lengths. The enlarged portions of the same wire, Figure 40(b) and (c), show some edge roughness on the right side of the wire with maximum values around 20 nm. The left-hand side of the wire is straight and smooth; the irregularity of the right hand side of the wire is caused by tearing of the connection of the edge feature over the sidewall. The edge roughness may also be the result of Pt or Ti that remained attached to the wire edge after etching. The minimum width of the wire in Figure 40 is approximately 30 nm as can be seen in Figure 41.

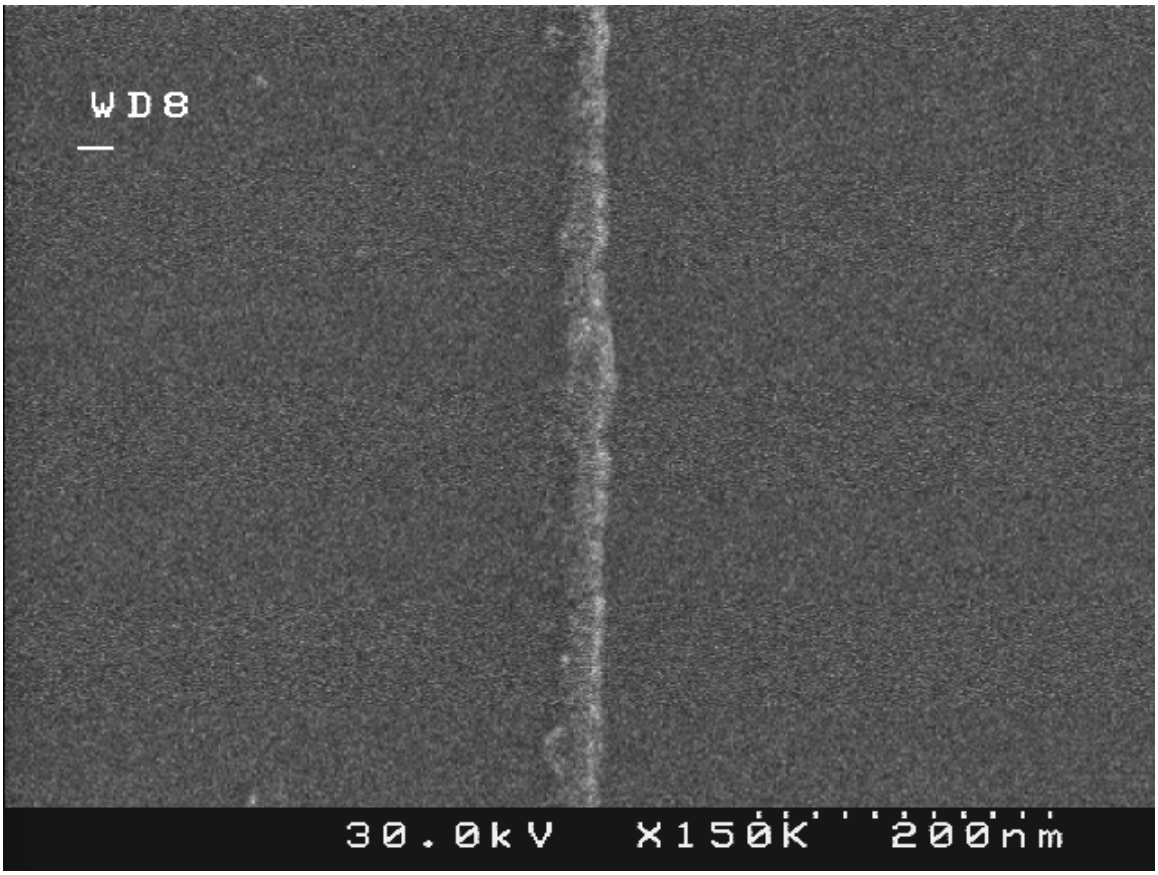

Figure 41. Scanning electron microscope image of a 30 nm Pt/Ti nanowire.

The successful fabrication of sub-100 nm nanowires without a heat shield, and active temperature control, and without compensating for lateral diffusion may be attributed to two factors. First, the Pt/Ti layer was deposited within 10 minutes of the sacrificial layer. This means that even though an increase in temperature would occur during the deposition of the sacrificial layer, the device layer would be deposited at a similar temperature which decreases the positioning inaccuracy due to thermal expansion. Secondly, based on the results discussed in Section 5.3, all of the three metals used in

these experiments (Al, Ti, and Pt) exhibited similar diffusive behavior which may have resulted in comparable edge motion of all three layers.

It is also possible that the few monolayers of atoms spreading around the deposits are too thin to produce observable features after differential etching. Figure 42 shows cross-sectional AFM linescans for a 24 nm Al and a 14 nm Pt feature created on SiO_2 in a deposition process described in Section 5.2. By shifting the Pt linescan by 500 nm to the right and adding it to the Al linescan, the cross-section of the structure formed by evaporating Pt on top of the Al after a 500 nm translation can be estimated.

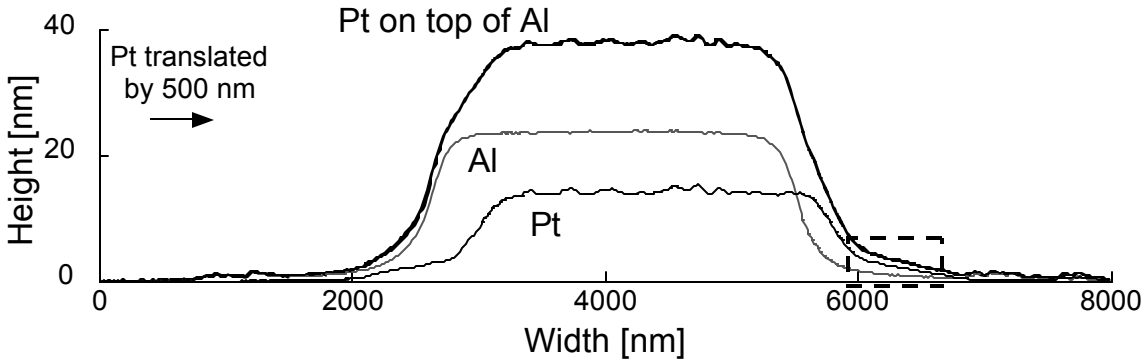

Figure 42. Cross-sectional atomic force microscope linescans of an Al and a Pt structure. The Pt linescan is shifted by 500 nm relative to the Al. The superposition of the Pt and Al linescans show the expected cross-section of a structure formed by depositing Pt on top of Al after a 500 nm translation.

It can be seen that although the extent of the lateral diffusion of Al and Pt is 2 and 1 μm, respectively, across this area the combined thickness of the Pt/Al layer is on the order of 1 – 2 nm. On the other hand, in the region indicated by the dashed rectangle a relatively thick Pt layer lies on top of a thin Al layer. It is possible the Pt in the dashed

region is not lifted off during differential etching due to the thinness of the underlying Al, thus forming an edge feature with a width comparable to the translation.

6.2 Nanowire pairs with controlled spacing

Piezoflexure-enabled nanofabrication is not only capable of creating sub-50 nm features, it also offers the possibility to control the spacing between the structures on the same nanometer-scale. In six separate pump-down cycles, three Pt and three Ti nanowire pairs of different widths and spacings were created using PEN. TABLE 4 summarizes the target widths and spacings for each wire pair. During these experiments the heat shield described in Section 3.1 was used to protect the PEN assembly from radiative heating, however, closed-loop temperature control was not used, and the lateral diffusion of the metals was not taken into account.

TABLE 4

TARGET DIMENSIONS AND SPACINGS FOR PLATINUM AND TITANIUM NANOWIRE PAIRS

	Platinum nanowire pairs			Titanium nanowire pairs	
	Width [nm]	Spacing [nm]		Width [nm]	Spacing [nm]
(a)	200	400	(d)	100	200
(b)	100	200	(e)	75	150
(c)	50	100	(f)	50	100

After the deposition of 44 nm Al at 5 Å/s as the sacrificial layer, the substrate, SiO_2/Si wafer, was translated to define the width of the first nanowire (200, 100, or 50 nm) and 22 nm Pt or Ti was deposited at 1 and 4 Å/s, respectively. After the deposition of the wire material, the substrate was translated to set the spacing between the wire pairs and a second sacrificial layer of 44 nm Al was deposited. Finally, the second wire was formed in the same manner as the first one.

The samples were etched in room temperature HCl to reveal the wire pairs. The etch times to completely remove the Al sacrificial layer and to lift off the overlaying Pt or Ti layers were between 3 to 26 minutes.

Figure 43 shows the resulting pairs of Pt, (a) – (c), and Ti, (d) – (f) nanowires. Also are shown the measured average widths of the wires and spacings.

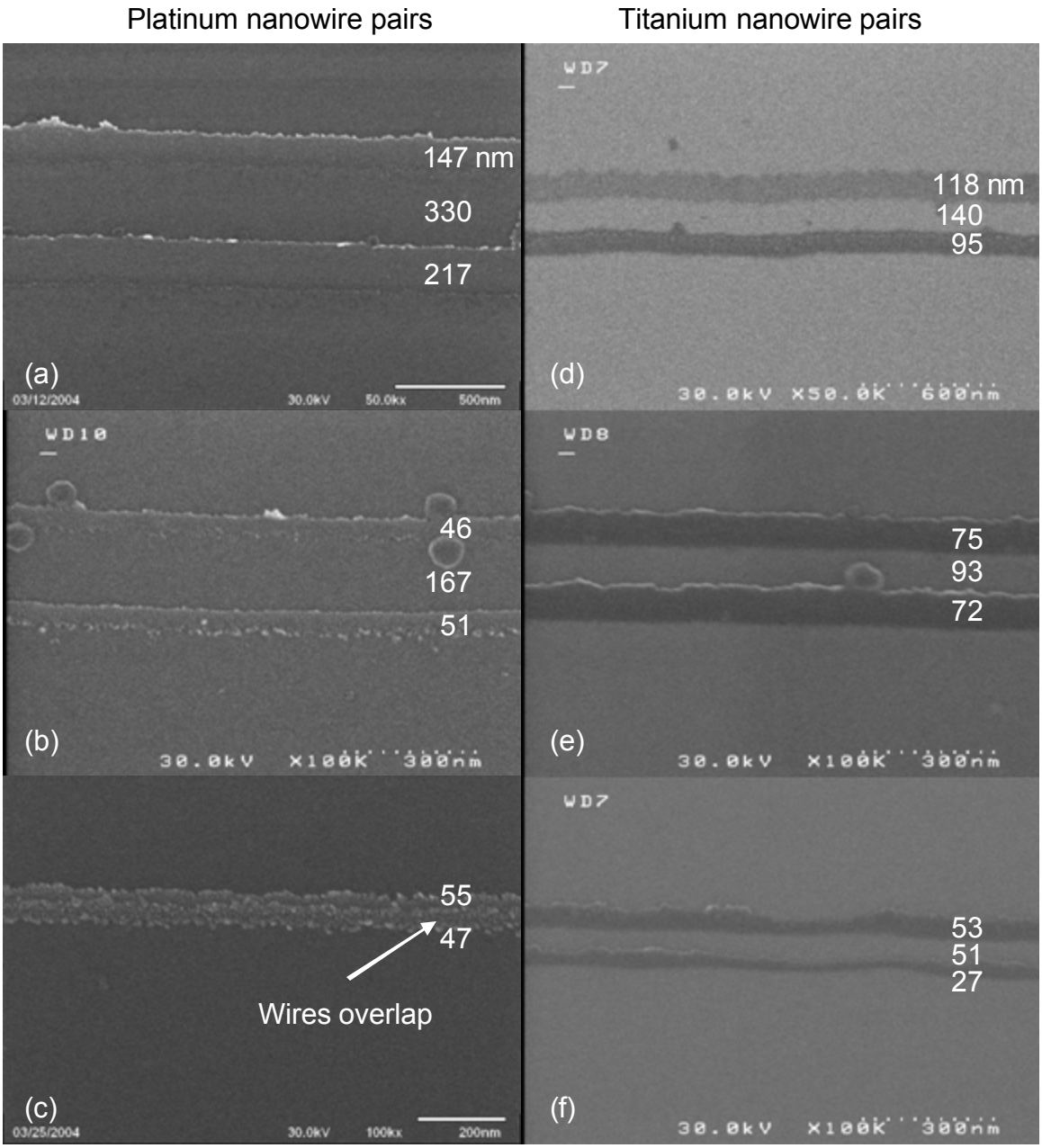

Figure 43. Scanning electron microscope images of Pt (a) – (c) and Ti (d) – (f) double nanowires of different sizes and spacings created by piezoflexure-enabled nanofabrication. The measured dimensions of the structures are also indicated.

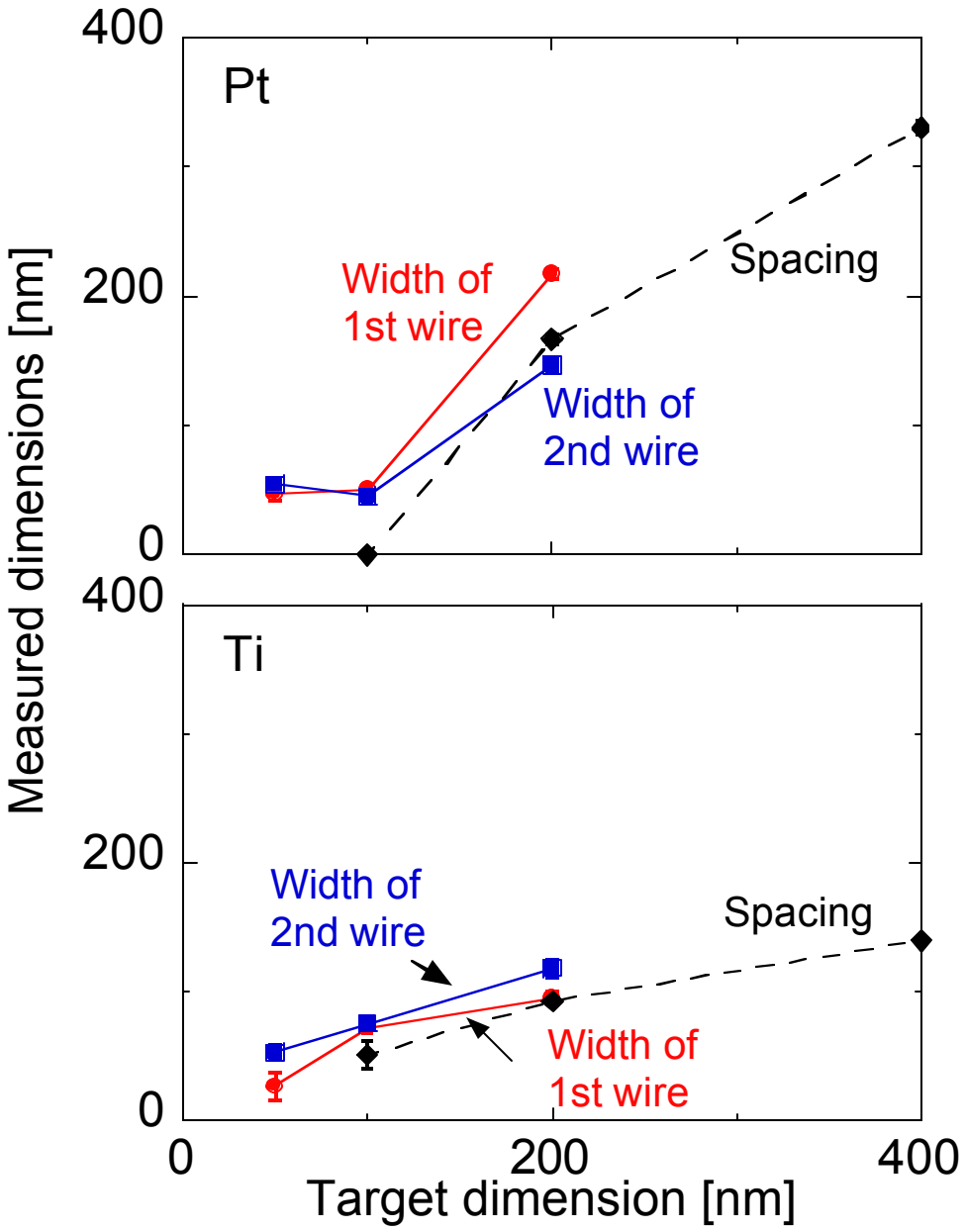

Figure 44. Measured vs. target dimensions of Pt and Ti wire widths and separations.

The measured widths and spacings of the fabricated nanowire pairs are plotted as a function of the target values in Figure 44. It can be seen that the actual dimensions are typically smaller than the targets. The error bars represent the standard deviation of the wire dimensions.

6.3 Nanowires and pads

As interconnect linewidth and film thickness shrink below 100 nm, the size and surface effects on resistivity become important [97]. For example, electronic transport can be expected to depend on film structure, edge roughness, grain size, and defects. These properties will manifest themselves in the electrical resistivity and in the physics of failure at high current density. Contact pads are necessary to probe wires of this scale, and with PEN they can be created in the same process with the nanowires without breaking the vacuum. This way the interface between the nanowires and the contact pads will not be contaminated or oxidized.

To demonstrate the capability of creating a single nanowire with contact pads using PEN, the structure shown in Figure 45 was fabricated. On an oxidized Si substrate, a 22 nm Al sacrificial layer was deposited at a rate of approximately 5 Å/s. The digital thermometer did not show an increase in the mask holder temperature during the Al deposition indicating a less than 1 °C temperature rise. Five subsequent Al depositions were performed to create sacrificial layers for other structures (not shown) during which the temperature of the mask holder did not rise. An 11 nm Ti layer was deposited at a rate of approximately 5 Å/s to form the nanowire after translating the substrate by 25 nm.

Finally, two 11 nm Ti layers were deposited at a rate of approximately 1.5 Å/s to form the contact pad. During these depositions the mask holder temperature also did not change. Differential etching was performed in hydrochloric acid at room temperature for 5½ minutes, with the beaker placed in an ultrasonic bath for the last 60 s.

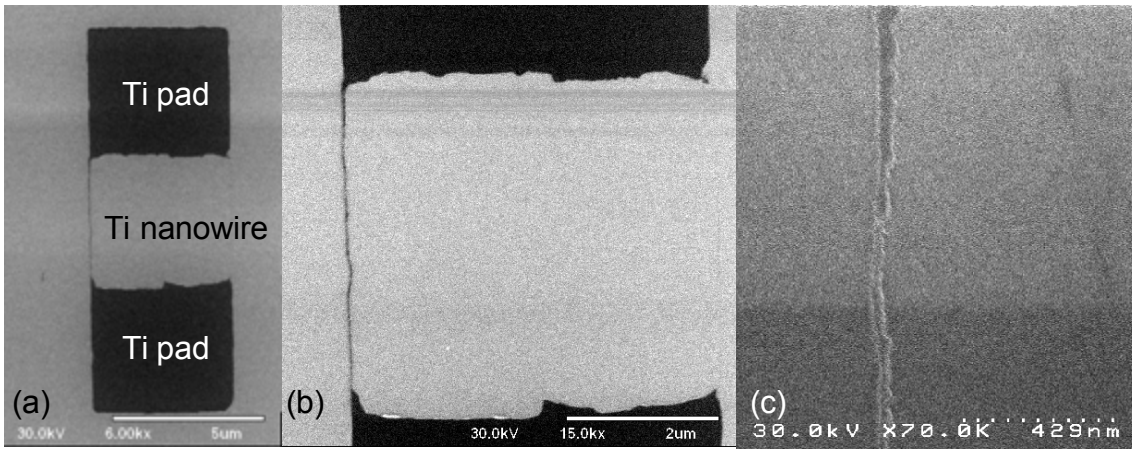

Figure 45. Scanning electron microscope images of an approximately 45 nm Ti nanowire with 4.6 μm Ti square pads connecting to both ends. Moving from left to right successive expansions of the structure are shown.

It can be seen that the pads are aligned to the wire feature with better than 50 nm accuracy and the wire is continuous over the distance between the pads, approximately 4 μm. Figure 45(b) and (c) are higher magnification SEM images of the same wire showing that the wire width is approximately 40 nm and some edge roughness with maximum values around 20 nm is present on the right side of the wire. The indentation in the middle of the wire is the result of a mask imperfection since it is present on the left side of the Ti pads as well. The alignment accuracy of the Ti pads is better than 50 nm.

The resistance of Cr nanowires was measured with the help of Wei Zhao of Notre Dame. Nanowires and contacts were created in a similar manner as depicted in Figure 11, using Ge as the sacrificial layer and Cr as the device layer. The selection of these two metals was made based on the lateral diffusion data of Section 5.3. Germanium produces the sharpest features of all the materials investigated and Cr is the least diffusive of all the device layer metals, Cr, Ti, Pt, and Au.

Through a 9 μm square aperture, 45 nm Ge was deposited at 18 Å/s, followed by the deposition of 10 nm Cr at 8 Å/s. Finally, 10 nm thick Cr pads were deposited. The lift-off was performed in Cyantek AL-12 at 70 °C. The current-voltage characteristics of a 700 and an 85 nm wide wire, 9 μm in length, were measured with an Agilent 4155B semiconductor parameter analyzer (Agilent Technologies, Inc., Santa Clara, CA) and are shown in Figure 46.

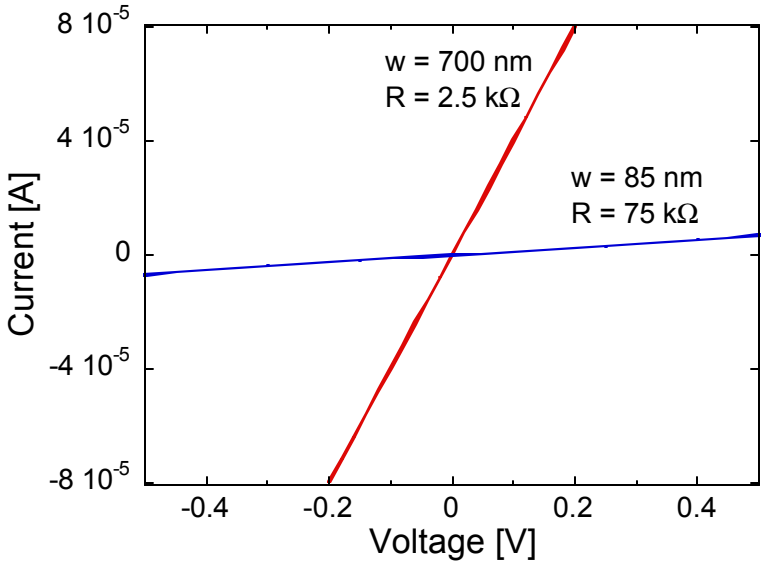

Figure 46. Current-voltage characteristics of a 700 and an 85 nm wide Cr nanowire of 10 nm thickness.

Over the range of -0.2 to 0.2 V, the I-V curve of the 700 nm wide wire is linear and the measured resistance is 2.5 kΩ which is 15× more than the calculated value for a wire with same dimensions using the bulk resistivity. Gould [98] showed that 10 nm thick Cr films deposited at 10 μTorr on a 20 °C substrate can have a resistivity approximately 20× the bulk value. The high resistivity of these films is attributed to surface scattering, small grain sizes (50 – 200 Å), contamination by residual gases during deposition, and absorption of air after deposition [98].

For the 85 nm wide wire, the maximum current measured for -0.5 to 0.5 V voltage range was less than 1.6 pA corresponding to 312 GΩ although it was verified by SEM that the wire was continuous. After driving a 1 μA current through the wire for 10 s, the measured resistance decreased to 75 kΩ, which is 56× more than the calculated value using bulk resistivity. The increase in resistivity compared to the 700 nm wire may be explained by increased grain boundary scattering due to the smaller horizontal dimension of the wire.

6.4 MOS capacitor arrays

The PEN system can be used to translate the substrate to a pristine area between depositions to allow the creation of arrays of MOS or other structures for material characterization. Each structure can be varied with respect to material, thickness, background pressure, and deposition parameters, e.g. rates and beam rastering. Such an array of structures formed by depositing Al on *p*-type Ge through a single square aperture under different deposition conditions is shown in Figure 47. This deposition sequence

enabled the formation of a 4-by-4 array of Al/Al_xO_y/*p*-Ge capacitors to electrically characterize the dielectric. With reference to Figure 47, the sequence of depositions was performed from left to right and from bottom to top with 25 μm translations between each deposition. First, Al_xO_y of 40 Å nominal thickness was deposited by evaporating Al at 5 Å/s in 5 μTorr O_2 background pressure. This was followed by the deposition of three 40 Å Al_xO_y by evaporating Al in 5 μTorr O_2. These three Al_xO_y layers were capped with 2000 Å Al deposited at 30 Å/s without O_2 background. The deposition rate for each 40 Å thick layer was varied as indicated in Figure 47, but the O_2 background pressure was kept constant using manual feedback control. In a similar manner, the middle two rows were deposited at different oxygen background pressures. Finally, the top row, consisting of Al_xO_y structures of varying thicknesses, was deposited at 5 Å/s in 10 μTorr O_2 background.

The three nominally 40 Å thick Al_xO_y features deposited at a constant rate but under three different O_2 background pressures, Figure 47(b), are used to measure the actual thickness of the Al_xO_y layers. The features in the 3-by-3 array, Figure 47(c), allow the systematic characterization of the electrical properties of the 40 Å thick Al_xO_y. By changing the O_2 background pressure in the evaporation chamber, the number of O_2 molecules striking the surface of a deposit changes, thus, the amount of O_2 incorporated into the deposit can be varied (see Appendix 6).

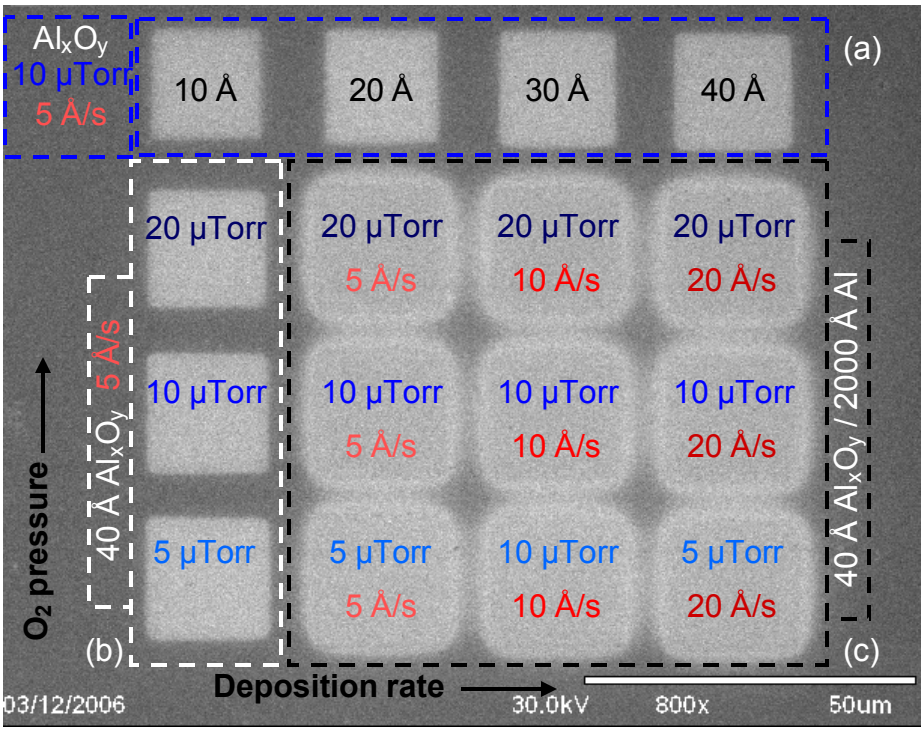

Figure 47. Scanning electron microscope image of an Al/Al_xO_y/*p*-Ge MOS capacitor array created in the PEN system. (a) Al_xO_y squares of different thickness created by depositing aluminum at 5 Å/s in a 10 µTorr O_2 background. (b) Al_xO_y squares of 40 Å thickness created by depositing Al at 5 Å/s in 5, 10, and 20 µTorr O_2 background. (c) Al_xO_y squares of 40 Å thickness capped by 2000 Å Al.

The aperture size, approximately 16 µm, and the thickness of the capping layer, 2000 Å, were designed to enable probing without damaging the underlying Al_xO_y features. As can be seen in Figure 47(a) and (b), the first two alumina features in each of the bottom three rows were created using the same deposition conditions. Having identical pairs of features makes it possible to perform morphological characterization and electrical measurements on the same sample eliminating measurement errors due to variations in process parameters.

Although deposited through an approximately 16 μm square aperture, the 2000 Å thick Al cap layers in Figure 47(c) expanded to approximately 24 μm most likely due to lateral diffusion of Al during deposition. The spreading of the Al layer suggests that lateral diffusion occurs not only on SiO_2/Si but on Ge substrates as well. As a result, a parallel Al/Ge Schottky-barrier contact is expected to shunt each MOS capacitor along the periphery, however, the capacitors were measured to be low leakage which suggests that there must be an oxide barrier to block the periphery current.

Based on Figure 38(a), a 40 Å thick Al_xO_y structure created by evaporating Al in O_2 is expected to spread 200 – 300 nm laterally. On the other hand, it can be seen from Figure 33 that the thickness of a high deposition rate Al deposit decreases to a few monolayers within less than 150 nm of the deposition edge. Beyond 150 nm only a very thin Al layer forms around the deposit which completely oxidizes in air. This way the non-oxidized, i.e. conducting, part of the Al cap layer is on top of the Al_xO_y layer and does not touch the Ge substrate.

It is also interesting to note in Figure 47(a) that as the thickness of the Al_xO_y deposits increases from left to right, the feature dimension increases as well. This apparent thickness dependence is in agreement with observations described in Section 5.4. This observation shows that lateral diffusion is significant even for very thin deposits.

Top-to-bottom current-voltage measurements of the Al/Al_xO_y/Ge capacitor structures were performed with the help of D. Wheeler of Notre Dame. Using the Agilent 4155B semiconductor parameter analyzer, equipped with a W probe and the wafer chuck grounded, the Al_xO_y layer was characterized in terms of breakdown voltage and leakage

current. For each measurement it was ensured that the probe made good contact with the Al cap without puncturing through it. The voltage was swept from 0 V to -1 V and back to 0 V, then a second measurement from 0 V to 1 V and back was appended. Figure 48 shows the I-V curves for the MOS capacitors deposited at 5 Å/s at three different O_2 background pressures.

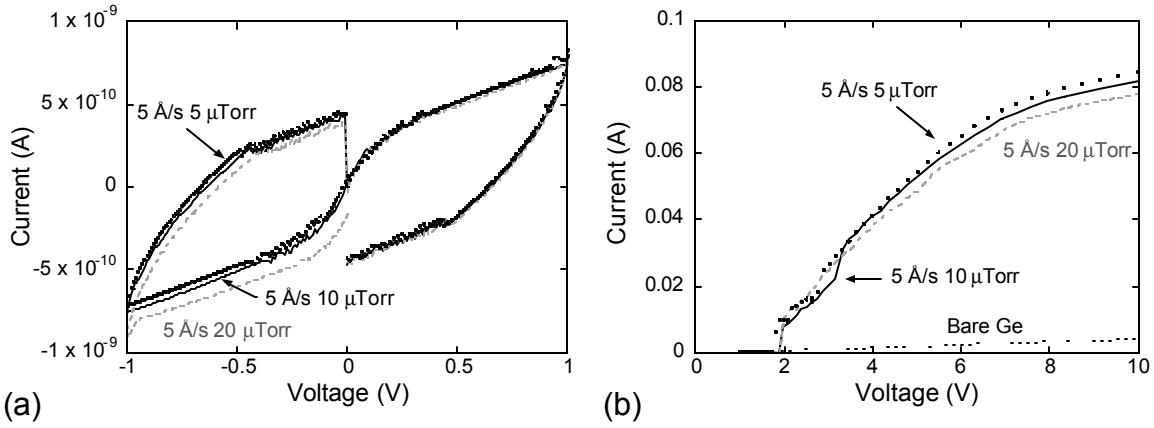

Figure 48. Current-voltage measurements of MOS capacitors deposited at 5 Å/s at three different O_2 pressures. (a) Hysteresis loops show that these structures are capacitors as expected. (b) When the bias voltage reaches 1.92 V, the Al_2O_3 dielectric breaks down.

The presence of hysteresis loops in Figure 48(a) show that these devices work as capacitors as intended. The leakage current, I_l, is approximately -7.93 × 10^{-10} A at -1 V. Using $r = UA/I_l t$, where U is the bias voltage, A is the area of the MOS capacitors, 16 μm × 16 μm, and t is the thickness of the Al_xO_y (4 nm), the resistivity of the Al_xO_y dielectric layer is estimated to be 8.07 × 10^{-10} Ωcm which is on the same order of magnitude with the value, 1.1 × 10^{-9} Ωcm, reported by Shamala et al. [99] for thermally-evaporated Al_2O_3.

The breakdown voltage of the same structures was measured by sweeping the bias voltage from 0 V to 10 V. The 4 nm thick dielectric layer of all three MOS capacitors broke down at approximately 1.92 V which corresponds to 4.8 MV/cm breakdown field which is in good agreement with values, 4 – 5 MV/cm, reported by Kolodzey et al. [100] and higher than the value, 1 MV/cm, reported by Shamala et al [99].

The electrical characterization of the MOS capacitors deposited at 10 and 20 Å/s produced similar I-V curves, therefore, it was concluded that the quality of the Al_xO_y layer does not vary significantly in the 5 – 20 μTorr O_2 pressure and the 5 – 20 Å /s range.

6.5 Thin film transistor structures

Besides structures created by sequences of deposition and translation, the PEN system is also capable of direct pattern writing through moving stencil apertures. The substrate is translated under a mask aperture during deposition leaving a feature with dimensions determined by not only the mask size, W_o, but the deposition rate, R, the translation length, L, and the translation velocity, v_t. The cross-section of such a structure is shown in Figure 49.

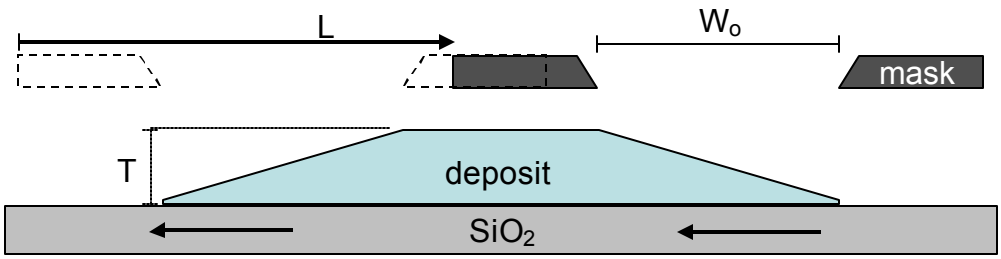

Figure 49. Schematic diagram of a feature deposited through a mask aperture while the substrate is translated. Dashed outline of the mask indicates the starting position of the mask. The shaded mask indicates the mask position at the end of the deposition.

For a translation greater than the aperture size, the horizontal dimension of the feature is equal to the sum of the translation length and the aperture size, $L + W_o$, and the width of the plateau is equal to their difference, $L - W_o$. The maximum thickness of the deposit, T, depends on the translation speed, the size of the mask aperture, and the deposition rate:

$$T = \frac{W_o}{v_t} R . \tag{12}$$

The sidewalls of the feature are sloped and the angle of the sidewall slope, a, can be calculated from the translation speed and the deposition rate:

$$a = \tan^{-1} \frac{R}{v_t} .$$

For a deposition at 10 Å/s with the substrate moving at 0.5 μm/s, the estimated slope angle is approximately 0.11°.

This technique enables the rapid fabrication of thin film transistors (TFT) where the channel of the transistor is created by direct pattern writing while the source, drain, and

gate electrodes, and the contact pads are created by deposition following the translation of the substrate to the desired position under the mask aperture. Figure 47 shows the schematic diagram of a poly-Ge channel TFT.

The channel of the TFT was created by depositing Ge at 10.5 Å/s while the substrate was translated by 10 μm at 0.5 μm/s. From Eq.(12), the estimated channel thickness is 105 Å. Two 100 Å Ti layers were deposited 7 μm apart at 7 Å/s to form the source and drain contacts. Titanium was selected to form the source and drain contacts because of its low Schottky barrier height to both n-type (0.77 eV) and p-type (-0.109 eV) germanium [101]. The gate oxide was formed by evaporating 30 Å Al at 2.2 Å/s in 28 μTorr O_2 background pressure. The gate metallization was created by depositing 500 Å Al at 20 Å/s. Finally, 2000 Å Al contact pads were deposited at 45 Å/s. Aluminum was selected to create the contact pads because it has low resistivity and can be evaporated at high rates (up to a 100 Å/s) to form thick layers. The TFT structure created using a 3.5 × 5 μm stencil aperture is shown in Figure 51.

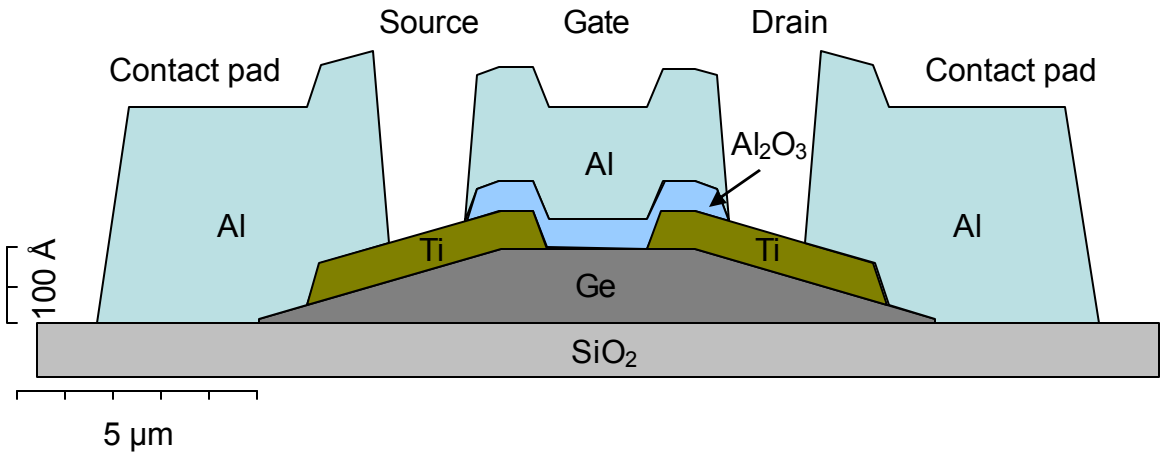

Figure 50. Schematic diagram of a TFT structure created in the PEN system. The channel of the transistor is created by depositing Ge while the substrate is being translated under a mask aperture. The Ti source and drain electrodes, the Al_2O_3 gate oxide, the Al gate metal, and the Al contact pads are created by deposition following the translation of substrate to the desired position under the mask aperture. The sloped sidewalls of the Ge channel are the result of the translation during deposition. The sloped sidewalls of the other features are to indicate the effect of lateral diffusion during deposition.

Also shown in Figure 51(a) is an additional structure that was created using the same deposition conditions and translations as for the channel and the drain and source electrodes of the TFT. Since this structure is identical to the channel of the TFT but is not covered by Al contact pads, the dimensions (length, width, and thickness) and the morphology of the channel can be accurately measured. The channel length, the

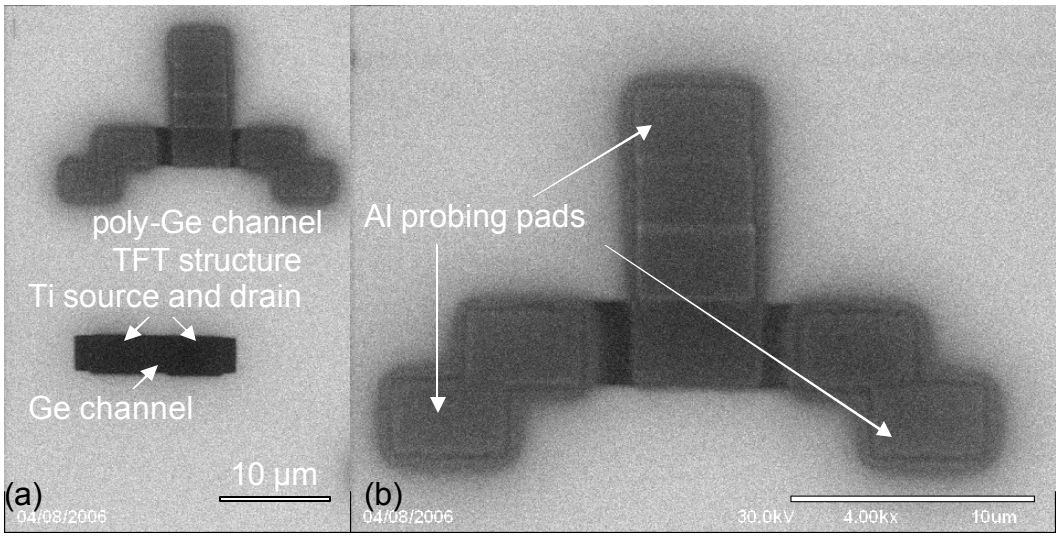

Figure 51. Scanning electron microscope images of a poly-Ge channel TFT transistor. (a) The TFT structure (top) and an additional structure created in the same way as the channel and the source and drain electrodes of the transistor (bottom). This structure is not covered by the Al contact pads, therefore, the dimensions and morphology of the channel can be measured. (b) Higher magnification scanning electron microscope image of the TFT structure.

separation between the source and the drain electrodes, is approximately 1.7 μm. It is also apparent that the source and the drain layers are wider than the channel itself due to the higher lateral diffusion of Ti compared to Ge. Figure 51(b) is a higher magnification SEM image of the TFT structure. In order to make sure that the probes would not touch during characterization, the location of the Al probing pads was designed to provide a minimum separation of 15 μm.

Electrical characterization of the TFT structure was attempted using the Agilent 4155B semiconductor parameter analyzer, however, making reliable contacts between the probe tips and the $3.5 \times 5\ \mu m^2$ Al probing pads proved impossible even when using probe tips with 0.5 μm diameter.

Another TFT structure was created using a 16 × 20 μm^2 rectangular aperture in a similar manner as described above. Germanium was deposited at 10.5 Å/s during a 40 μm translation of the substrate at 2 μm/s to form an approximately 100 Å thick poly-Ge channel. Two 100 Å Ti layers were deposited 30 μm apart at 4.5 Å/s to form the source and drain electrodes. The gate oxide was formed by depositing 50 Å Al at 5 Å/s in 25 μTorr O_2 background pressure. The gate metallization was created by depositing 500 Å Al at 20 Å/s. Finally, 2000 Å Al contact pads were deposited at 45 Å/s. Figure 52 shows SEM images of the TFT structure.

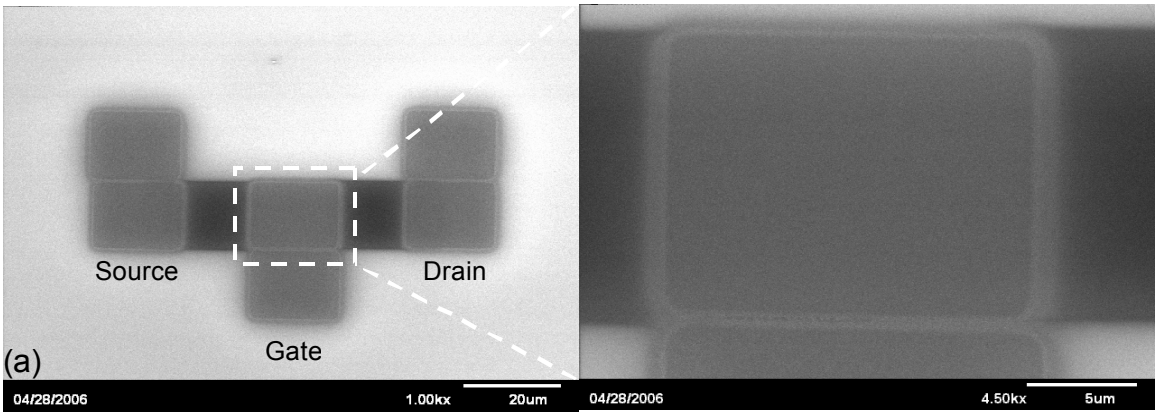

Figure 52. (a) Scanning electron microscope image of a poly-Ge channel TFT created using a 16 × 20 μm^2 rectangular aperture. (b) Higher magnification image of the gate area, indicated by the dashed rectangle on (a), showing the effect of lateral diffusion during the deposition of the 500 Å contact pad.

Current-voltage measurements of the TFT were performed. The channel resistance was determined by a two-probe measurement with probes contacting the drain and the source contact pads. The drain-source voltage, V_{DS}, was swept from 0 to 10 V five times and the drain current, I_D, was measured. The slope of the nearly linear I-V curve, shown in Figure 53(a), is 9 × 10^{11} A/V corresponding to 11 GΩ channel resistance. A third

probe was added to apply gate bias through the gate contact pad. The drain-source bias was swept from 0 to 10 V five times and the gate voltage, V_G, was increased by 1 V from 0 to 4 V. Figure 53(b) shows that as V_G was increased, the I_D curve was shifted by the same voltage which suggests that the measured drain current is actually a result of leakage between the drain and the gate. The same drain current was measured when the source probe was lifted and the measurement was repeated. The high gate-drain leakage current can be a consequence of the apparent lateral diffusion of the gate metallization, Figure 52(b), that may have created a lower resistance current path between the gate and the drain contacts.

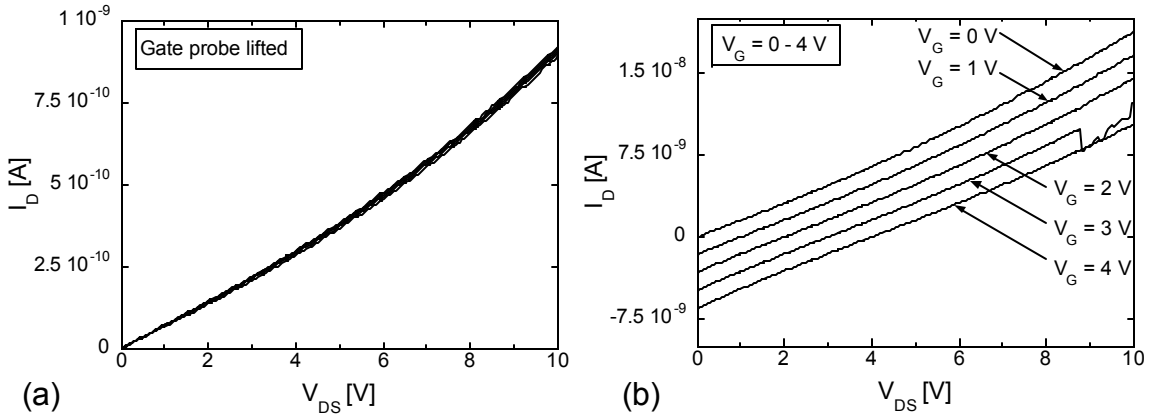

Figure 53. Current-voltage curves of the TFT structure shown in Figure 52. (a) Drain current vs. drain-source voltage with the gate probe lifted. (b) Drain current vs. drain-source voltage with the gate voltage changed from 0 to 4 V.

CHAPTER 7

SUMMARY AND SUGGESTED FUTURE WORK

7.1 Summary

Piezoflexure-enabled nanofabrication, a new nanoscale device fabrication technique based on the combination of dynamic stencil mask lithography and sidewall processing was explored and characterized. A system consisting of an Airco/Temescal FC1800 electron beam evaporator, a Polytec PI *x-y* nanopositioner and controller, a sample stage – mask holder assembly, a feedback temperature controller, and thermal shielding has been designed and constructed, and the capability of PEN to batch fabricate nanometer-scale structures orders of magnitude smaller than the stencil aperture size on full wafer scale in a single pump-down cycle of the evaporator has been demonstrated.

A stencil mask fabrication process based on the anisotropic KOH-etching of silicon was developed to produce rectangular and square apertures as small as approximately one-by-one square microns with edge uniformity on the order 30 nm.

The PEN process attributes such as geometrical edge taper, mask clogging, thermal expansion, and lateral material diffusion have been identified and characterized. The edge taper of the deposited patterns is intrinsically governed by the evaporation geometry and within the constraints of the evaporator, the dimensions of the PEN apparatus were

chosen to minimize this value. The rate of material build-up during deposition on the edges of the stencil apertures was directly measured for Al and found to be approximately $1/4^{th}$ of the deposited layer thickness. This phenomenon is expected to slightly increase the edge taper, however, it can be compensated for by an equal translation of the substrate during deposition. Thermal expansion of the components of mask-substrate fixture due to radiative heating from the evaporation source can introduce positioning inaccuracy on the order of microns. Thermal shielding and high-accuracy active temperature control was added to the PEN system to keep the components at a constant setpoint temperature during the deposition process.

Significant lateral diffusion of material under the stencil mask on the order of microns was found to occur during deposition even near room temperature. A quantitative study of this spreading behavior of Al, Au, Cr, Ge, Pt, and Ti on SiO_2 has been performed. Two mechanisms accounting for the lateral spreading of the deposited materials have been identified: the deposition edge moves by Fickian diffusion with a diffusion coefficient of 6.7 nm^2/s and a thin layer forms around the deposits as a result of surface diffusion. The extent of lateral spread was found to depend on the material and the thickness of the deposited structures. It was shown that this motion of material can be significantly suppressed by introducing O_2 or N_2 backgrounds during evaporation.

Nanowires with minimum feature dimension of approximately 30 nm were fabricated to demonstrate the capability of PEN to form nanometer-scale features. Nanowires with micron-scale pads were formed to show that PEN allows the simultaneous creation of both nanometer- and micron-scale features. The resistance of 700 and 85 nm Cr wires

was measured to be approximately 16 and 56× higher than calculated using bulk resistivity values.

Piezoflexure-enabled nanofabrication offers the possibility to control the spacing between these structures on the same nanometer-scale. Platinum and Ti nanowire pairs of different widths separated by nanometer-scale spacings were fabricated to show this capability.

An array of Al/Al_xO_y/*p*-Ge MOS capacitor structures was created for rapid characterization of Al_xO_y as gate dielectrics for field-effect transistors. Current-voltage measurements showed the presence of hysteresis as expected from capacitors. The average resistivity was measured to be 8.07×10^{-10} Ωcm at -1 V bias and the dielectric layer broke down at approximately 4.8 MV/cm field. Finally, thin film transistor structures were designed and fabricated using the direct pattern writing feature of the PEN system.

7.2 Suggested future work

In the course of this project it has become clear lateral diffusion during deposition is one of the most significant challenges associated with stencil lithography which makes reaching the one nanometer theoretical limit of PEN feature dimensions a very challenging goal. Fortunately, the thickness of the spreading layer is only a few monolayers and sub-50 nm edge features have been successfully created, but understanding this motion will be necessary to fully exploit the powers of PEN. The accurate characterization of the surface, temperature, and vacuum dependence of lateral

diffusion is necessary to identify substrates, materials and deposition conditions that minimize material spread which in turn enables reaching the practical limits of this technique. Lateral diffusion was shown to decrease in O_2 and N_2, however, it needs to be investigated how the incorporation of gas molecules into thin films during deposition influences the resistivity of the fabricated structures.

Another unexplored area related to lateral diffusion is how to make surfaces that impede the motion of adatoms during deposition either physically, e.g. rough surfaces, or chemically, e.g. surfaces that react with the deposited material.

The current temperature controlling method is based on heating the mask-stage assembly, therefore, the substrate temperature is also increased. Since diffusion lengths typically increase with higher temperature, active heating as a mean of temperature stabilization is not optimal from the point of lateral diffusion. Redesigning the PEN apparatus to employ cooling to keep the temperature constant during deposition has the promise of decreased lateral diffusion.

The feasibility of the PEN technique has been proved and the primary process attributes have been identified, the demonstration of nanomechanical devices such as the nanoelectromechanical tunneling transistor and inertial sensors seem to be the natural continuation of the research effort presented in this dissertation. The fabrication of such three dimensional structures requires the development of a cantilever release process. A release layer is necessary to prevent the cantilever from sticking to the substrate during the wet etching process steps. The preferred material for this release layer is not attacked during the differential etching of the electrode structures and can be removed by dry

etching. A possible candidate material for such a layer is Si because it can be deposited by electron-beam evaporation, and it can be removed selectively in gas-phase etches in a highly controllable manner.

Finding ways to apply the PEN technique to making electronic devices could be another interesting research area. For example, PEN provides a simple method to create antenna-coupled metal-oxide-metal diode infrared detectors with contact pads. The advantage this technique offers is that in a single experiment a multitude of devices created using different metals, oxides, deposition conditions, and geometries can be fabricated and tested.

APPENDIX 1:

DEFLECTION VS. BIAS CALCULATION FOR THE

NANOELECTROMECHANICAL TUNNELING TRANSISTOR

An analytic expression describing the deflection of a NMTT cantilever in response to an applied electric field can be obtained using a simple model in which the cantilever and the gate of the NMTT are considered as electrodes of a parallel plate capacitor with the top plate attached to a spring, Figure 54. It is assumed that the capacitance between the source and the drain is negligible because of the small area of the drain electrode.

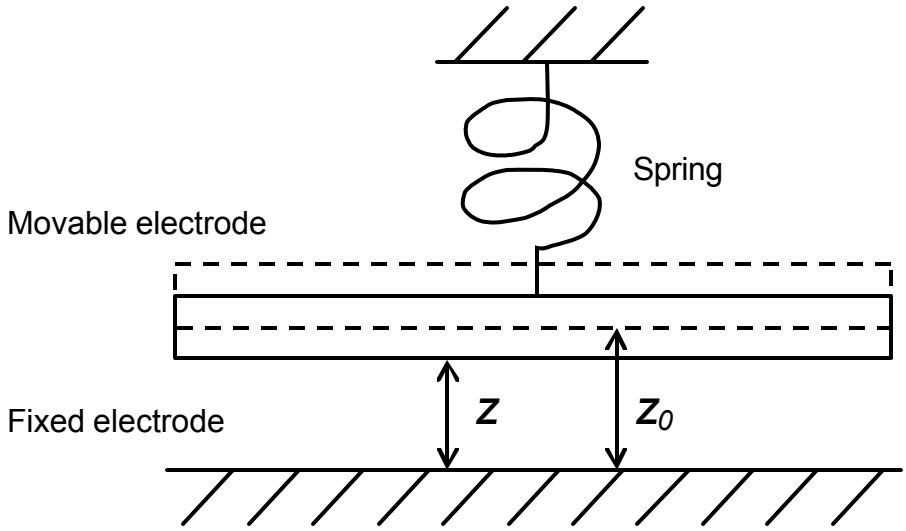

Figure 54. Schematic diagram of the model used to estimate the electrostatic behavior of the nanoelectromechanical tunneling transistor. The dashed rectangle represents the position of the cantilever when no bias is applied between the cantilever and the gate.

The total force between the two electrodes of a parallel plate capacitor, F_z, will be equal to the sum of the forces, df, between elemental charges, which can be calculated using Coulomb's Law. In order to simplify the calculations, the assumption is made that there is a homogenous electric field, $\mathscr{E}$, between the plates that has the same intensity and direction everywhere. Figure 55 shows the force acting between two elemental charges on the two electrodes separated by a gap, z.

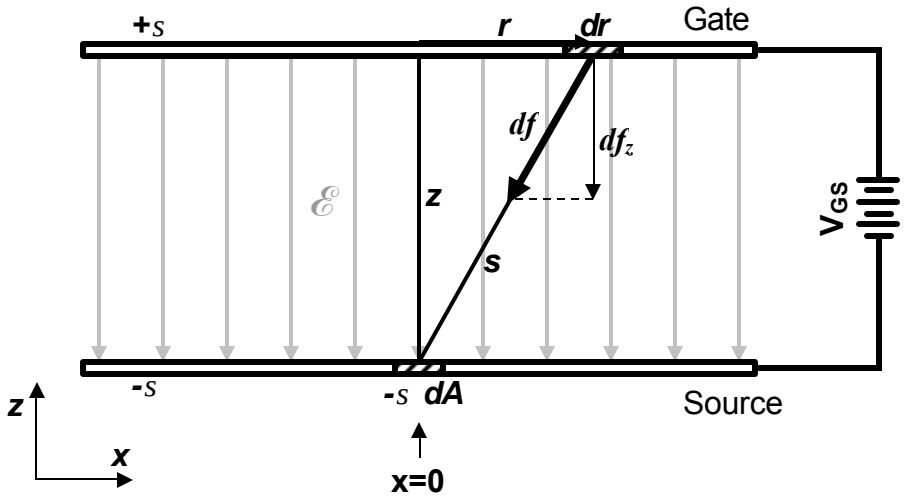

Figure 55. Schematic diagram of a parallel plate capacitor showing the force between two elemental charges.

In response to a potential difference, V_{GS}, charge $+Q$ and $-Q$ accumulate on the top and the bottom electrodes, respectively. Since both electrodes have the same area, A, the resulting surface charge densities, $\pm s = \pm Q / A$, are also equal. The charge of an elemental area, dA, on the bottom electrode is $-dQ = -s\ dA$. In order to calculate what force this elemental charge exerts on the charge on the top plate, the top plate is divided into concentric rings, and the forces between the elemental surface charge and the rings

of charge are calculated. The advantage of this approach is that the x and y components of the forces cancel.

The charge on a ring of radius r and width dr is $s\,2\pi r dr$ (the surface charge density multiplied by the differential area of the ring). Coulomb's Law can be used to calculate the force between these two charges:

$$df = k\frac{-s\,dA\cdot s\,2\pi r dr}{s^2} = \frac{-2\pi k s^2 r dA dr}{s^2} \tag{13}$$

where k is the electrostatic constant, $k = 1/4\pi\varepsilon_0$, where ε_0 is the permittivity of free space. The distance between the elemental charge and the ring charge is equal along the ring and can be expressed using the Pythagorean theorem in terms of r and z. Moreover, since the top electrode is attracted by only the z component of df, which can be expressed as $df_z = df\frac{z}{s}$, the force that the elemental charge exerts on the ring of charge becomes

$$df_z = \frac{-2\pi k s^2 z r dA dr}{\left(\sqrt{r^2+z^2}\right)^3} \tag{14}$$

The total force on the top electrode is the sum of all differential forces:

$$F_z = -2\pi k s^2 z dA \int_{r=0}^{\infty} \frac{r}{\left(r^2+z^2\right)^{3/2}} dr \tag{15}$$

Integration by substitution using $u = r^2 + z^2$ yields:

$$F_z = -2\pi k s^2 z dA\left[\frac{-1}{\sqrt{r^2+z^2}}\right]_{r=0}^{r=\infty} = -2\pi k s^2 z dA\frac{1}{z} = -2\pi k s^2 dA \tag{16}$$

The force per differential area (the force density) is $\frac{F_z}{dA} = \frac{-s^2}{2\varepsilon_0}$ and multiplying it with the surface area, A, gives the total electrostatic force, F_E, that pulls the top electrode towards the bottom one:

$$\left|F_E\right| = \frac{s^2 A}{2\varepsilon_0} = \frac{1}{2}sA\frac{s}{\varepsilon_0} = \frac{1}{2}Q\mathcal{E} \tag{17}$$

Since charge, $Q = CV_{GS} = V_{GS}\varepsilon_0 A/z$ and electric field, $\mathcal{E} = V_{GS}/z$, F_E can be rewritten as $F_E = \frac{1}{2}\varepsilon_0 A V_{GS}^2/z$. Equating the electrostatic force on the cantilever with the tension in the spring $(k_s(z_0 - z))$ yields,

$$V_{GS} = \sqrt{\frac{2k_s(z_0 - z)z^2}{\varepsilon_0 A}}, \tag{18}$$

where k_s is the spring constant. The gate bias has a maximum value of $V_{GSMax} = \sqrt{8k_s z_0^3/27\varepsilon_0 A}$ for a separation of $z = \frac{2}{3}z_0$, where z_0 is the undeflected distance of the cantilever from the gate. That is, the gate voltage required for a given deflection reaches a maximum when the cantilever is deflected to one third of the total gap between the cantilever and the gate. The gate bias as a function of the separation between the cantilever and the gate is shown in Figure 56. For gate voltages exceeding V_{GSMax}, the electrostatic force exceeds the spring force and the cantilever will accelerate into the fixed electrode.

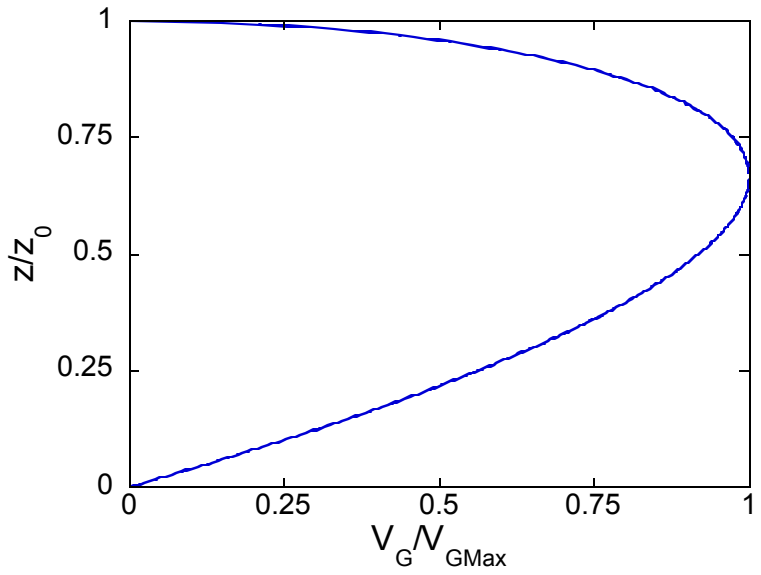

Figure 56. Gate bias, normalized to the maximum gate bias, as the function of the separation between the cantilever and the gate, normalized to the undeflected separation.

Energy considerations give further insight into the behavior of the cantilever. The total energy of the system after the deflection of the cantilever towards the gate electrode is equal to the difference between the initial electrostatic energy of the capacitor and the electrostatic energy expended to do mechanical work plus the energy of the expanded spring [102].

$$\mathscr{E} = \frac{\varepsilon_0 A V_{GS}^2}{2z_0} - \frac{\varepsilon_0 A V_{GS}^2}{2z} + \tfrac{1}{2} k_s (z_0 - z)^2 \qquad (19)$$

The energy versus the separation for three different values of V_{GS} (V_{GS} is expressed as a portion of V_{GSMax}) is shown in Figure 57.

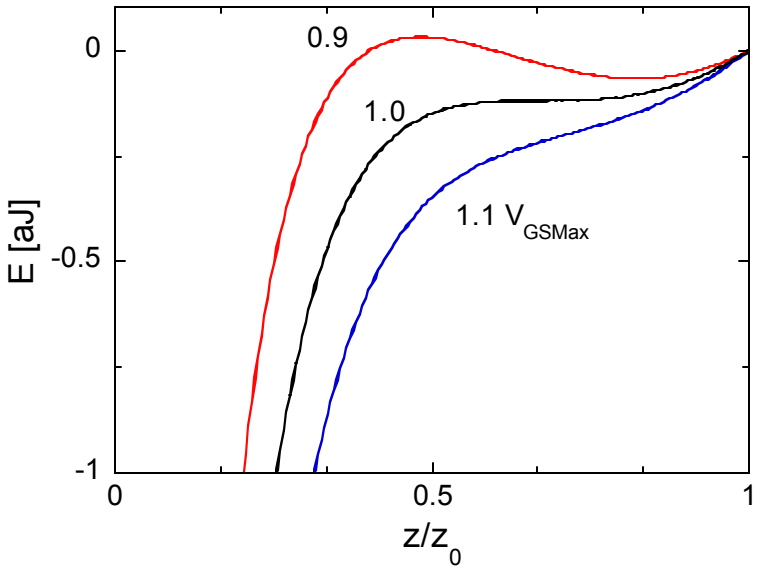

Figure 57. Energy, normalized, as the function of the separation between the cantilever and the gate, normalized to the undeflected separation.

For $V_G < V_{GMax}$, there is one stable position. As long as $z/z_0 > 4.9$, the cantilever will return to this stable position. For $V_G > V_{GMax}$, there is no stable position, z goes down to 0, i.e., the cantilever crashes to the lower electrode. For $V_G = V_{GMax}$, there is an energetically stable position at $z = \frac{2}{3} z_0$, however, this stability is very sensitive, the smallest decrease in z would cause the cantilever to crash. Therefore, for stable device operation in tunneling mode, the tunneling gap, w_t, must be less than one-third of the undeflected gate-cantilever distance, z_0.

APPENDIX 2:

SELECTED CHEMICAL WET ETCHANTS

OF METALS OF INTEREST FOR PEN

Differential etching was not examined extensively in the course of this investigation. Two etchants were used for Al: a commercial Al etchant, Cyantek AL-12, containing HNO_3, H_3PO_4, and CH_3COOH, and HCl. In future etchants need to be selected based on their etch selectivity. This appendix is a start at compiling some etchants which can serve as a resource for future research. All quantities are in milliliters unless otherwise noted.

ALUMINUM

Aluminum dissolves in strong and weak acids or bases. The start of the etching is delayed by the natural aluminum-oxide layer which is normally up to 5 nm thick. The start and the end of the reaction are recognizable by the start and the end of the generation of gas. [105]

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
HCl	~30%	Use at 20-50 °C	105
H_2SO_4	~30%	Use at 20-50 °C	105
H_3PO_4	~65%	Etch rate: 200 nm/min at 50 °C	105
HF : H_2O	11 : 100		106
HNO_3 : H_2O	11 : 100		106
HCl : HNO_3	2 : 1		106
NaOH : H_2O	10-20 g : 100 ml	Use at 60-70 °C, with higher concentration also at RT	107
NaOH : $ZnCl_2$: H_2O :	0.5 - 25 g : 1 g : 100 ml :		107
HCl : HF : H_2O	15 : 10 : 90		107
HNO_3 : HF : H_2O	6 : 2 : 92		107
H_3PO_4 : HNO_3 : CH_3COOH	25 : 1 : 5	Etch rate: 2000 nm/min at 70 °C, 2000 nm/hour at 20 °C	105
H_3PO_4 : HNO_3 : CH_3COOH : H_2O	80 : 5 : 5 : 10	Aluminum Etchant Type A by Transene Comp. Inc, Danvers, MA Etch rate: 530 nm/min at 50 °C	108
H_3PO_4 : HNO_3 : H_2O	80 : 5 : 0-20	Etch rate: 150 nm/min at 40 °C	109
HCl : HNO_3 : HF	75 : 25 : 5	Use fresh	107
H_2SO_4 : HF : H_2O	12.5 : 12.5 : 100		106
$FeCl_3$: H_2O	11 g : 100 ml		106
HF : saturated $Al_2O_{12}S_3$ solution	10 : 100		106
HF : H_3PO_4 : H_2O	6 : 11.7 : 100		106
Na_3PO_4 : H_2O : CH_3COOH	11 g : 100 ml : 1 ml		106

CHROMIUM (AND MOLYBDENUM)

Chromium and molybdenum are chemically related and exhibit similar behavior[110]. Chromium is highly resistant to acids but reacts with dilute HCl, H_2SO_4; not with HNO_3 [111] and can be dissolved in some alkaline solutions [110].

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
$HCl : H_2O_2$	3 : 1		110
$NaOH : K_3Fe(CN)_6 : H_2O$	10 g : 30 g : 100 ml	Temperature up to 40 °C	110
$(NH_4)_2Ce(NO_3)_6 : HClO_4 : H_2O$	9 %wt. : 6 %wt. : 85 %wt	CR-7 by Cyantek Corp., Fremont, CA Etch rate: 170 nm/min at RT	108
$(NH_4)_2Ce(NO_3)_6 : HClO_4 : CH_3COOH$	22 %wt. : 8 %wt. : 70 %wt	CR-14 by Cyantek Etch rate: 93 nm/min at RT	108
$H_2SO_4 : H_2O$	1 : 9	Use boiling	113
$HNO_3 : HCl$	1 : 3	Use fresh	113
$HNO_3 : HF$	1 : 3		113
$HNO_3 : HF : H_2SO_4 : H_2O$	20 : 10 : 15 : 50		113
a) $KOH : H_2O$ b) $K_3[Fe(CN)_6] : H_2O$	10 g : 100 ml 10 g : 100 ml	For Mo and W, NaOH and $Na_3[Fe(CN)_6]$ can also be used. Use fresh	113

GERMANIUM

Germanium is not etched by HCl and dilute alkali hydroxides but is attacked by aqua regia, concentrated HNO_3 and H_2SO_4, alkali peroxides, nitrides, and carbonates [114].

Etchant	Ratio/Conc.	Comments	Ref.
H_2O_2	30 %	Etch rate: 0.15 μm/min at 74 °C, 0.22 at 83, 0.31 at 93, and 0.4 at 102	115
$NH_4OH : H_2O_2 : H_2O$	1 : 1 : 5	Standard RCA-1 clean solution	116
$HNO_3 : CH_3COOH : HF$	5 : 3 : 3	Etch rate: 26 μm/min	117
$H_2SO4 : H_2O_2 : H_2O$	10 : 1 : 2	Caros's etch. Etch rate: 10 nm/min	117

GOLD

Gold is an electrochemically noble metal, therefore, it can only be dissolved in a very strong oxidant or in weak oxidants with a complexing agent. Gold dissolves in boiling in aqua regia (3:1 part by volume mixture of 38% HCl and 65% nitric acid). Gold is superficially attacked by aqueous halogens at room temperature. Complexing gold strippers containing cyanides can also be used to etch Au. [118]

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
Dehydrated Na_2CO_3 : $O_2NC_6H_4SO_3Na$: NaOH : NaCN	38 g : 60 g : 2 g : 100 g	Dissolve the salts in the given sequence in H_2O. Thick Au layers are eaten away at 50-60° C in 10-30 minutes. During short low temperature etches Al is hardly attacked.	119
KI : I_2 : H_2O	4-4.6 g : 1-1.3 : 40-100 ml	The concentrated version has an etch rate of 500-1000 nm/min at 20 °C. Selective to Al at 20 °C	119
C-35		This is a proprietary etch by Film Microelectronics Inc., Burlington, MA. It works at room temperature and is quite selective.	112
HCl : HNO_3	3 : 1	Non-selective: attacks most metals. Faster hot: 25-50 µm/min	112
a) KCN : H_2O b) $(NH_4)_2S_2O_8$: H_2O	10 g : 100 ml 10 g : 100 ml	Double KCN and $(NH_4)_2S_2O_8$ content before using.	120
$FeCl_3$: H_2O : H_2O_2 (3%)	32 g : 100 ml : 100 ml		120

MOLYBDENUM (see also CHROMIUM)

Molybdenum is not attacked by dilute acids or concentrated HCl. Molybdenum is practically insoluble in alkali hydroxides or fused alkalines but reacts with HNO_3, hot concentrated H_2SO_4, fused $KClO_3$ or KNO_2. Molybdenum is also attacked by F_2 at room temperature, by Cl_2 or Br_2 at a red heat. [121]

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
HCl : H_2O_2	1 : 1		112
$K_3Fe(CN)_6$: NaOH : H_2O	30 : 10 : 60		122
HNO_3 : HF : H_2O	33 : 33 : 34		122
HNO_3 : H_2O_2 : NH_3 solution			122
HNO_3 : HF (40%) : HCl	15 : 30 : 15		113
HNO_3 : HF (40%) : H_2O :	35 : 15 : 75		113
HNO_3 : HF(40%) : $C_3H_6O_3$	10 : 10 : 10-20	Use fresh	113

NICKEL

Nickel is slowly attacked by dilute HCl, H_2SO_4, and HNO_3. Fused alkali hydroxides do not etch Ni [123].

Nickel is particularly difficult to etch due to its chemical ruggedness. Even for microetching strongly concentrated acids are necessary, so that there are hardly special macroetchants. Additionally, nickel forms a thin handling layer, which can be eliminated only by repeated polishing and etching. [124]

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
$HF : HNO_3$	1 : 1		112
$H_2O : HNO_3$	50 : 50-100		125
$CuSO_4 : H_2O :$ $HCl : C_2H_5OH$ (96%) :	10 g : 50 ml : 50 ml : 50 ml		125
$CuSO_4 : H_2O :$ HNO_3	10 g : 10 ml : 20 ml		125
$H_2O : HNO_3 : HCl$ $: H_2O_2$ (30%)	20-30 : 0-20 : 20 : 10	Use fresh	125
$HCl : HNO_3 :$ $FeCl_3$ solution	600 : 18.5 : 125	Use boiling	125
$HNO_3 : HCl$	20 : 100		125
$FeCl_3 : HCl : H_2O$ or C_2H_5OH (96%)	5-8 g : 2-25 ml : 20-100 ml		125
a) $KCN : H_2O$ b) $(NH_4)_2S_2O_8 :$ $H_2O : H_2O_2$ (3%)	5 g : 95 ml 10 g : 100 ml : few drops		125
$CrO_3 : HCl$	0.01-1 g : 100 ml		125
$NaOH : H_2O_2$ (30%)	85 : 15		125
$CuCl_2 : C_2H_5OH$ or CH_3OH (95%) : HCl	2 g : 40-80 ml : 40 ml		125

PLATINUM

Platinum is resistant to single inorganic acids but it can be etched in boiling aqua regia with the formation of chloroplatinic acid. Platinum is also attacked by halogens, by caustic alkalines, alkali nitrates, and alkali peroxides. In the presence of reducing agents arsenates and phosphates also can be used to etch Pt. [126]

One other effective etchant is boiling hydrogen peroxide (30%) [127].

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
H_2O_2		Use boiling	112
HCl : HNO_3	3 : 1	Use hot	112
NaCN : H_2O	5.5 g : 100 ml		128
H_2SO_4 : H_2O	25 : 100		128

TANTALUM

Tantalum is almost completely immune to chemical attacks at temperatures below 150 °C. Tantalum is only attacked by HF, acidic solutions containing the fluoride ion, and free sulfur trioxide. Alkalis attack Ta only slowly. At high temperatures, tantalum becomes much more reactive. [135]

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
H_2SO_4 : HNO_3 : HF	50 : 20 : 20		127
HF : HNO_3	1 : 1		112

TITANIUM

Titanium is resistant to dilute sulfuric and hydrochloric acid, most organic acids, moist chlorine gas, and chloride solutions [129]. In general, Ti is attacked only by acids at high temperature [130]. Nitric acid oxidizes Ti to the dioxide. [130] Titanium dissolves in H_2SO_4 at 80° C and in 30% H_2O_2 at 50-60° C [131].

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
HF : HNO_3 : H_2O	1 : 1 : 50	Use at 60-80 ºC	112
H_2O_2 (30%) : NH_4OH (25%)	100 : 5	Use at 50-60° C	131
H_2SO_4		Use at 80° C	112
HF : H_2O	1 : 9		132
$Fe(NO_3)_3$: $C_2H_2O_4$: H_2O : HF (40%)	10 g : 35 g : 200 ml : 2 ml		133
HCl : H_2O	50 : 50		133
H_2O_2 (30%) : H_2O : KOH solution (40%)	15 : 78 : 12		133

TUNGSTEN

Tungsten is very resistant to single acids, it is only attacked by concentrated HNO_3 or aqua regia [134].

Etch solutions:

Etchant	Ratio/Conc.	Comments	Ref.
KH_2PO_4 : KOH : $K_3Fe(CN)_6$	34 g : 13.4 g : 33 g	Add water to make 1000 ml. Etch rate: ~160 nm/min at 20° C	110
HF (49%) : HNO_3 (65%)	1 : 1		131
H_2O_2 (30 %)		Can add conc. NH_3. Use at 20° C and at high temperature	131

APPENDIX 3:

LOW PRESSURE STOICHIOMETRIC SILICON NITRIDE

DEPOSITION PROCESS RECIPE

During the KOH-based silicon stencil mask fabrication process both sides of the Si wafers are covered with a silicon nitride masking layer. Approximately 1000 Å thick silicon nitride is deposited using the following process settings of the low-pressure chemical vapor deposition furnace.

(a) ASM LPCVD recipe:

Step	**Time (min)**	**Temp. (°C)**	**Pressure (Torr)**	**Silane (slpm)**	**Ammonia (slpm)**	**N_2O (slpm)**
Ramp N_2	1	820	0.25	×	×	×
Flow N_2	17	820	0.25	500	5	×
Pumpdown	1	820	×	100	1	×
Ramp Gas	2	820	0.2	1000	1.2	×
Flow Gas	60	820	0.2	1000	1.2	×
Pumpdown	1	200	×	1000	10	×
Purge N_2	15	200	×	100	2	×

This recipe was changed for unrelated reasons but the Si mask patterning process worked with the following recipe as well.

(b) Modified ASM LPCVD recipe:

Step	Time (min)	Temp. (°C)	Pressure (Torr)	Silane (slpm)	Ammonia (slpm)	N_2O (slpm)
Start3	0.08	200	×	1000	10	×
Slowpump	10	325	×	1000	10	×
Pumpdown	1	820	×	1000	10	×
Leakchk	1	820	×	1000	10	×
Pumpdown	1	820	×	1000	10	×
Ramp N_2	1	820	0.25	250	2.5	×
Flow N_2	17	820	0.25	500	5	×
Pumpdown	1	820	×	100	1	×
Ramp Gas	2	820	0.2	1000	1.2	×
Flow Gas	75	820	0.3	1000	1.2	×
Pumpdown	1	200	×	1000	2	×
Purge N_2	15	200	×	1000	2	×
Pumpdown	1	200	×	1000	10	×
Leakchk	1	200	×	1000	10	×
Backfill	10	200	×	1000	10	×
End3	0.17	200	×	1000	10	×

× = 0 flow setting and not checked by recipe step

APPENDIX 4:

SILICON NITRIDE PATTERNING PROCESS TRAVELER

The process of silicon stencil mask fabrication using KOH-etching is outlined in Figure 22. The process steps included in this traveler are used to pattern the approximately 1000 Å masking silicon nitride layer before anisotropic KOH-etching.

Wafer #: Date:

1. 10 min at 70 °C RCA 1 and RCA 2 clean
2. 110 °C dehydration bake for 2 min on hot plate
3. Apply photoresist (HMDS+AZ5214) using recipe #9 (4000 rpm for 30 s)
4. 90 °C bake for 1 min on hot plate
5. Exposure:
   Karl Suss #... Intensity:…….. mW/cm^2 (160 mJ/cm^2 needed → ……. s)
6. Develop in AZ327 for 45 s
   Inspect development with optical microscope
   Measure photoresist thickness after developing with step profiler:
   Step down: ……µm, ……µm, ……µm,
   Step up: ……µm, ……µm, …… µm
7. RIE etching:
   10 min CF_4 seasoning if other gas was used previously
   5 min CF_4 etching
   Measure photoresist thickness after RIE etch with step-profiler:
   Step down: ……µm, ……µm, ……µm,
   Step up: ……µm, ……µm, …… µm
8. Rinse in acetone and methanol for 1 min

9. Strip photoresist in DryTek for 15 min
10. Rinse in acetone and methanol for 1 min
11. Step-profile depth of the openings:

    Step down: ……μm, ……μm, ……μm,

    Step up: ……μm, ……μm, …… μm

Remarks:

a) Make sure the mask is in contact with the wafer during exposure
b) 45 s developing should be enough if using fresh AZ 327
c) 5 min RIE etching works for an individual wafer and two wafers as well

APPENDIX 5:

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Nanofabrication using nanotranslated stencil masks and lift off

Zoltan Racz, Jianli He, Srivatsan Srinivasan, Wei Zhao, and Alan Seabaugh[a)]
266 Fitzpatrick Hall, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556

Keping Han, Paul Ruchhoeft, and Jack Wolfe
Department of Electrical and Computer Engineering, University of Houston, Houston, Texas 77204

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We propose and demonstrate a technique for forming nanometer-scale metal features based on evaporation onto a substrate through a stencil mask. In this work, the stencil mask is laterally translated by a piezoflexure stage, between evaporations of different metals. The metals are chosen based on their etch chemistry to allow one material to be lifted off with respect to another. In this way, sidewall features are formed with dimensions and spacings controlled by moving the translational stage, which has 1 nm resolution. © *2004 American Vacuum Society.*
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I. INTRODUCTION

Simple fabrication approaches are desired for sub-50 nm feature formation. In particular, it would be useful to construct wires with nanometer dimensions spaced relative to one another with nanometer precision. In this article, we describe a sidewall process in which the feature sizes are set by the piezoelectric translation of a stencil mask and the features are revealed by a bimetal lift-off process. Since commercial piezoelectric positioning stages now achieve nanometer resolution, the minimum feature size of this technique approaches a few nanometers. Nanofabrication using stencil masks has been previously reported,[1,2] but not in combination with sidewall processing.

The nanomechanical device which has motivated this work is shown schematically in Fig. 1. This switch[3] consists of two nanometer-scale metal lines of different thicknesses and an overlying metal cantilever. The gap between the cantilever source electrode and the supply-connected drain electrode, d_C, is made shorter than the gap between the source and gate-connected electrode, d_G. When a bias is applied between gate and source, the source cantilever is attracted to the gate. Because of the thicker metallization of the drain electrode, the source forms a tunneling contact with the drain while maintaining a significant distance from the gate, as shown by Fig. 1(b), thereby creating a nanometer-scale switch. Like a field-effect transistor, this device should exhibit both current and voltage gain. Such a switch, at the dimensions shown in Fig. 1, could switch at several gigahertz with a 1.5 V signal swing.[3]

II. METHODOLOGY

The approach for achieving nanometer scale lines and spaces is outlined in Fig. 2 as would be used to create the gate and drain electrodes of the nanomechanical switch of Fig. 1. A sequence of evaporations is shown, Figs. 2(a)–2(d), performed in a single pump-down cycle of a conventional electron-beam evaporator. Shown in Fig. 2(a) is the side view of a fixed shadow mask mounted over a substrate on which the nanostructure is to be formed. In this example, SiO_2 represents a grown oxide on a silicon wafer. Following each evaporation [Figs. 2(b)–2(d)], the substrate is translated laterally with respect to the shadow mask leaving a set of nanometer, interembedded, in this case metal, features. Note that the shadow mask opening does not determine the size of the feature; the feature size is controlled by the translation of the shadow mask. Materials for evaporation are chosen based on their etch chemistry. The principle is that one metal can be lifted off with respect to the other by selective etching. In this example, aluminum is the lift-off structure for platinum; the Al is removed by etching in $HCl:H_2O$ without attacking the underlying oxide or etching the platinum, leaving a pair of nanometer-scale lines with a controlled difference in height and precise separation, as shown in Fig. 2(d). In this article, we demonstrate the steps shown in Figs. 2(a) and 2(b), and the metal lift-off technique.

Sidewall processing using this technique requires steep side walls. The edge sharpness of the side walls, i.e., the edges of the deposited patterns, is mainly governed by the evaporation geometry as illustrated in Fig. 3. An analysis shows the width of the edge taper, w, of a deposited feature through a stencil mask is approximated by

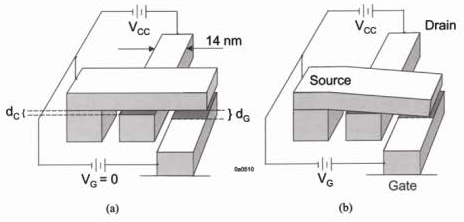

FIG. 1. Vertical nanoelectromechanical switch: (a) Natural open position, and (b) closed position under positive gate bias. As a representative scale, the contact length is chosen to be 14 nm with d_C and d_G of 2 and 4 nm, respectively.

a)Electronic mail: seabaugh.1@nd.edu

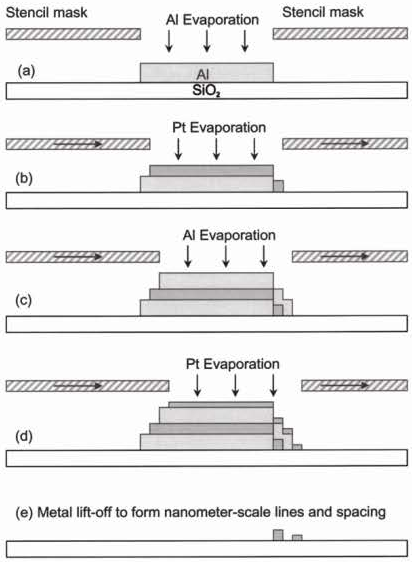

FIG. 2. Formation of nanometer metal wires with nanometer spacings by translating a stencil mask and lift off: (a) Aluminum is evaporated through a stencil mask, (b) the mask is translated by nanometers and platinum is evaporated, in (c) and (d) the process is repeated, followed by (e) where lift off is used to reveal nanometer-scale lines with nanometer spacings. Thickness differences between the two lines are feasible since they are set by the deposition conditions.

$$w \cong \frac{h+t}{H} d, \tag{1}$$

where h is the substrate-to-mask spacing, t is the thickness of the mask, H is the mask-to-evaporation-source distance, and d is the diameter of the molten evaporation source. In order to get sharp side walls, we desire thin masks, large source-to-substrate throw, and a small or collimated evaporation source.

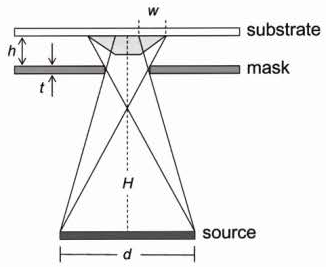

FIG. 3. Factors influencing the sharpness of sidewall features.

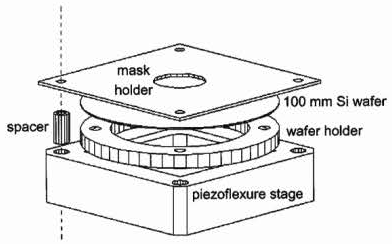

FIG. 4. Fixture assembly for nanotranslated stencil mask and substrate. Parts from top to bottom include: Stencil mask holder, 100 mm Si wafer, wafer holder, spacer, and $x-y$ flexure nanotranslation stage.

III. EXPERIMENT

In this work, the deposition of metals was performed in a commercial Airco/Temescal (Berkeley, CA) FC-1800 electron-beam evaporation system which has a source-to-substrate throw of 50 cm. We used ultrathin masks ($t \leqslant 1\ \mu$m) in contact mode to decrease the term $h+t$ in Eq. (1). In addition, we designed an aperture of 3 mm diameter to reduce the size of the evaporation source. With such a configuration, the expected edge taper, w, is 6 nm, which is tolerable when the resulting lift-off features are tens of nanometers. We note that with a better system configuration, for example, a larger evaporator with longer source-to-substrate distance and better collimation, the feature edge taper width can be reduced to ~1 nm which means that wires on the order of a few nanometers in width are feasible.

The translation of the shadow mask is achieved using a commercial Polytec-PI (Auburn, MA) P-731 flexure $x-y$ nanopositioner with built-in capacitive sensors which operate under closed-loop feedback control. A mask–substrate fixture has been designed constructed, as shown in Fig. 4. A 100 mm wafer was fixed to the wafer holder that is mounted on the flexure portion of the Polytec-PI $x-y$ stage, the mask holder is attached to the fixed portion of the $x-y$ stage via three spacers (one is shown). Through the circular aperture in

FIG. 5. SEM of an Al nanodot produced by depositing through a polyimide membrane mask.

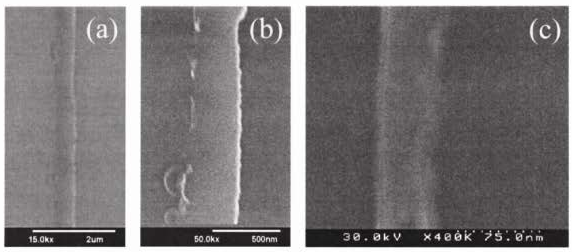

FIG. 6. Wires fabricated by a combination of nanotranslated stencil masks and metal lift-off processing: (a) 330 nm Ti/Pt wire, (b) enlarged portion of (a), and (c) 45 nm Ti/Pt wire.

the center of the mask holder, a stencil mask mounted on an aluminum ring is placed to establish close contact and flatness between the substrate and the mask. Finally, the mask is fixed to the mask holder by silver paste.

Experiments have been carried out using two types of ultrathin masks, a KOH-etched Si rigid mask and a polyimide membrane mask. Rigid masks were fabricated using 10 mil thick double-side-polished silicon wafers with patterned Si_3N_4 and KOH etching. Due to the directional selectivity of Si etching by KOH, a slope of 54.74° is formed, (111) plane, along the openings of the mask. Polyimide membrane masks, with a thickness of approximately 1 μm, were formed by reactive ion etching. These masks are stiff enough to be used in contact mode and the sub-0.5 μm apertures allowed us to observe the effect of hole clogging in stencil masks. With these membrane masks, it is also possible to directly "write" nanofeatures onto the substrate by translating the substrate during evaporation of metals.

IV. RESULTS AND DISCUSSION

The clogging of mask openings by evaporated materials is a common concern when the featuring size is on the nanometer scale.[2] This phenomenon introduces a sidewall slope in the deposited metal which can be compensated for with the translation of the mask relative to the substrate during deposition. We studied this effect by evaporation of metals through nanosized, patterned polyimide membrane masks. Figure 5 shows a scanning electron micrograph (SEM) of a nanodot produced by depositing 300 nm of aluminum onto SiO_2 through a polyimide membrane mask. It can be seen from Fig. 5 that an edge taper results. Based on our experimental geometry for this evaporation, the expected edge taper is about 20 nm. An edge taper of ~55 nm is observed from Fig. 5. The extra 35 nm of taper is introduced by the clogging of the mask opening. The thickness of the evaporated aluminum is 300 nm, the clogging growth rate is about 1/9th of the deposition rate.

Figure 6 shows metal wires formed by the sidewall metal lift-off process of Fig. 2. After the deposition of a 300 nm Al layer, the substrate was translated and a bilayer of 5 nm of Ti and 45 nm of Pt were deposited. The Ti layer served as an adhesion promoter to the SiO_2. Shown in Fig. 6 are two sizes of lines produced after lift off, 320 and 45 nm. It can be seen in Fig. 6(a) that over the extension of several microns, the wire exhibits a good uniformity with an average width of 330 nm and no observable discontinuities. In fact, we found this kind of uniformity over millimeter lengths. Figure 6(b) shows an enlarged portion of the same wire showing some edge roughness. The 45 nm wire shown in Fig. 6(c) shows greater irregularities along the lift-off edge structure with approximately 20 nm of roughness. Since the left-hand side, which is not influenced by the lift-off process, is still straight and smooth, this irregularity can only be attributed to the lift-off process. This may be caused by a tearing off of the top layer Pt during the lift-off process. It may also be introduced by some incomplete material removal as we have observed in regions where the etching is not allowed to complete.

V. CONCLUSIONS

We have outlined a technique to create nanometer scale structures with nanometer spacings with resolution of both wires and spaces set by piezoelectric translation. A sidewall bimetal lift-off process achieved feature sizes as small as 45 nm. Geometrical considerations, namely, source-to-substrate distance, mask-to-substrate distance, mask thickness, and source size, are found to be decisive parameters determining the ultimate smallness. Compensation schemes, such as translational correction, will need to be introduced to address mask clogging and achieve the minimum feature sizes of this technique.

Presented at the 47th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication, Tampa, FL, 27–30 May 2003.

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APPENDIX 6:

IMPINGEMENT OF GAS MOLECULES ON DEPOSITION SURFACES

The presence of a gas ambient in the vacuum chamber can influence the composition and structure of the deposited thin films. For example, Petrov et al. [136] showed that the microstructure and orientation of Al films is a function of oxygen concentration during thermal evaporation. By increasing the background gas concentration, more gas molecules are available at the deposition surface for incorporation or chemical reaction. The following calculations, based on [96], show how a desired hit ratio of the gas molecules versus the deposited molecules can be estimated based on the partial pressure of the background gas and the deposition rate of evaporated material.

The gas impingement flux, Φ, is defined as the number of molecules striking a unit surface area per unit time:

$$\Phi = \frac{PN_A}{\sqrt{2pMRT}} = 1.1\times10^{21}\frac{P_{[\mathrm{Torr}]}}{\sqrt{MT}}\frac{\text{molecules}}{\text{cm}^2\text{s}}, \qquad \text{(A1)}$$

where P is the pressure of the gas in Torrs, M is the molar weight of the gas, R is the universal gas constant, and T is the absolute temperature. The time needed to form a complete monolayer of gas molecules on the surface is determined by the number of surface atoms and how many molecules hit the surface in unit time. The number of

surface atoms can be estimated from bulk densities, and is on the order of 1.5×10^{15} atoms/cm^2, and thus, the time, t_c, for complete coverage is:

$$t_c = \frac{\text{Number of atoms/cm}^2}{\Phi} = 1.36\times10^{-6}\frac{\sqrt{MT}}{P_{[\text{Torr}]}} \text{ s}. \quad \text{(A2)}$$

Using Eqs.(1) and (2), the minimum partial gas pressure required for a given hit ratio (i.e. the number of encounters between surface atoms and gas molecules) can be calculated for a deposition rate.

The monolayer formation time of a metal with an atomic diameter of 2.55Å (e.g. Al), evaporated at a deposition rate of 1 Å/s, is 2.55 seconds. For a 1.5/2 O_2-to-Al hit ratio (the minimum necessary to form stoichiometric Al_2O_3), 0.75 monolayer of O_2 needs to form. For O_2 at 300 K, the complete coverage time is

$$t_c = 1.36\times10^{-6}\frac{\sqrt{0.032\times300}}{P_{[\text{Torr}]}} = 4.2\times10^{-6}\frac{1}{P_{[\text{Torr}]}} \text{ s}.$$

The formation time of 1 monolayer Al must be equal to the formation time of 0.75 monolayer O_2, therefore,

$$0.75\times4.2\times10^{-6}\frac{1}{P_{[\text{Torr}]}} \text{ s} = 2.55 \text{ s} \text{ and } P = \frac{3.15\times10^{-6}}{2.55} = 1.24\times10^{-6}\text{Torr}.$$

Since the number of gas molecules needed to form aluminum oxide increases linearly with increasing deposition rate, necessary ambient pressures for other deposition rates can be easily calculated.

$$P = \text{Deposition Rate in Å/s} \times 1.24 \times 10^{-6}\,\text{Torr}$$

The mean free path of the evaporated atoms is approximately

$$l_{[\text{cm}]} = \frac{5 \times 10^{-3}}{P_{[\text{Torr}]}},$$

which means that up to 80 Å/s (i.e. 100×10^{-6} Torr partial O_2 pressure) deposition rate Al atoms do not collide with O_2 molecules in the vacuum chamber.

APPENDIX 7:

PLATINUM ADHESION TO THERMALLY-OXIDIZED SILICON

In the differential etching of Pt on Al structures, it was observed that although Pt is chemically very resistant, it was removed in HCl and AL-12 etchant.

An optical microscope image of the only Pt feature that remained attached to the substrate after differential etching of structures shown in Figure 10 in hydrochloric acid for 10 minutes at room temperature using ultrasonic agitation is shown in Figure 58.

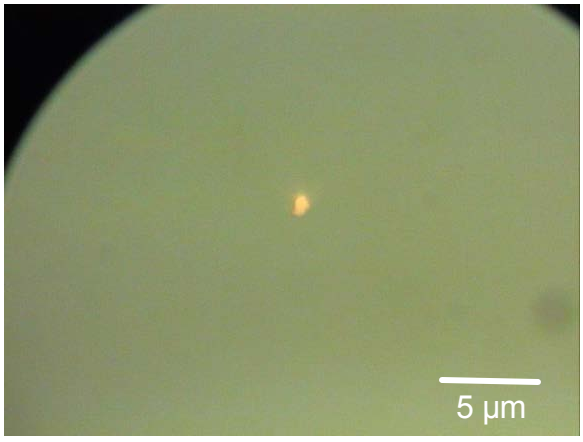

Figure 58. Optical microscope image of the resulting feature after differential etching the structures shown in Figure 10 in hydrochloric acid for 10 minutes at room temperature using ultrasonic agitation.

Based on the SEM images, Figure 10(a) - (d), two approximately 6 μm × 60 μm rectangular Pt features and approximately 3 μm wide Pt lines extending over several hundred microns were expected to be formed after the removal of the Al layers.

The almost complete removal of the Pt features from the SiO_2 surface may be explained by the generally poor adhesion of Pt films to oxide surfaces [137]. For good adhesion, a metal film has to be oxygen active to react chemically with the oxide surface [138], therefore, it is not surprising that Pt, a noble metal, does not adhere to thermally-oxidized silicon.

It is known that an intermediate layer of metal with large heat of oxide formation such as Cr, Mo, Ta, and Ti effectively improves adhesion [139]. Kondo et al. [140] showed that a 100 Å Ti layer inserted between Pt and a $TiO_2/SiO_2/Si$ substrate provides strong adhesion. In later PEN processes the addition of an approximately 100 Å Ti layer successfully improved the adhesion of Pt.

It was also observed that Pt thin films were removed from SiO_2 substrates after being brought into contact with deionized water. Figure 59 is an optical microscope image of a 77 nm Pt thin film layer deposited on SiO_2 after a drop of deionized water was dropped on its top surface.

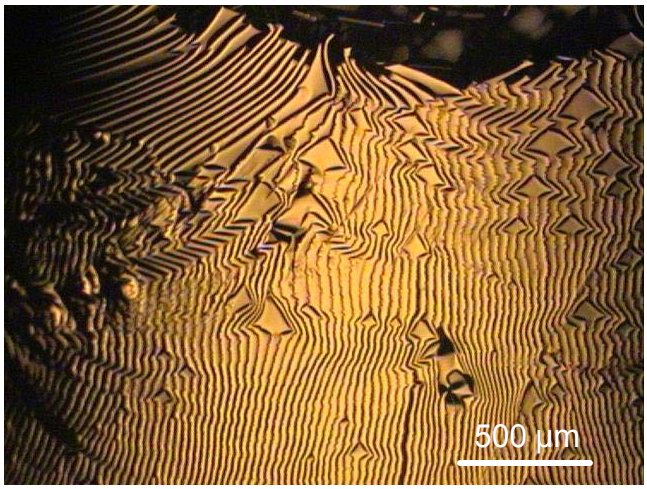

Figure 59. Optical microscope image of stress-release patterns in a 77 nm Pt thin film after a drop of deionized water came into contact with its top surface.

It is interesting to note that the adhesion between the Pt double wires and the oxidized silicon substrate was strong enough to prevent their removal during differential etching even without a Ti adhesion layer. Due to the nanometer-scale dimensions, weaker internal stress builds up in these structures. Smaller lateral size necessarily means smaller stress and appreciable film stress arises after only 10 nm of deposition after which large stresses develop up to a thickness of roughly 60 nm [141]. The dimensions of the Pt double wires (less than 220 nm wide and 22 nm thick) were considerably smaller than the dimensions of the structures shown in Figure 10 (more than 3 µm wide and 33 nm thick) and as a consequence their adhesion may be better. It is in agreement with the adhesion test results by Henderickson et al., who found that Au electrodes deposited on quartz consist of a weakly adhering central area and a strongly adhering narrow rim that was less than 40 nm thick due to shadowing by the deposition mask [142].

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