LOW POWER BISTABLE-BODY TUNNEL SRAM

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by

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I would like to take this opportunity to thank my advisor

CHAPTER 1

INTRODUCTION

Complementary metal-oxide–semiconductor technology (CMOS) scaling has followed Moore's law for more than three decades leading to increase in processing speeds, higher device density and hence larger integrated functionality. However the power dissipation density has increased with increasing clock frequency and transistor subthreshold leakage has increased significantly resulting in static power dissipation comparable to dynamic switching power dissipation. Thus CMOS has emerged as a power-constrained technology [1]. More recently the increase in the processing power has been achieved by architecture level parallelism by using multiple processing cores without increasing clock frequency to avoid increase in switching power dissipation density. The increasing static leakage still remains a formidable challenge for ultra-scaled CMOS particularly in high performance applications. At the same time the size of on-chip embedded cache which primarily has been six-transistor static random access memory (6T SRAM) has increased and occupies more than 40 % of the chip area at 45 nm technology node as seen in Figure 1.1 and is expected to occupy more than 70% of the chip area by 2016 [2]. Thus the static power in on-chip SRAM can dominate the total system power during low switching activity. Moreover since the data in the cache needs to be retained even when the processor sleeps, static leakage cannot be avoided. Thus, in

order to reduce power consumption, SRAM technologies with significantly lower leakage currents are needed.

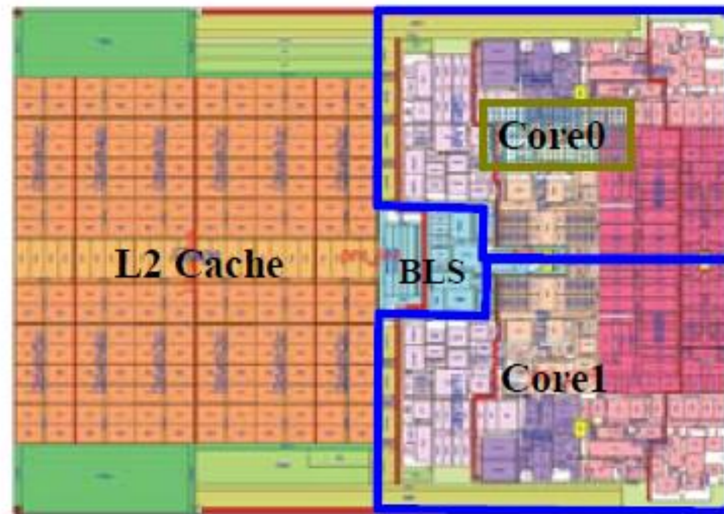


Figure 1.1 Die photo of Intel Penryn processor [3] built using 45 nm high-k metal gate technology showing 50 % of the chip area being occupied by SRAM.

This chapter will give a brief description of conventional 6T CMOS SRAM cell and previously investigated tunnel SRAM (TSRAM). Chapter 2 will explain the proposed bistable-body TSRAM along with detailed working of the cell and simulations results. Chapter 3 describes the possible extensions and new cells based on the concept. Finally, Chapter 4 will give a summary of the work presented and the challenges in practical implementation of the proposed cell.

1.1 6T SRAM:

The conventional 6T SRAM has been the mainstream technology for on chip embedded SRAM. It uses two cross-coupled CMOS inverters in a positive feedback loop as a latch. The data is read and written using pass transistors. Since the SRAM is used for on chip

cache the transistors used are state of the art high performance transistors. The transistors are sized to achieve optimum tradeoff between performance, area, static power, signal-noise margin and stability. Figure 1.2 shows the various components of static power dissipation in a 6T SRAM cell [4]. Since the transistor gate leakage for high-k metal-gate technology is more than two orders of magnitude lower than the transistor subthreshold leakage in off state [5], the static power in 6T SRAM is dominated by transistor subthreshold current.

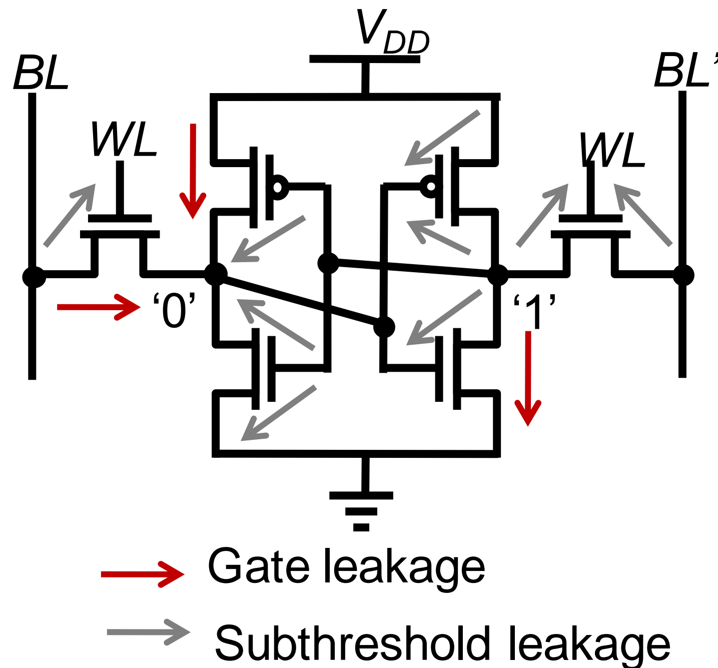
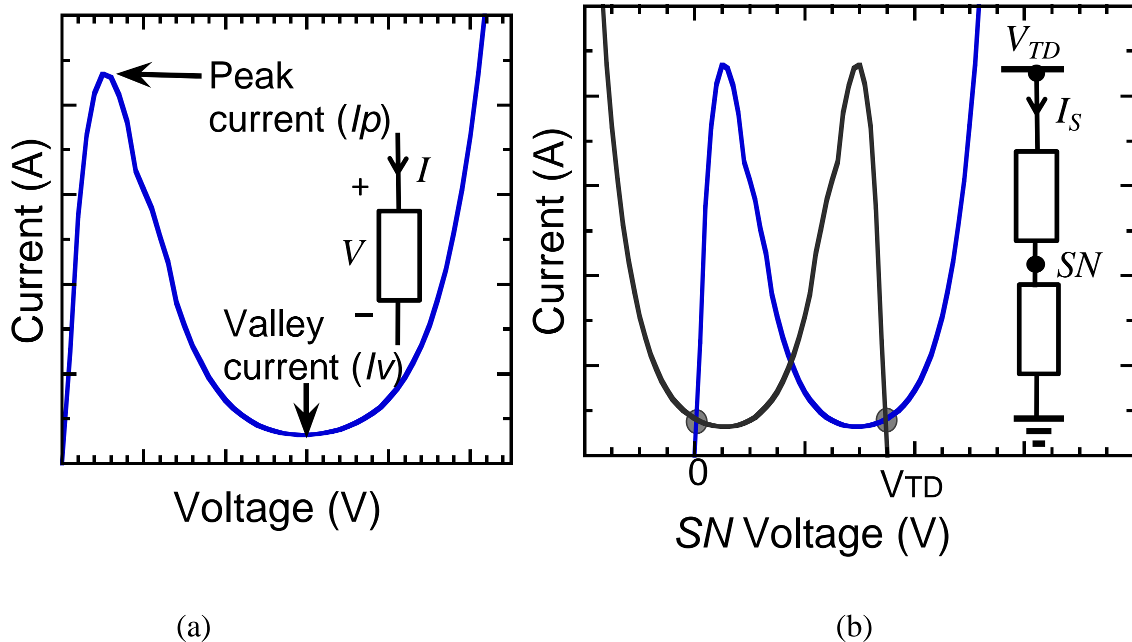


Figure 2.2 Static power dissipation components in 6T SRAM [4]

1.2 Tunneling SRAM prior art:

The use of tunnel diode (TD) negative differential resistance (NDR) for memory applications was first proposed in 1960 [6]. Figure 1.3(a) shows the current-voltage characteristics (I-V) of a generic NDR device and Fig. 1.3(b) shows the load line diagram for two series-connected NDR devices. The gray circles on the load line are stable points.

Thus two-series connected NDR devices can act as a latch with the common node voltage being one of the two stable points on the load line diagram. The NDR devices in the latch can be either a single device or a combination of devices leading to NDR characteristics between two terminals. The most widely investigated NDR element for the NDR latch has been the tunnel diode (TD) as it inherently has NDR characteristics. Also since the TD is a two terminal device a vertical TD can be used resulting in area efficient cell.



(a) (b)

Figure 3.3 (a) Current-voltage characteristics of an NDR device (b) Load line diagram for two series-connected NDR devices.

The TSRAM based on TDs was first proposed by Van der Wagt et al. [1] and the TSRAM cell is shown in Fig 1.4(a). The cell resembles a conventional trench capacitor based dynamic random access memory DRAM cell [7] with the TD latch holding the state of the storage node (SN) capacitor and hence resulting in static operation. During the write operation the pass transistor is turned on to charge the storage capacitor. When the bit line (BL) voltage is high and the on state current of the pass transistor is higher

than the peak current of the TD used the state switches to a high voltage state. When the transistor is turned on and the BL voltage is kept low the capacitor discharges into the BL and the cell is switched to a low voltage state. The state is read by precharging the BL and turning on the pass transistor. During the read operation there is charge sharing between the storage capacitor and the BL leading to a change in the BL voltage which can be sensed. Thus the read operation is destructive and a storage capacitor comparable to the BL capacitance, 40 fF, is needed to cause a significant shift in the BL voltage.

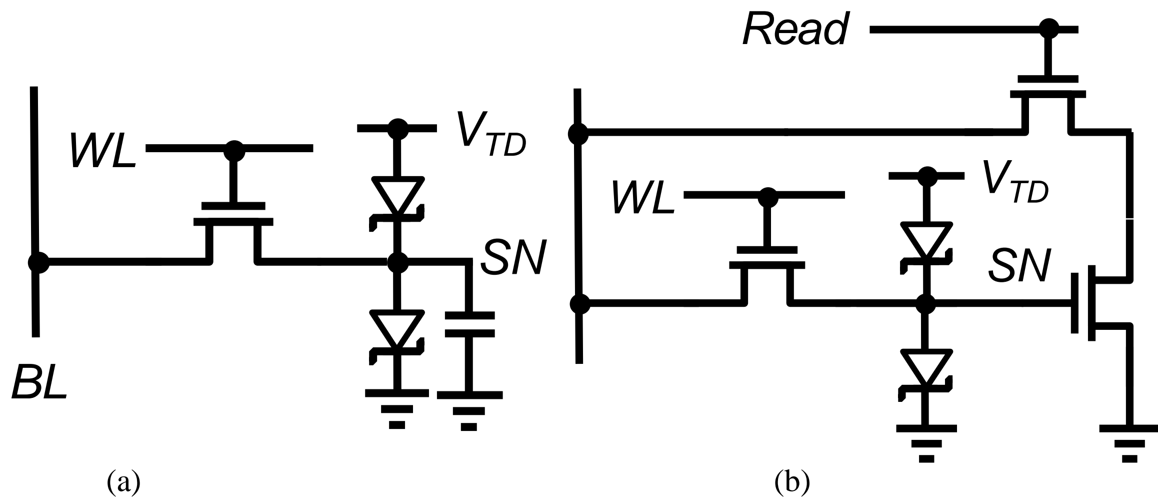


Figure 4.4 (a) Tunnel SRAM (b) Gain cell configuration for tunnel SRAM.

The use of a large storage capacitor requires addition of a DRAM capacitor process to CMOS. The destructive read makes the use of this cell for on-chip embedded SRAM difficult. One possible alternative to this is the three-transistor gain cell TSRAM shown in Fig 1.4(b). In this cell the SN is connected to the gate of a Metal-oxide-semiconductor field-effect transistor (MOSFET) and the data is read using a separate pass transistor. The read current consists of the N-channel MOSFET (NMOS) on-current for high SN voltage and NMOS off-current for the low SN voltage respectively. The write operation

is similar to the one-transistor TSRAM cell. Thus the read is nondestructive and the use of a SN capacitor is eliminated. The gain cell however requires larger area and the TD voltages need to be compatible with transistor gate voltage; thus rules out using arbitrarily low static supply voltage for the TD pair and hence leads to higher static power.

1.3 Power Dissipation

The prior art for TSRAM uses a pass transistor to write the data into the cell. In order for the the TD latch to hold the data at the SN node, the peak current of the TDs needs to be larger than the off-state leakage of the pass transistor which is primarily the thermal subthreshold leakage of the transistor. Also since the transistor leakage needs to be supplied by the TD supply voltage the static current of the cell is greater than subthreshold current of the transistor. As a result the previously investigated Tunnel SRAM cells do not offer an advantage in static power dissipation compared to 6T SRAM and hence the problem of power dissipation density due to high static current in memory cells remains unaddressed.

CHAPTER 2

BISTABLE-BODY TUNNEL SRAM.

2.1 Cell concept

In the bistable-body TSRAM memory cell, Fig. 2.1, charge is stored in the transistor body and held by the bistable TD pair. The body charge shifts the threshold voltage and this is sensed by the resulting change in the MOSFET drain current. The ability to sense this change in the drain current forms the basis for reading the logic state of the cell. In the presence of transistor leakage, the static current through the TDs ensures that the SN potential remains latched to either near 0 V or near the TD bias voltage, V_{TD}.

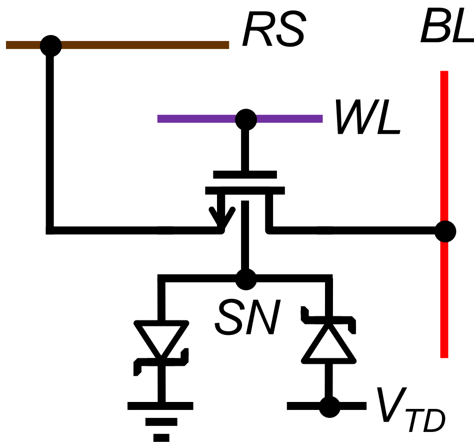


Figure 2.1 Body-biased TSRAM cell consisting of a MOSFET with the body potential held by a tunnel diode bistable latch.

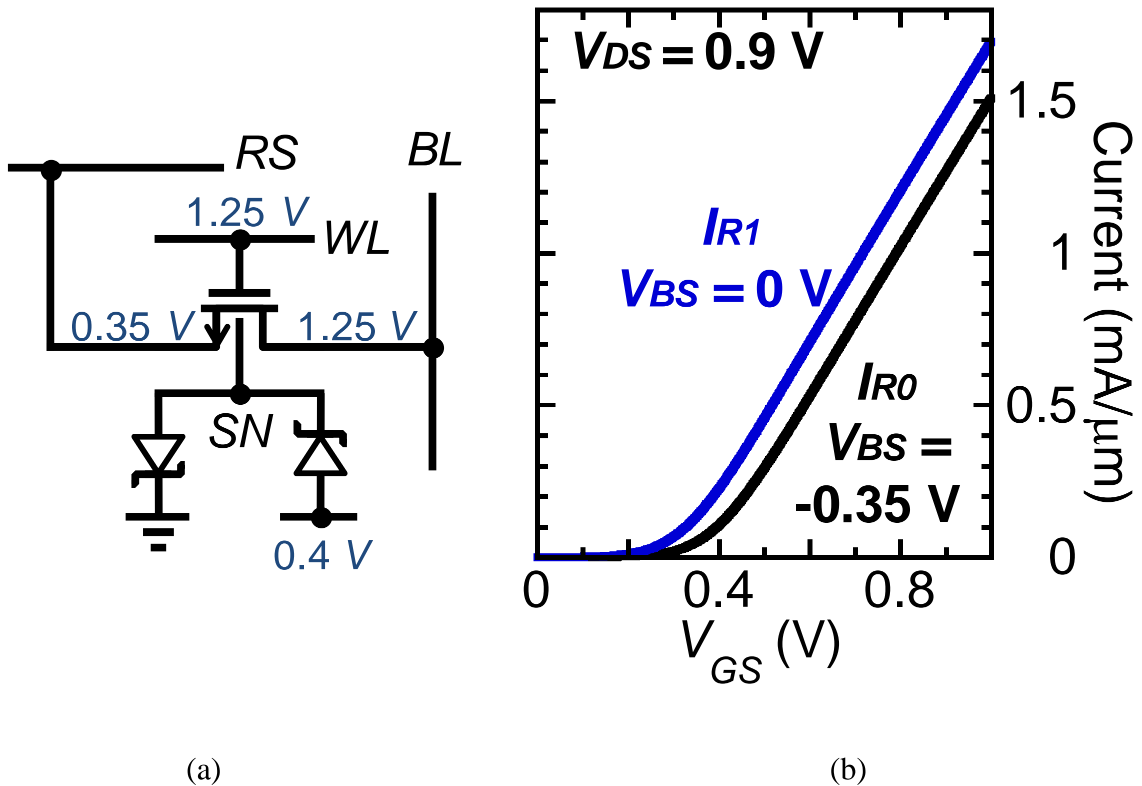
The power dissipation in the body-biased TSRAM cell is lower than in previously investigated TSRAM because the body current of the transistor is orders of magnitude

lower than the subthreshold MOSFET leakage current and allows orders-of-magnitude-lower-leakage TDs to be incorporated.

2.2 Cell operation

A. Read

The read operation is performed by sensing the MOSFET drain current, using the read conditions shown in Fig. 3(a). With the storage node at state zero, the body-to-source voltage is negative resulting in a high threshold voltage and hence low drain current. With the storage node in a "one" state the body-to-source voltage is near zero



(a) (b)

Figure 2.2 (a) Bistable-body TSRAM cell biased during the read operation (b) The read currents are shown for reading state one, I_{R1}, and zero, I_{R0}.

volts resulting in a high drain current. This difference in the drain current is sensed to discriminate the state as shown in Fig. 2.2(b).

B. Reset

In order to write the cell, the storage node needs to be reset to the logic level zero. Since the SN may be at zero or one, a reset must precede every write operation. This is accomplished by forward-biasing the transistor source-to-body or the drain-to-body junctions. The drain-side or bit line cannot be used to discharge the cell because this will discharge all the cells in the column and these would need to be rewritten back in sequence. The source-side or reset (RS) line is a better choice as it is easier to rewrite a word line than it is to rewrite a column. As a result of the reset operation all the cells on the word line are initialized to zero. In this operation the capacitor at the SN is discharged to 0 V with the biases shown in Fig. 2.3. The gate voltage is made negative during the reset to avoid current from the source to the drain.

Figure 2.3 Bistable-body TSRAM cell biased during the reset operation

C. Write logic level one

Gate-induced drain-to-body band-band tunneling current is used to write logic level one into the cell. Figure 2.4 (a) shows the bias conditions which enable band-band tunneling between drain and body to charge the body capacitance at the SN to logic level one. When the band-band tunneling current exceeds the peak current of the TD, the SN potential switches the state to logic level one.

D. Write logic level zero

Figure 2.4 (b) shows the bias conditions for writing a zero. The write zero operation has the same bias conditions as the write one operation except that the drain (BL) is at a low voltage, 0.35 V, during the write cycle. As a result there is no band-band tunneling from drain to body and the storage node remains at 0 V.

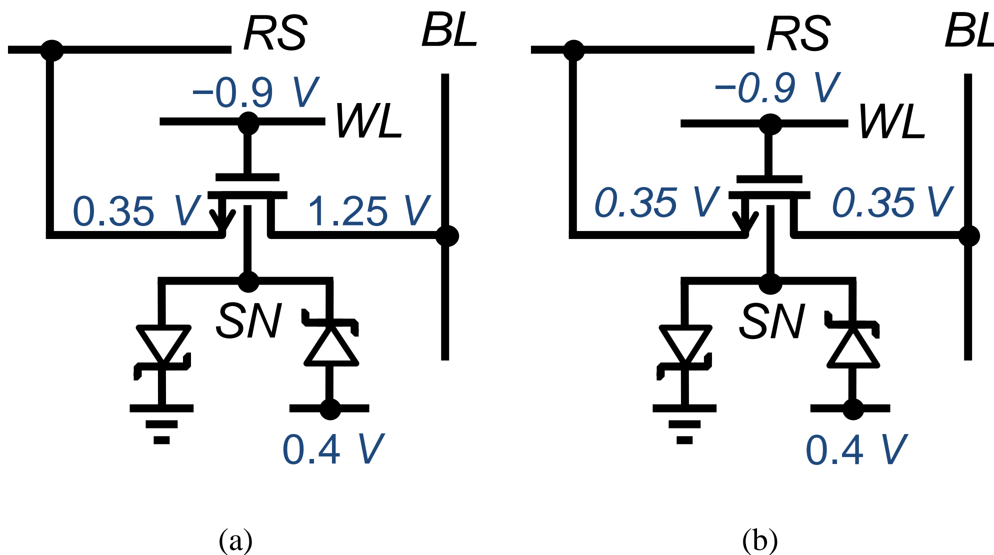


Figure 2.4 (a) Bistable-body TSRAM cell biased during the write one operation and (b) biased during write zero operation.

2.3 Simulation setup and results

A tunnel diode HSPICE model, based on the experimentally demonstrated devices in [8] has been implemented and used in the simulations throughout this work. The model is in excellent agreement with the measured TD characteristics as discussed in the Appendix I. The area of the TDs used in simulations is 32 x 32 nm^2. The ASU 32 nm high performance predictive *n*MOSFET SPICE model [9, 10] is used for the simulation of the cell and is summarized in Appendix II. A 32 nm transistor width is used in all simulations.

Figure 2.5 shows the timing sequence for writing and reading a one. For this sequence, the storage node is initially at a high voltage, 0.35 V.

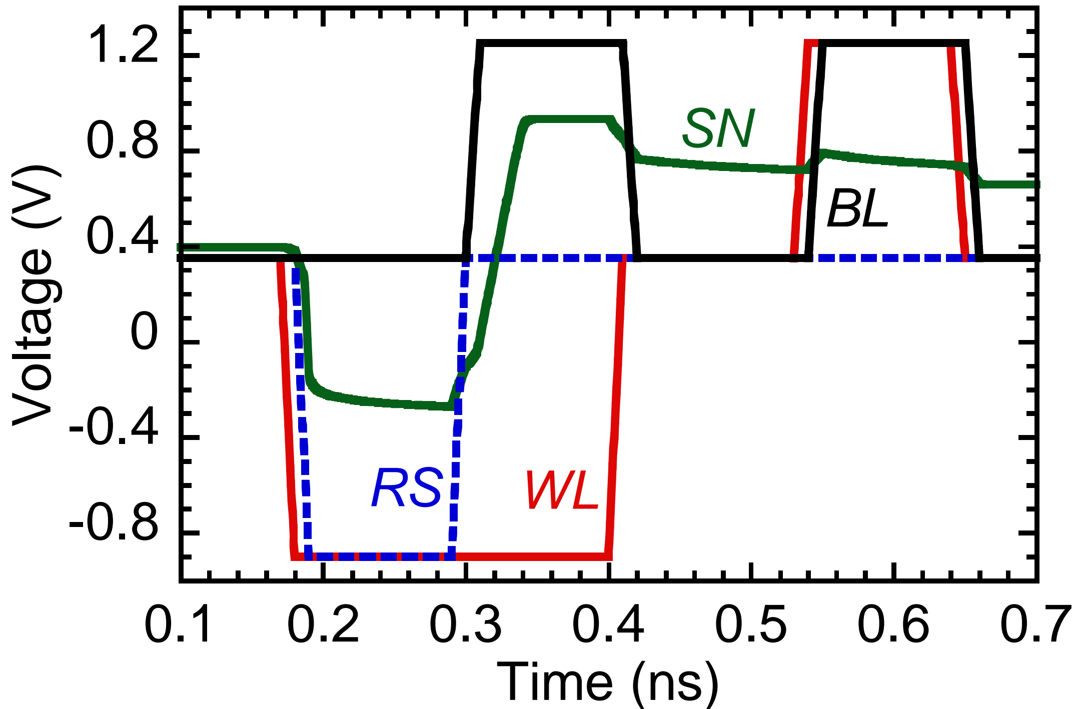


Figure 2.5 Transient simulation of write one operation followed by a read one operation.

The reset operation pulls the storage node low to reset the cell, followed by the write one operation which pulls the storage node high.

Figure 2.6 shows the sequence for writing and reading a zero. The write zero operation has the same timing sequence as the write one operation except that the drain (BL) is at a low voltage, 0.35 V, during the write cycle. The read operation is again shown after the write.

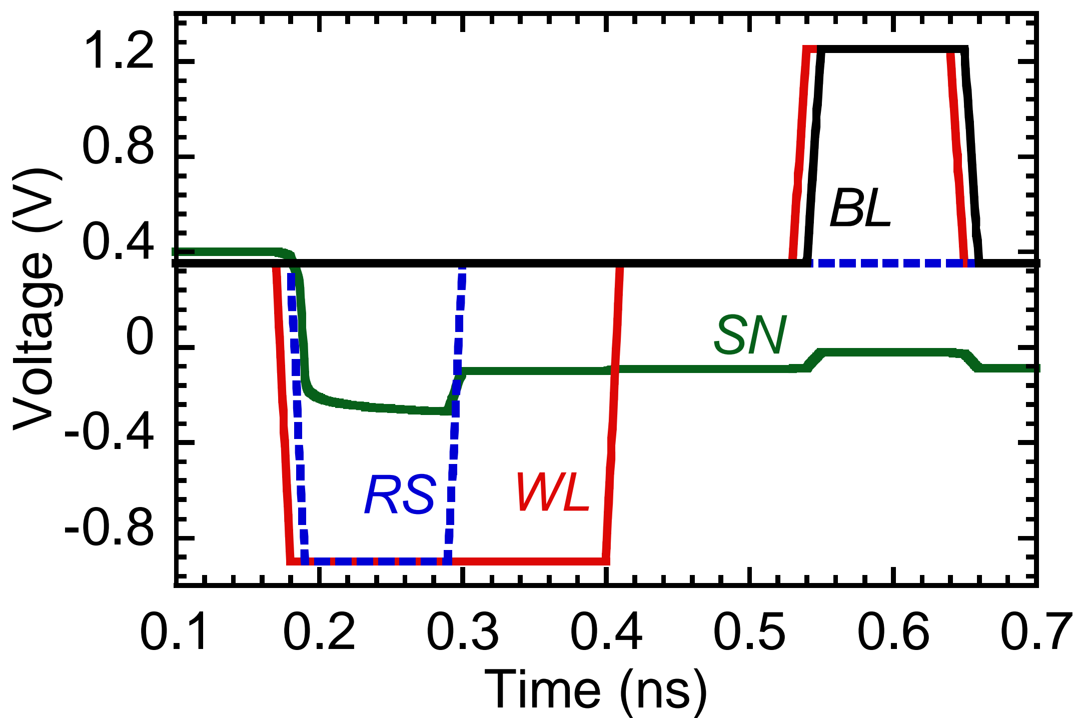


Figure 2.6 Transient simulation of write zero operation followed by a read one operation

As can be seen in Figs. 2.5 and 2.6, the read operation is nondestructive. An overshoot of the SN voltage above the tunnel diode supply voltage during the writing of a one and an undershoot, below 0 V, during the reset operation are not detrimental to functionality. The SN voltage difference between state one and zero is higher during this

transient state and leads to a higher difference between the read current in state one, I_{R1}, and the read current in state zero, I_{R0}. The steady state case I_{R1}/I_{R0} is when the SN has reached V_{TD} (0.4 V) in state one and 0 V in state zero.

The simulation results are summarized in Table 4.1. The cell operation with read and the write pulses of approximately 100 and 200 ps duration. respectively, is shown. The access time of the cell can be comparable to 6T SRAM because the same high performance transistor is used as and the array configuration is similar. The time for the reset operation incurs a time overhead which is less than the write time pulse and hence the maximum penalty due to the reset operation is a factor of 2. For simulations at the 32 nm node, the ratio of the read-one to the read-zero, I_{R1}/I_{R0}, is 1.35, measured at 0.6 ns in Figs. 2.5 and 2.6 when the SN voltage is higher than 0.4 V in state one and lower than 0 V in state zero.. The steady state ratio, I_{R1}/I_{R0}, measured when the voltage in state one has settled to the TD supply voltage and in state zero has settled to zero, is 1.20. A small additional SN node capacitance of 0.15 fF is needed to avoid disturbance of the SN when the bit line switches to write other cells. This capacitance is needed so that the gate-to-body transient leakage during the read operation does not flip the state of the cell. To avoid this disturbance, the read time is restricted to a time given by the ratio of the body charge to the peak transient body leakage during the read operation. For the 32 nm technology, and a SN capacitance of 0.15 fF, this maximum read time is less than 10 ns.

Table 2.1 Bistable-body TSRAM simulation using a 32 nm node Si MOS transistor and low current-density InAlAs/InGaAs tunnel diodes.

Write "1" SN charging time (0 - 0.35 V)	15	ps
Reset SN 0.35 - 0 V discharge time	<10	ps
Static body leakage	0.52	fA
TD static current	0.5	pA
State "0" read current (I_{R0})	32	μA
State "1" read current (I_{R1})	43	μA
I_{R1} / I_{R0}	1.35	
Worst case state "0" read current	32	μA
Worst case state "1" read current	38	μA
Worst case I_{R1} / I_{R0}	1.2	

2.4 Power dissipation

In order for the series TD pair to maintain the state, it is necessary that the peak current in the TDs be higher than the total leakage due to all the static leakage current paths from the SN. Since the SN is connected to the body, the leakage current paths from the SN node are given by the reverse-biased body-to-source current, the body-to-drain current, and the body-to-gate tunneling current. Figure 2.7 shows the currents in the 32 nm node predictive model for the *n*MOSFET as a function of the gate-to-source voltage, V_{GS}. The total static body leakage current (I_{B0}) is seven orders of magnitude lower than the subthreshold leakage (I_{SUB}) current of the MOSFET. The static leakage of the 6T SRAM cell is determined by the subthreshold leakage current of the *n*MOSFET. In the bistable-body TSRAM the static leakage is dictated by the body leakage current, I_{B0}. For this reason, the static current of the bistable-body TSRAM cell can be more more than seven orders of magnitude lower than the static current in a 6T SRAM cell. The static current in the cell simulations reported here does not represent a minimum; higher peak-

to-valley current ratio structures would lower the valley current, I_v, and enable further reduction in static power dissipation.

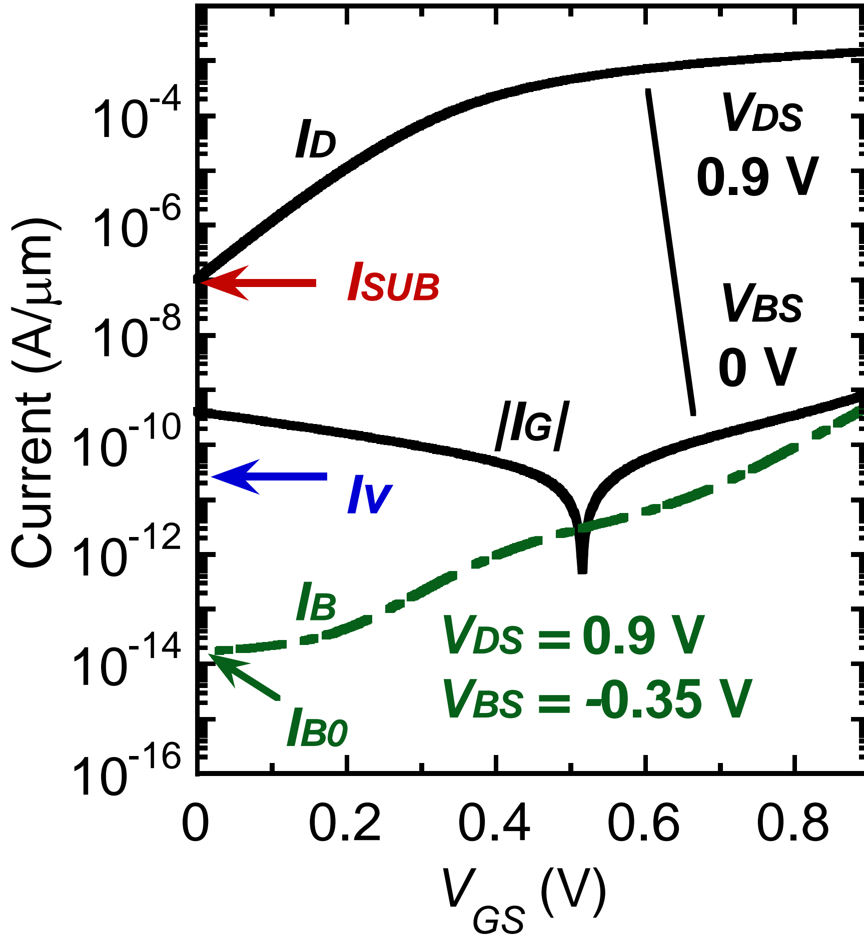


Figure 2.7 Current-voltage relations in the 32 nm node *n*MOSFET ASU high-performance predictive model [8]. For the body current, I_B, measurement, the source voltage is 0.35 V and the body is held to 0 V in order to account for the worst case bias conditions.

The comparison of the static power for 6T SRAM and the proposed cell is shown in Table 4.2. Static current is lower by a factor of more than 24,000, supply voltage is lower by a factor of two, leading to a 55,000x reduction in static power dissipation in the bistable-body TSRAM over the 6T SRAM.

Table 2.2: Comparison of static power dissipation (32 nm node technology).

	6T SRAM	1T-2TD TSRAM
Static current	$2\ I_{SUB}$ [11]	I_V
	206 nA/μm	8.3 pA/μm
Static supply	0.9 V	0.4 V
Static power	185 nW/μm	3.32 pW/μm

2.4 Area

A layout for the bistable-body TSRAM is shown in Fig. 2.8. The spacing between any two lithographic features is equal to the metal half-pitch, F, including the spacing between the contacts. No T-shaped sections are used in the metal interconnects including the gate metal. The area of the cell with 4 metal layers is $48F^2$. The area reported for the 6T SRAM at 32nm node [12] is 0.171 μm^2 and the metal half-pitch used is approximately 56 nm resulting in an effective cell area equal to $54F^2$, thus the area of the bistable-body TSRAM is comparable to that of 6T SRAM.

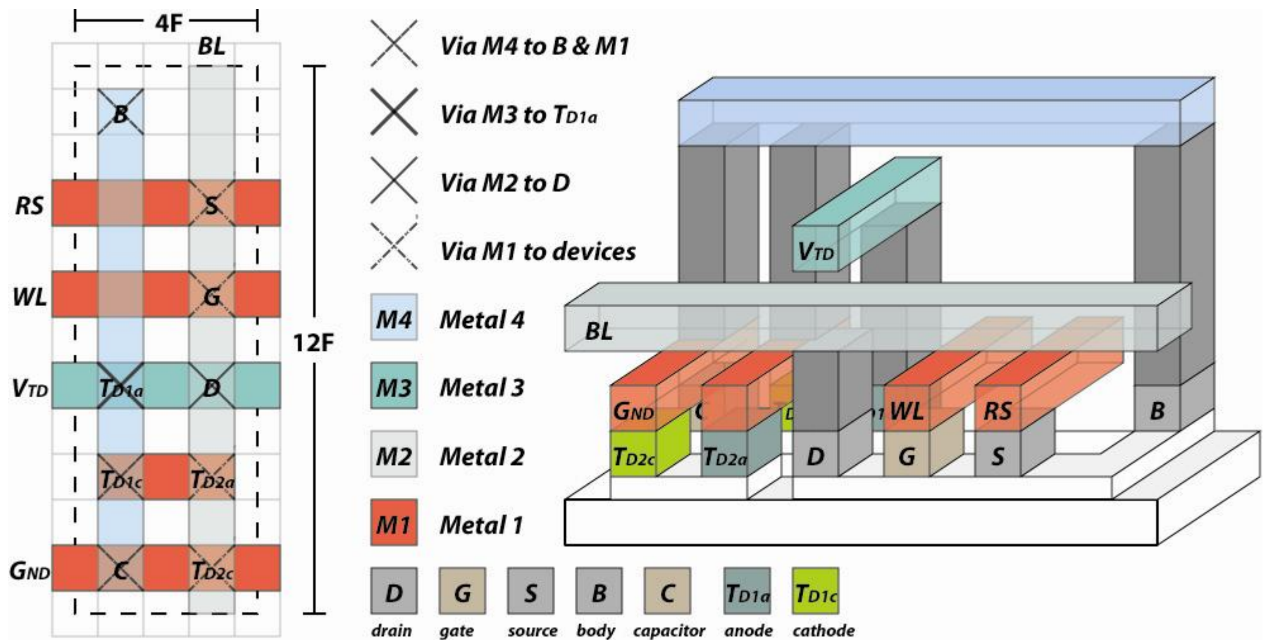


Fig. 2.8: Layout of the bistable-body TSRAM with Metal1 half-pitch F.

2.5 System level considerations

In the bistable-body TSRAM, the ratio of the read current in state one to that in state zero is I_{R0}/I_{R1} = 1.2, when the high state body voltage is 0.35 V. The ratio can be increased to 1.4 if the TD pair is redesigned for operation at 0.9 V. There are other memory technologies like floating body DRAM [13-14] where the change in current between state zero and one can be less than 25% and reliably sensed.

In the proposed cell, a reset operation is required prior to each write on a row basis. This reset before the write operation may be avoided by using a scheme similar to that currently used in floating-body DRAM wherein the capacitive coupling between the gate (WL) and the body of an SOI based transistor is used to selectively discharge cells connected to the bit line [13].

A drawback of the proposed TSRAM cell is the number of distinctive voltages that must be provided on the control lines. Four voltages are needed: -0.9 V, 0 V, 0.35 V and 1.25 V and hence additional supporting circuitry for the SRAM array.

2.5 Process variations

Process induced variations in both transistor and TD characteristics will affect the cell stability, static power, and current sense margin. The TD valley current sets the static current of the cell and hence the static power of the cell increases proportionately with increase in the TD valley current resulting from process variations. The variation in the TD valley current also shifts the stable points on the load line of the series-connected TD pair which in turn can reduce the difference in the SN voltage in the state one and zero. This effect has been analyzed with the TD model used in this work. A 100% increase in the TD valley current shifts the SN voltage by 3 mV for a 0.4 V supply. In the case when the valley currents of both the diodes vary such that the SN voltage in state one and zero are shifted in opposing directions, total 6 mV difference, the SN voltage difference is 1.5%.

The process induced increase in the static body leakage can flip the state of the cell if the static leakage increases to a value more than the peak current of the tunnel diodes.

However the tunnel diodes used in this work have valley current three orders of magnitude higher than the static body leakage as shown in Fig. 6 and hence this process variation poses no limitation.

The threshold voltage variations in the transistor affect the read sense margin as the state is read by sensing the change in the threshold voltage via the drain current. The local variation in threshold voltage σV_t at 32 nm node can be as high as 40 mV [15]. The difference in threshold voltage in the state one and zero in the bistable-body TSRAM is 110 mV. Thus the local threshold variations can reduce the read sense current margin by 37% resulting in effective read zero to read one ratio, I_{R0}/I_{R1}, of 1.13.

CHAPTER 3

FUTURE DIRECTIONS AND CONCLUSION

3.1 Challenges associated with NDR device and potential solution

In the Bistable-body TSRAM memory cell discussed in previous chapter a tunnel diode is used as an NDR element. The use of tunnel diode, a two terminal device gives an advantage in terms of area but there are some challenges associated with use of TD. In particular the maximum ratio of peak to valley current ratio of the TDs demonstrated till date is 144 [16] which is low for variability tolerant memory array. The fabrication process requires addition of epitaxially grown III-V materials with CMOS process. Also the valley current densities are three orders of magnitude higher than the minimum possible valley current densities for the proposed cell. In this chapter a three terminal device structure is which can potentially overcome all the above challenges with a tradeoff in area is proposed and discussed qualitatively.

The device is based on using two three terminal devices in a loop to achieve an NDR characteristics between the two terminals [17]. The previously investigated schemes [17, 18] use a combination of an enhancement mode MOSFET and a depletion based MOSFET as shown in Fig 3.1.

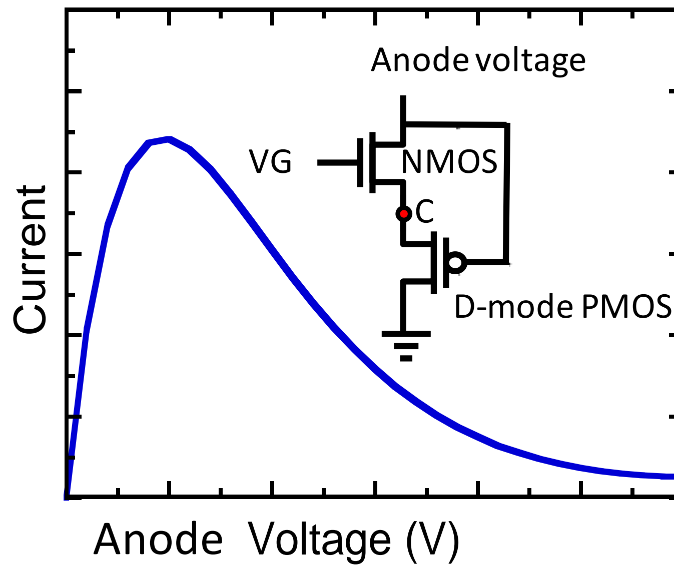


Figure 3.1 NDR behavior using an enhancement mode NMOS and depletion mode PMOS [17]

The gate of the depletion mode PMOS is connected to the drain of the NMOS which acts as the anode terminal for the effective NDR element. The gate of the NMOS is connected to external bias voltage. The source of both NMOS and PMOS are connected together. The threshold voltage and widths of the devices are designed such that at low voltage the net resistance of the pair is dominated by PMOS and hence the drain-to-source voltage drop across the NMOS is lower and the voltage at the source of the NMOS increases with increase in the anode voltage. At low anode voltages the gate voltage of PMOS increases however the PMOS does not turn off as the voltage at the source is increasing as well. As a result the voltage at common node and the current continues to increase until the voltage at the common node reaches the threshold voltage of NMOS. Any further increase in the common node voltage drives the transistor into the subthreshold regime exponentially increasing the NMOS resistance. As a result of conflicting behavior due to

increasing drain voltage and reducing gate to source voltage there exists a regime where the voltage at the common node gets pinned even when the anode voltage is increasing [17,18]. In this regime increase in anode voltage results in depleting of PMOS and reduction in current resulting effectively an NDR behavior between the anode and the cathode.

The off current of the MOSFET dictates the valley current of the combination and thus the valley current is limited by thermal diffusion limited subthreshold current of the MOSFET. Since the cell proposed in the chapter two has static leakage orders of magnitude lower than the transistor subthreshold characteristics the valley current using the previously investigated transistor based NDR elements are much higher than the leakage at the storage node and hence not suitable for Bistable-Body cell.

3.2 Tunnel FET for NDR.

There has been considerable investigation recently to use an electric field-induced inter-band tunneling as a mechanism for a logic switch [19, 20]. The device structure for a Germanium based P-type tunneling field effect transistor (PTFET) [21] along with the energy band diagrams for two different gate to source voltage (V_{GS}) 0 V and – 0.5 V is shown in Fig 3.2. The p-n junction is reverse biased both during the off and on condition and hence the barrier seen by both electrons and holes for thermal diffusion is equal to the bandgap plus the applied bias. This results in a low thermal diffusion current arising primarily from minority carriers and space charge generation recombination current. During the off condition the tunneling distance for the carriers in valence band to tunnel to conduction band is large resulting in low tunneling current. During the on condition

the gate is biased such that the tunneling distance is reduced resulting in exponential increase in tunneling current. Since the the energy barrier seen by the carriers is effectively that of a reverse bias PN junction the thermal subthreshold current is strongly suppressed compared to MOSFET. The motivation for tunnel-FET has been to achieve a steep subthreshold slope to achieve a low off-current. Achieving high on-current as required for high speed logic operations still remains challenging for these devices.

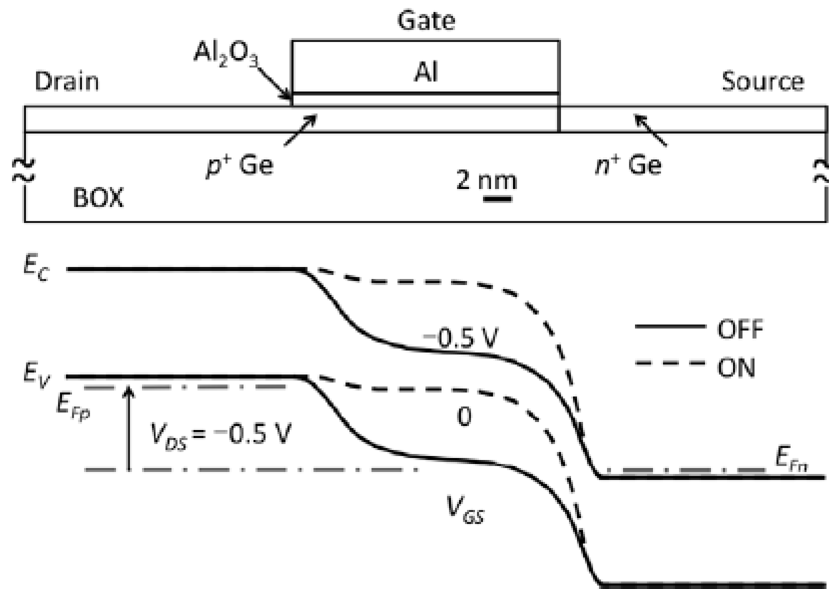


Figure 3.2 P-type Tunnel FET device structure and corresponding band diagram for V_{GS}=0 V and −0.5 V for V_{DS} = −0.5 V [21]

3.3 NDR device using enhancement mode N-MOSFET and P-Tunnel FET.

The proposed device structure is shown in the Fig. 3.3. It consists of an enhancement mode NMOS and the P type Tunnel FET. Since the off state leakage of the PTFET can be orders of magnitude lower than that of PMOS at the same technology node, the valley current, which is dictated by transistor off current can accordingly be

orders of magnitude lower than the previously existing schemes using MOSFET's. The device requirements for the PTFET are lower off current compared to MOSFET and an on-current to off-current ratio of a factor of 1000 or higher. Since the peak current of the NDR device and hence the on current of PTFET is not related to the performance of the memory cell the on current need not be comparable to that of the corresponding MOSFET unlike that required for logic applications of TFET. The bistable body memory cell using the proposed NDR device is shown in Fig 3.3(b). The cell is similar to the bistable body tunnel SRAM using tunnel diodes discussed in chapter two except that the tunnel diode is replaced with the proposed transistor based NDR element. A detailed study is required in future to understand the implications of TFET device characteristics on NDR behavior

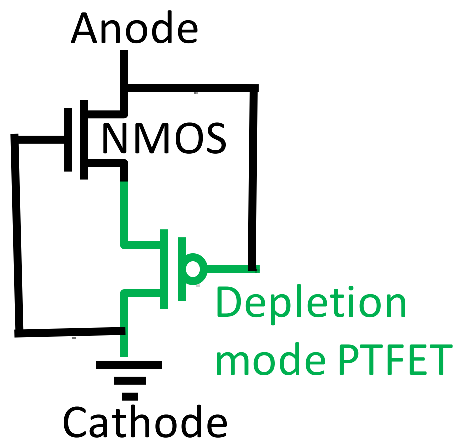


Figure 3.3 NDR device using enhancement mode NMOS and a depletion mode P type Tunnel FET.

3.4 Conclusion

The bistable-body TSRAM is proposed and validated using simulations. The cell using one transistor and two tunnel diodes is a high speed, low power static memory cell, offering over four orders of magnitude reduction in static power compared to the 6T SRAM for the same transistor technology. A layout with cell area equal to $48F^2$ is shown. The speed of the cell is comparable to the 6T SRAM. A possible extension of the work using transistor based NDR element is briefly discussed. Thus the cell is a potential candidate for embedded SRAM in current and future technology generations.

APPENDIX

The transistor model used in the simulations is the ASU predictive model V2.1, 32 nm node, high performance, incorporating stress, high-k and metal gate. The drain current vs. drain-to-source voltage and gate-to-source voltage is shown in Fig. A.1(a) and the frequency response is shown in the Fig. A.1(b).

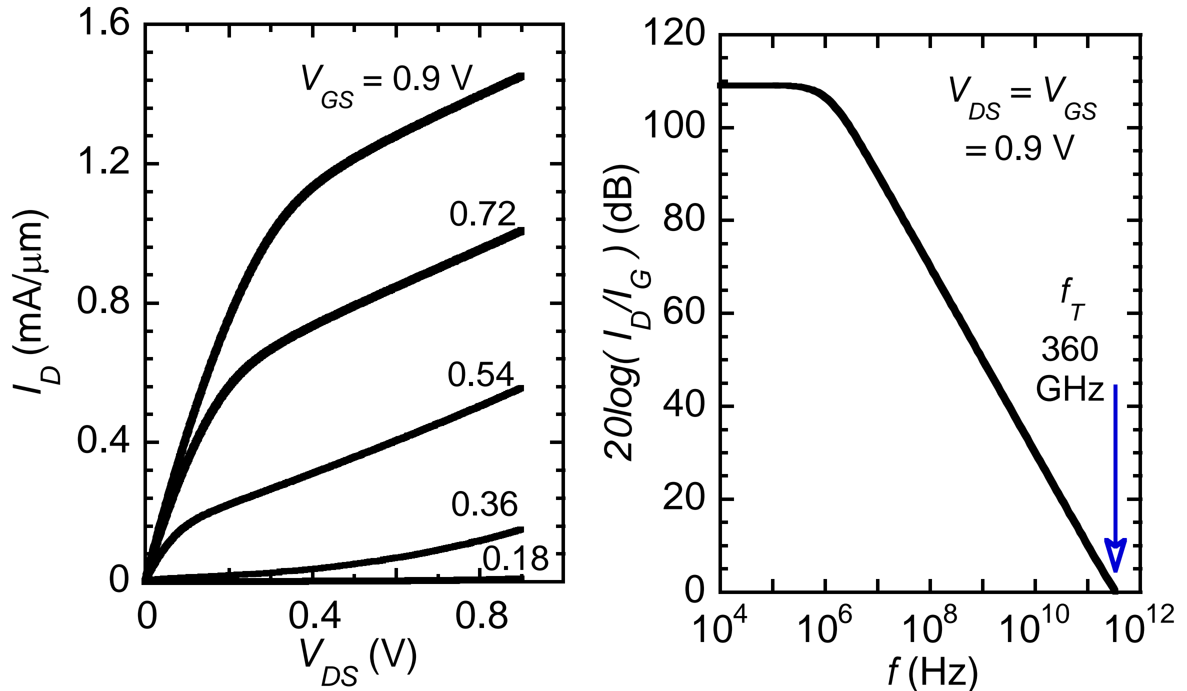


Fig. A.1. (a) Simulated common source transistor characteristics for the 32 nm node nMOSFET used in the simulations of is paper. (b) Simulated short-circuit current gain vs frequency for the same transistor.

The tunnel diode is modeled in SPICE using an analytic relation adapted from [22] to describe the current-voltage behavior. The first term describes the tunneling and negative resistance; the second term describes the diode relation.

$$I = aKV \exp\left(1 - \frac{V}{V_P}\right) + aJ_S \exp\left(\frac{V}{\eta V_T}\right)$$

In a SPICE subcircuit, Eq. (1) is used to describe a voltage-controlled current source. This source is shunted by a depletion capacitance of 8.4 fF/μm^2. This parallel circuit is then connected in series with a resistance of 0.3 Ω/μm^2 and an inductance of 5 fH/μm^2. This model is in excellent agreement with the dc measurements of Fig. A.2 using the parameters shown.

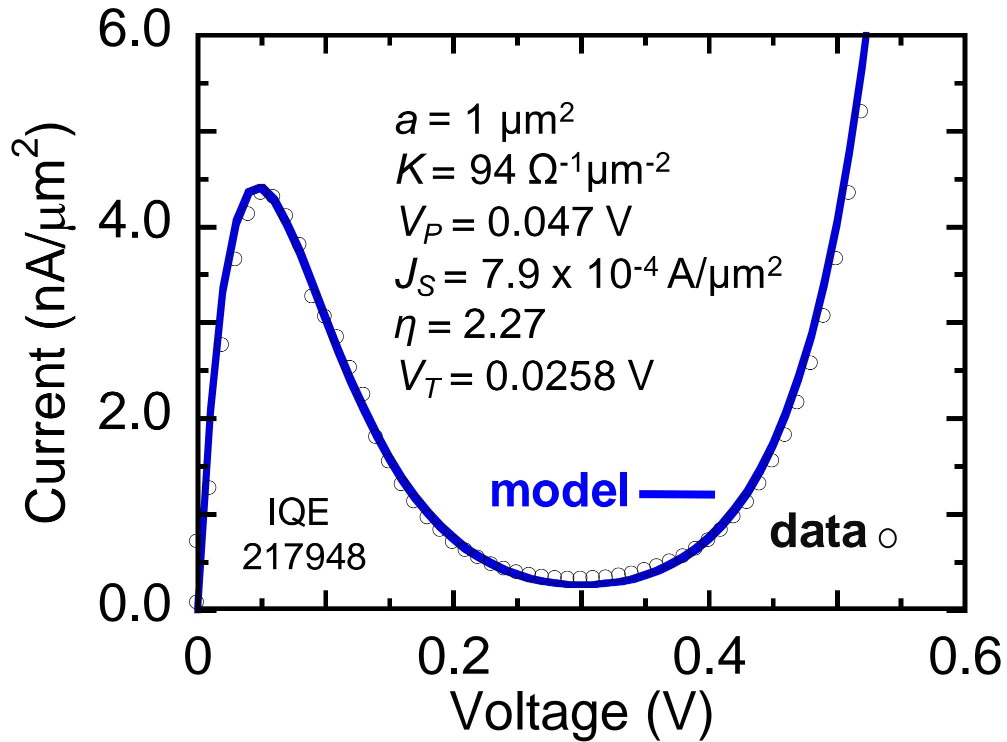


Fig. A.2. Comparison of measured and modeled current voltage characteristics for a *p*+*n*+ InGaAs/InAlAs interband tunnel diode.

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