Sb-BASED HIGH ELECTRON MOBILITY TRANSISTORS:

PROCESSING AND DEVICE CHARACTERIZATION

A Thesis

Submitted to the Graduate School

of the University of Notre Dame

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science in Electrical Engineering

by

Bin Wu, B. E.

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Alan C. Seabaugh, Director

Department of Electrical Engineering

Notre Dame, Indiana

April 2003

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Abstract

by

Bin Wu

A single-metallization process for AlSb/InAs/AlSb high electron mobility transistor (HEMT) fabrication has been demonstrated. The effects of gate metal to channel short-circuiting problem have been observed from the common-source transistor characteristic measurement. One micron gate with threshold voltage V_T of -1.25 V has been achieved by avoiding the gate metal to channel short-circuiting. A low peak extrinsic transconductance g_m of 35 mS/mm has been observed at 0.4 V source to drain bias V_{DS} due to a high source resistance, $R_S = 7.49$ Ω-mm.

Wet oxidation of $Al_{0.8}Ga_{0.2}Sb$ has been performed; surprising data has been shown. Because of the instability and highly reactive nature of AlSb, attempts were made to improve the device isolation by wet oxidizing the AlGaSb mesa floor. Contrary to expected results, the conductivity of the oxidation products increases in orders of magnitude.

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FIGURES

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor Dr. Alan C.

Seabaugh for his constant help and inspiration throughout the course of this project. I

would also to than HRL Laboratories for funding this project under the DARPA

antimonide-based compound semiconductors program.

I would like to thank my groupmates for their discussion and suggestions.

I would also like to thank Michael Thomas, Mark Richmond, Alex Komor, and Tatyana

Orlova for their help.

I would like to thank Dr. P. Fay and Dr. L-E Wernersson for consenting to

be on my committee.

CHAPTER 1

INTRODUCTION

Overview

In this introductory chapter, we review the physics of high electron mobility transistors (HEMTs) and motivate the choice of the InAs/AlSb material system.

1.1   Heterostructures and modulation doping

1.1.1   Heterostructures

A heterojunction is the junction formed between dissimilar semiconductors. Heterojunctions are essential elements in a wide range of devices, including semiconductor lasers, light-emitting diodes (LEDs), heterostructure bipolar transistors (HBTs), high electron mobility transistors (HEMTs) and resonant tunneling diodes (RTDs), *etc.* The development of heterostructure devices is very rapid today, accelerated by a maturing epitaxial growth technology.

When two materials with different energy bandgaps, E_{g1} and E_{g2}, form a heterojunction, the conduction band and valence band of the two semiconductors cannot

both be continuous across the interface. Breaks at the band edges are called conduction

band and valence band discontinuities, ΔE_C and ΔE_V, respectively. There are three

different types of heterojunctions: straddling junctions, staggered junctions, and broken

gap junctions. They are sketched in Figure 1.1, each with a typical material combination.
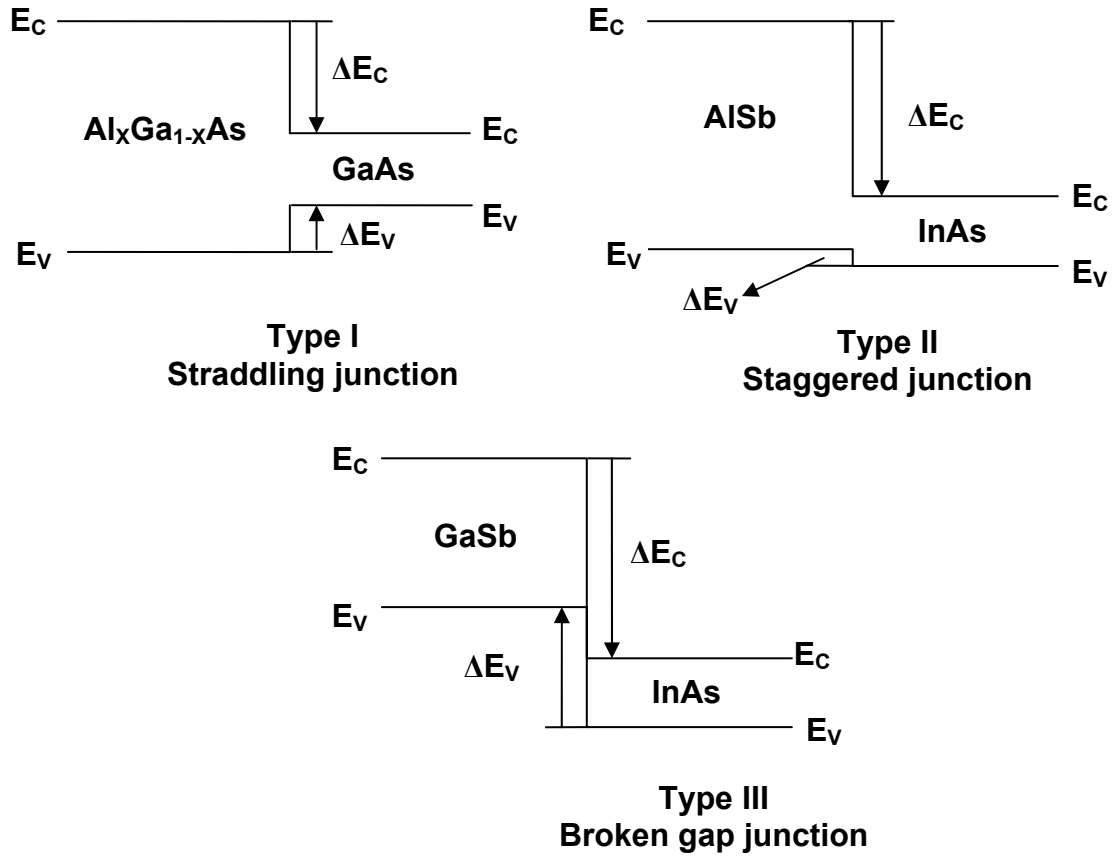
Figure 1.1 Straddling, staggered, and broken gap heterojunctions.

From Figure 1.1, we can see that in the type I, straddling heterojunction,

the sum of ΔE_C and ΔE_V is the bandgap difference, $|E_{g1} - E_{g2}| = \Delta E_g$, between the two

contact semiconductors. While in the type II, staggered heterojunction, ΔE_g is the difference of the two band discontinuities. In type III, broken gap heterojunction, the conduction band minimum of one material lies below valence band maximum of the other. As in the staggered heterojunction, ΔE_g in the broken gap heterojunction case also equals the difference between the two discontinuities. In addition to the energy bandgap and effective mass differences, strain, doping concentrations, and interface charge also contribute to the properties of heterojunctions.

In this work, we utilize the AlSb/InAs/AlSb heterostructure which has a type II staggered junction band lineup. In this structure, conduction electrons are confined in the InAs by a 1.35 eV barrier formed by the conduction band offset between InAs and AlSb, while the valance band holes are unconfined.

1.1.2   Modulation doping

In semiconductors, carrier density and mobility are inversely related; as the carrier concentration increases the mobility decreases due to ionized impurity scattering. For a field-effect transistor, high channel conductivity is wanted, hence both carrier concentration and mobility are important to maximize. Modulation doping (Dingle *et al.* [1], 1978) provides a way to achieve a high concentration channel without the introduction of ionized impurity scattering caused by the dopants; the carriers and the dopants are spatially separated from each other.

Schottky Metal

undoped
AlGaAs

n-AlGaAs

i-GaAs

2-dimensional
electron gas
(2DEG)

SI-GaAs

E_1

E_2

E_F E_C

(a)

(b)
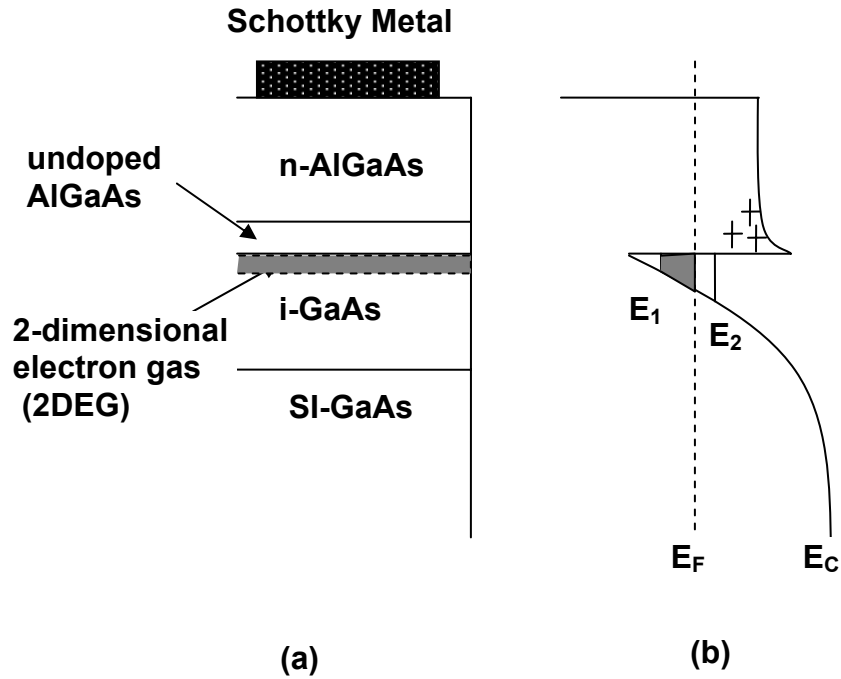
Figure 1.2 Modulation-doped two-dimensional electron gas: (a) layers description and (b)
energy band profile.

The modulation doping concept is illustrated in Figure 1.2. Electrons
transfer from the n-AlGaAs layer to the undoped GaAs layer, accumulate near the
interface, and form a two-dimensional electron gas (2DEG). The AlGaAs layer is
depleted in the vicinity of the heterojunction. In practice, an undoped AlGaAs spacer
layer is inserted between the n-type AlGaAs and GaAs layer [1]. This undoped layer
serves to further separate the ionized donors in the doped AlGaAs layer from the high
concentration 2DEG within the GaAs layer, reducing the ionized impurity scattering, thus
increasing the electron mobility.

1.2   Metal-semiconductor junctions in a HEMT

Metal-semiconductor junctions are essential elements of all semiconductor devices. When a metal-semiconductor Schottky junction is formed, a depletion region forms in the semiconductor. An applied voltage changes the width of the depletion region. A metal-semiconductor ohmic contact is purely resistive; the current through the contact is linearly proportional to the voltage across it.

In the HEMT, a rectifying Schottky gate contact changes the channel conductivity to control the current flowing from the source to the drain, while for the drain and source contacts, linear low resistance ohmic contacts are required. Non-ideal ohmic contacts reduce the extrinsic transconductance of the HEMT.

1.3   Compound semiconductor HEMTs

The high electron mobility transistor (HEMT) is also known by other names, including heterostructure field-effect transistor (HFET) or modulation-doped-field-effect transistor (MODFET). Figure 1.3 shows the typical HEMT structure examined in this work. In a HEMT, the contact between the gate metal and the semiconductor material under it is a Schottky contact. It forms a depletion region in the layers above the channel layer, under the gate electrode. The width of the depletion region can be changed by the voltage applied to the gate. When the depletion region expands to the bottom of the channel, the output drain current is turned off.
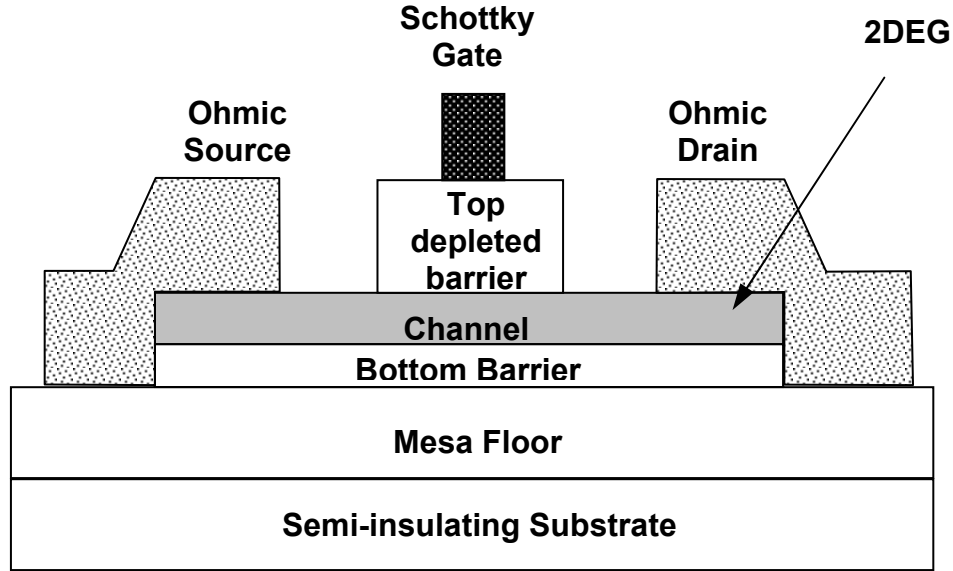
Figure 1.3 A typical HEMT structure in this work. A two-dimensional electron gas is formed in the channel layer.

Figure 1.4 is the calculated energy band diagram of the typical heterostructure used in this work. The Schottky barrier height between Ti and InAlAs is ~ 0.6 eV [2]. The Be sheet charge has a density of 8×10^{11} cm^{-2}, separated from the channel by a 6.5 nm undoped AlSb spacer. The computed first energy state, E_0, in the InAs quantum well is approximately 7 meV below the Fermi level, E_F; a 2DEG with a concentration of 9×10^{11} cm^{-2} is formed in the channel at zero gate voltage.
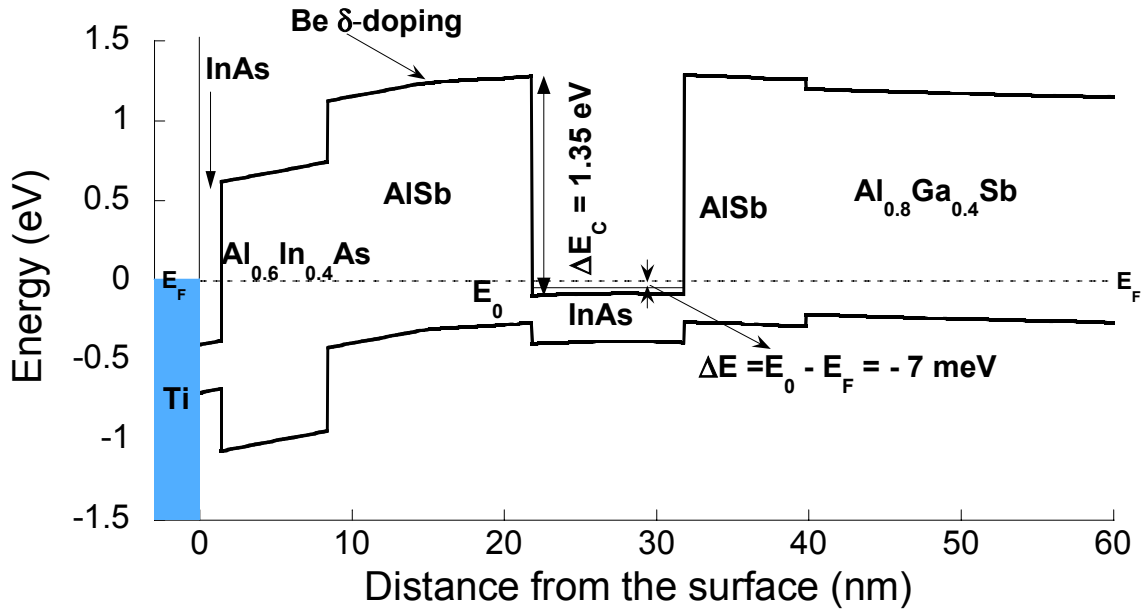
Figure 1.4 Energy band diagram of an InAs/AlSb HEMT. The channel is modulation doped with Be acceptors in the top AlSb barrier to raise the threshold voltage. This simulation was done using the Poisson-Schrödinger Solver BandProf of W. R. Frensley.

Today, most FETs are made on silicon. But with the rapid growth of the telecommunication industry, the demand for high-speed compound semiconductor FETs has increased significantly. The high electron mobility and peak velocity of direct gap compound semiconductors and the band gap engineering options in these materials make them highly attractive for the fabrication of high speed devices. The combination of advantages, including advantages, the high mobility and the high peak velocity of electrons in the InAs layer and the high AlSb/InAs conduction band offset, makes the InAs/AlSb material system attractive for exploring high frequency, low power transistors. TABLE 1.1 summarizes the bulk electronic properties of selected semiconductors.

TABLE 1.1

PROPERTIES OF IMPORTANT ELEMENTS AND BINARY SEMICONDUCTORS[A]

Material	Bandgap (eV)	Mobility (cm^2/V-s)		Transition type[B]	Γ-L Valley Separation[H] (eV)	Effective Mass m_Γ*/m_0		Electron Drift Velocity (10^{7}cm/s)
		Electron	Hole			Electron[C]	Hole[D]	
Si	1.124	1450	505	I		0.92/0.19	0.54/0.15	~ 1[E]
Ge	0.66	3900	1800	I		1.57/0.082	0.28/0.04	
AlAs	2.15	294	N/A	I		1.1/0.19	0.41/0.15	
AlSb	1.61	200	400	I		1.8/0.26	0.33/0.12	
GaAs	1.424	9200	320	D	0.31	0.063	0.50/0.076	1.8[F]
GaN	3.44	440	130	D		0.22	0.96	2.5[A]
GaSb	0.75	3750	680	D		0.0412	0.28/0.05	
InAs	0.353	33000	450	D	0.9	0.021	0.35/0.026	3.5[F]
InP	1.34	5900	150	D	0.53	0.079	0.56/0.12	2.4[F]
InSb	0.17	77000	850	D		0.0136	0.34/0.016	6.1[G]

[A] From Sze [3] except where otherwise indicated
[B] I, indirect; D, direct
[C] Longitudinal/transverse effective mass for ellipsoidal constant energy surfaces
[D] Heavy-hole/light-hole effective mass for degenerate valence band
[E] Saturated electron velocity [4]
[F] Peak electron velocity [4]
[G] Saturated electron velocity [5]
[H] J. B. Boos *et al* [6]

1.4   InAs/AlSb HEMTs

1.4.1   Advantages of the InAs/AlSb material system

Figure 1.5 shows the bandgaps versus lattice constants of cubic III-V materials.
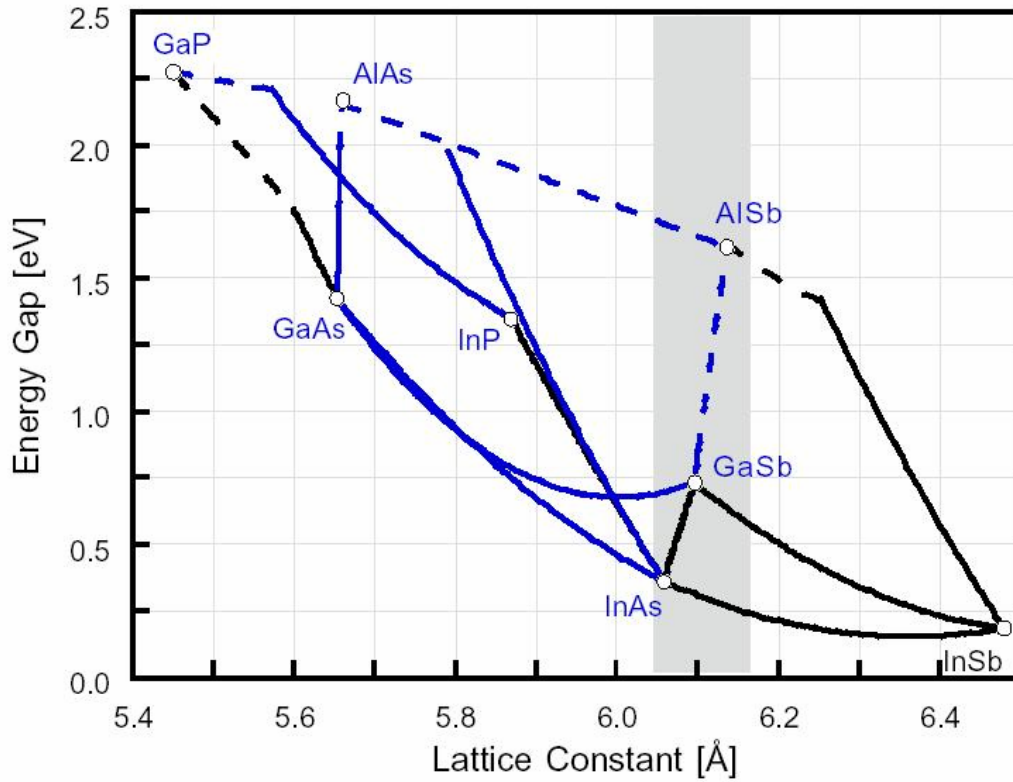
Figure 1.5 Energy gap vs. lattice constant of III-V compound semiconductor of most interest. The grey stripe is to highlight the 6.1Å family. The Figure is reproduced from Bolognesi [7].

In the gray area, AlSb, GaSb, and InAs are nearly lattice matched to a 6.1Å lattice constant. High-quality binary InAs layers can readily be grown on (Ga,Al)Sb

alloys. In the mid-1980's, Kroemer started the investigation of the growth and transport properties of InAs/AlSb quantum wells (QWs) for HEMTs at the University of California, Santa Barbara. He inferred, using the transitivity postulate [8], that the nearly lattice-matched InAs/AlSb QWs should feature a very large conduction band discontinuity. This conduction band discontinuity, ΔE_C, was later measured experimentally by Nakagawa *et al.* [8] to be ~ 1.35 eV which is indeed the largest conduction band discontinuity for any binary III-V system [7]. Dandrea et al. [9] theoretically showed that there is a strain-induced bandgap narrowing in InAs due to the 1.6% lattice mismatch between AlSb and InAs. This causes a valence band discontinuity of ~ 0.04 - 0.10 eV. The above band offsets lead to a staggered (type II) band diagram for the QWs. The band alignment of an InAs channel clad by AlSb barriers is show in Fig. 1.6.
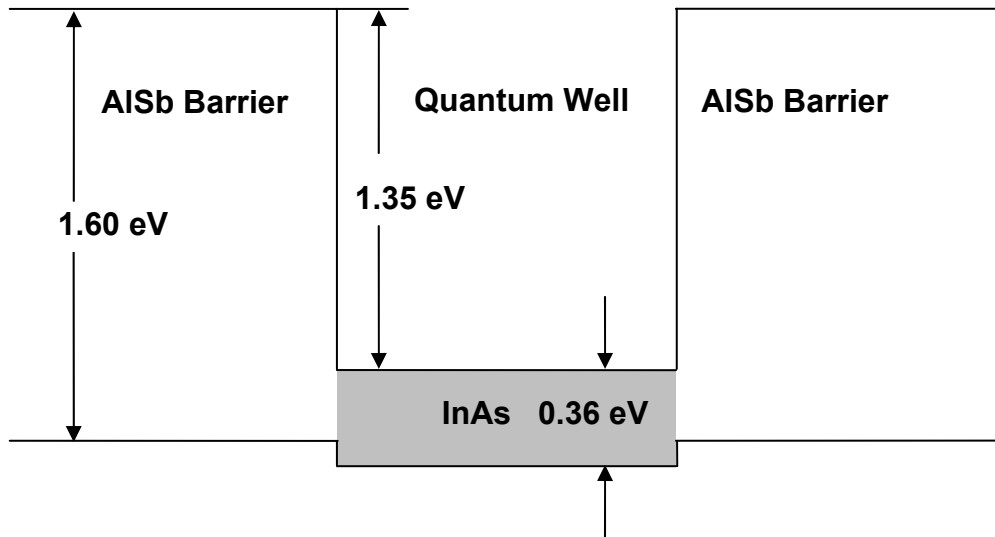
Figure 1.6 Energy band diagram of an AlSb/InAs/AlSb heterostructure.

The excellent electron confinement supplied by the deep AlSb/InAs/AlSb QW and the high electron mobility of InAs at room temperature make for an appealing material system for HEMT development. Mobilities of 20,200 - 30,000 cm^2/V-s in a 100 Å QW have been measured by Brown and coworkers for the materials used in this work [10].

1.4.2   Special considerations in the InAs/AlSb material system

Aluminum antimonide easily oxidizes in the air and unprotected AlSb can degrade and flake off the wafer if left exposed to air for appreciable amounts of time, AlSb also etches easily in alkaline solutions compared to most binary and compound semiconductors. Common photolithographic developers are alkaline, so the unintended etching of AlSb must be taken into consideration during the etching processes [11]

Impact ionization in the narrow band gap InAs of ~0.36 eV channel can lead to undesirable current increases, kinks, in the common-source transistor characteristic. According to Kunihiro, *et al.* [12], traps in the AlSb buffer layer may interact with impact-generated holes to further amplify the already increased output conductance. Gate leakage current is also increased due to the accumulation of impact ionization generated holes in the AlSb buffer layers. Although the type II band lineup of AlSb/InAs/AlSb heterojunctions supplies a deep quantum well for the electrons, it leaves holes without confinement. The lack of hole confinement in InAs/AlSb quantum wells increases gate leakage current when some of the holes generated by impact ionization are drawn into the negatively biased gate.

There is no lattice matched insulating substrate for the 6.1 Å family. For this reason, high-speed HEMTs base on this material system are grown on GaAs or InP substrates with buffer layers to transition to the 6.1 Å lattice constant.

1.4.3   Current status of InAs/AlSb HEMTs

Despite the current immaturity of AlSb/InAs/AlSb HEMTs, considerable progress has been made in the last two decades. A source to drain current I_{DS} of 750 mA/mm and g_m of above 1.1 S/mm has been achieved with a 0.5 μm long gate by Brar *et al.* [13]. This work also reported a 0.25 μm gate-length device showing cutoff frequency f_T of 120 GH_Z and f_{max} of 100 GH_Z at drain voltages below 0.4 V. For enhancement-mode HEMTs, significant achievements have been published by Zhao et al [14], showing high extrinsic transconductance of 425 mS/mm for $V_{DS} = 0.8$ V. Naval Research Laboratories have many publications on InAs/AlSb HEMTs [15] − [20]. From a high-speed point of view, the effective channel velocity of 4×10^7 cm/s InAs makes the InAs-based transistors highly attractive.

1.5   Scope of this work

The goal of this research work has been to explore fabrication processes for InAs/AlSb HEMTs. Because of the instability and highly active chemical property of AlSb, attention has been focused on chemical etch processes for a single-metallization device process. We have also tried to wet oxidize the AlGaSb mesa floor, intending to get

a more stable surface to enhance the device isolation and prevent the underlying AlSb buffer layer from being oxidized. To our surprise we have found that oxidized AlGaSb is conductive.

In Chapter 2, we discuss our fabrication process for the InAs/AlSb HEMTs. The DC characteristics of the HEMTs fabricated in this work are reported and analyzed.

Chapter 3 shows the results of our wet oxidation experiments on the AlGaSb. The unexpected electrical property after oxidation motivates further study. The conclusions are given in Chapter 4 and future research directions on InAs/AlSb-based HEMTs are outlined. Appendices are included, which detail the step-by-step device process and the mask layout.

CHAPTER 2

InAs/AlSb-based HEMT FABRICATION

Overview

  In order to fabricate high performance devices, it is important to develop a reliable and reproducible process. For this study, we have laid out a mask suitable for both DC and RF measurement.

  In this chapter, we present both InAs/AlSb HEMT processing results and device characterization. First, the epitaxial structure of the wafer used in this work is described and the function of each layer is discussed. Then the detailed device fabrication procedure with one-step metallization is demonstrated, including a successful optical lithography process to get 1 μm gates by lift-off. The process traveler is included, Appendix A.

2.1   Epitaxial structure of InAs/AlSb HEMTs

The wafers we are using in this work were grown by Dr. Brown and coworkers in the School of Electrical and Computer Engineering, Georgia Institute of Technology. The epitaxial growth is by molecular beam epitaxy (MBE) on (100) GaAs substrates. Figure 2.1 shows the cross section of the epitaxial layers.
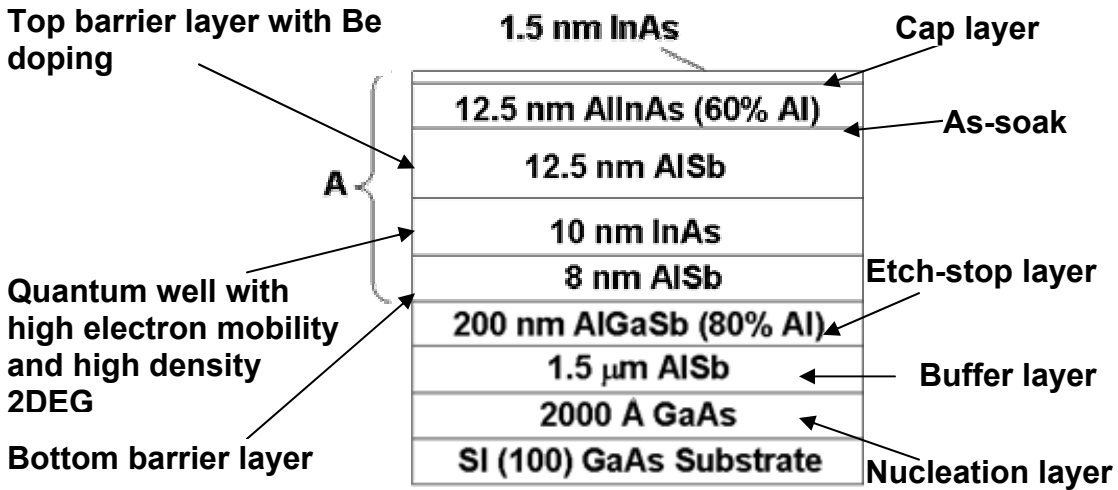
Figure 2.1 Epitaxial structure of HEMT wafer (part A is drawn to scale).

There is a 7% lattice mismatch between semi-insulating (SI) GaAs substrate with a lattice constant of 5.65 Å, and the 6.1 Å lattice constant desired for the device layers. To make the transition in lattice constant, a 200 nm GaAs buffer layer is first grown on the bare substrate before starting the AlSb growth. This buffer layer improves the run-to-run reproducibility of InAs/AlSb QWs grown subsequently [21]. The thick 1.5 μm AlSb layer acts as a strain-relaxed buffer to reduce the strain caused by the

7% lattice mismatch [22]. This mismatch introduces a high dislocation density at the beginning of the growth, and results in a threading dislocation density of $\sim 10^{7}$ cm^{-2} in the thick AlSb buffer layers[11]. With this thick AlSb buffer layer, a high mobility of 20,000-30,000 cm^{2}/V-s at 300 K with a electron sheet density of $\sim 10^{12}$ cm^{-2} has been achieved in the AlSb/InAs/AlSb system grown on the GaAs substrate. The mobility can even increase to 300,000 cm^{2}/V-s at low temperatures, < 10 K [11].

Above the AlSb buffer layer is 200 nm of $Al_xGa_{1-x}Sb$. Here the mole fraction x, is approximately 0.8. AlSb oxidizes easily in air, and the oxidation results in an increased volume. The oxidized surface has a rough morphology, tending to flake and crack [5]. The AlGaSb serves as a chemically-stable etch-stop layer and acts as the mesa floor in the device. The mole fraction of Al, < 90 %, makes the ternary alloy significantly less susceptible to oxidation than the highly reactive AlSb [11]. The etching selectivity between the AlSb and the AlGaSb is enough for etches to stop in the etch-stop layer. Hence, the AlGaSb protects the underlying AlSb buffer layer from oxidation.

The layers labeled "A" in Figure 2.1 comprise the active device region, including an 8 nm thick AlSb bottom barrier, a 10 nm thick InAs channel, and a 12.5 nm thick AlSb top barrier. A Be p-type δ-doping layer is inserted in the top AlSb barrier to raise the threshold voltage of the device. The Be doping density and the thickness of the spacer layer was varied to explore the dependence of channel concentration and electron mobility on Be. The Be sheet charge serves to compensate the intrinsic barrier donors and bend the bands upwards in the barrier [14]. The top barrier layer is followed by an $Al_xIn_{1-x}As$ (60 % Al) layer which is intended to lower the gate leakage by increasing the valence

band barrier between the channel and the gate electrode [13], which is shown in Figure 1.4. At the interface of the top AlSb barrier layer and the AlInAs layer, the AlSb layer usually contains a short-period lattice-matched Al(As, Sb) digital alloy barriers which improve the barrier for holes [21] to further reduce the gate leakage current; the additional arsenic lowers the valence band edge, building a barrier to block the hole transport towards the surface [11]. Finally, an InAs cap layer is grown to protect the underlying layer from oxidation. The Be sheet charge and the InAs cap layer increase the surface barrier with the intent of making an enhancement-mode device [14].

2.2   Device fabrication process

2.2.1   Etchants for InAs/AlSb heterostructures

In the search for a suitable etchants for InAs/AlSb-based HEMTs fabrication, different chemical wet etchants have been studied. Etchants suitable for using in HEMTs fabrication are summarized in TABLE 2.1 with the etching speed and selectivities between InAs and AlSb.

TABLE 2.1
IMPORTANT CHEMICAL WET ETCHANTS FOR InAs/AlSb-BASED HEMTs

Solution (volume ratio unless specified)	Selectivity	InAs (Å/s)	AlSb (Å/s)	Comment
NH_3OH: H_2O (1:5)	Selective		5	Etches AZ5214-E photoresist
HF: H_2O (1:700)	> 10000	<0.01	> 100	Etches AlSb very fast
Acetic acid: H_2O_2: H_2O (5: 10: 100)	> 1000	25	< 0.025	Suitable for channel undercut etch
Citric acid-based solution	~ 2.5	10	~ 4	Slow etchant for AlSb
AZ327 MIF (no dilution required)	> 300	< 0.01	~30	Hard bake of photoresist is recommended before etching
Tartaric acid: H_3PO_4: H_2O_2: H_2O (5: 10: 6: 50)	N/A	> 100	> 100	N/A

In TABLE 2.1, the best etchant for etching AlSb that we have found is the

AZ327 MIF developer. It etches AlSb in a moderate rate (3 nm/s) and has a rather high

selectivity over InAs (exceeding 300). This developer does not attack unexposed or

reverse-baked photoresist. Because it is a photoresist developer, the sample is exposed to

it for at least three times during a complete fabrication process: channel etching, mesa

isolation and metal deposition. The etching sequence, time and the developing process

should always be carefully designed. The best InAs channel recess etchant is acetic acid

solution; it has a high etching rate (2.5 nm/s) and selectivity (exceeding 1000) over AlSb.

2.2.2   HEMT processing

        HEMT fabrication processes typically include these steps: device mesa

isolation, source/drain contact formation, and Schottky gate deposition [23]. In GaAs-

based HEMT fabrication, the traditional way is to define the device mesa first, then

deposit and alloy the source/drain contact metal, and lastly deposit a Schottky gate. But this procedure for the InAs/AlSb HEMT suffers from the high reactivity of AlSb to oxygen and common alkaline-based solution developers. Dvorak [11] has reported a non-alloyed ohmic contact process for InAs/AlSb HEMTs based on selective wet etches. In his work, the ohmic contacts are deposited before the mesa isolation step. In this way the AlSb is exposed to developer only to define the gate. In an other approach, Boos *et al.* [6], postponed the mesa isolation to the last step, using air bridges and wet chemical etching; this process also eliminates the mesa-sidewall gate leakage current, which is explained later.

In our work, we have developed a single-metallization process in which source, drain, and gate metals are deposited simultaneously. In this process, we have encountered an apparent mesa-sidewall-related gate leakage current which is yet to be removed. Here we briefly list the sequence of the device formation:

(a) Define the source/drain contact by ultraviolet (UV) contact lithography using positive photoresist. Remove the top InAs and the $Al_{0.6}In_{0.4}As$ layer by a citric-acid-based etchant. Etch the AlSb top barrier layer to the underlying InAs channel layer. Because the etchants used are selective to AlSb, a shiny surface is apparent on completion.

(b) Define the mesa using positive photoresist. Etch to the $Al_{0.8}Ga_{0.2}Sb$ mesa floor.

(c) Define the metallization pattern for source, drain, and gate using negative photoresist. Evaporate Ti/Pt/Au and lift-off in acetone.

Over etching to the underlying AlSb buffer must be avoided. If the AlSb layer is exposed to the air, it oxidizes rapidly. The products of this oxidation are unstable, and tend to crack and flake off the substrate. This makes further processing

difficult if not impossible. etal deposited on oxidized AlSb also tends to peel off. This is shown in the optical micrograph of Figure 2.2. The photo was taken from a sample which was overetched by a highly-diluted hydrofluoric (1 HF: 500 H_2O) during the mesa isolation and further etched in AZ327 MIF developer during the lithography for gate metallization. The source and drain regions were etched to the InAs channel, then photoresist was placed on the central (white) rectangle shown in Figure 2.2. In etching to the mesa floor, the source-drain metal regions etched beyond the AlGaSb layer into the underlying AlSb where it oxidized. This photo was taken 25 minutes after the etching, illustrating the rapidity of AlSb degradation due to oxidation.
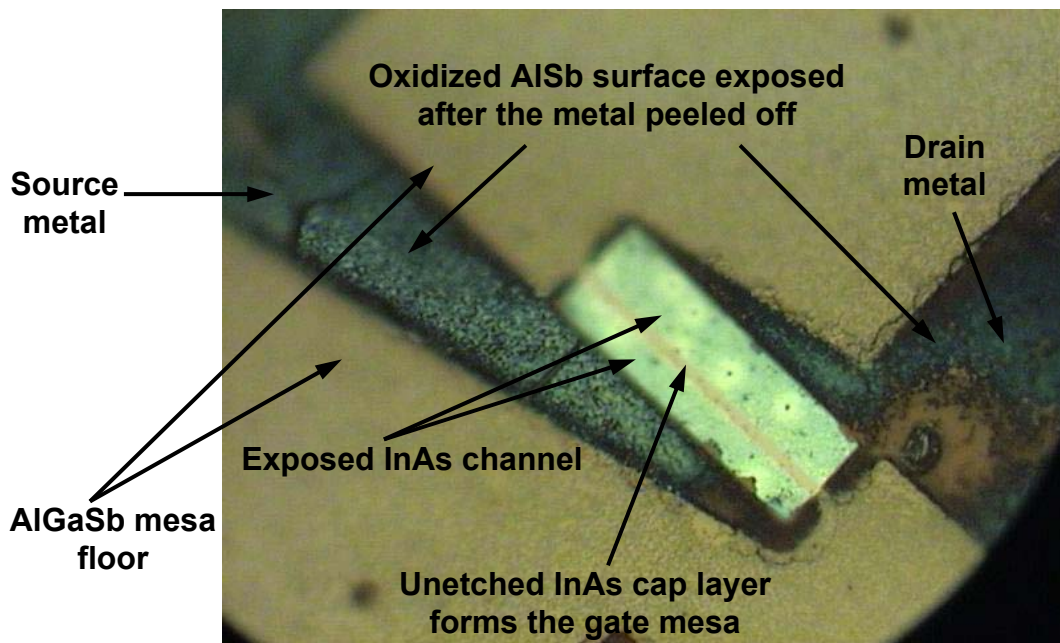
Figure 2.2 The effect of exposing AlSb buffer.

The following figures, Figures 2.3.1 and 2.3.2, illustrate the single-metallization process flow.
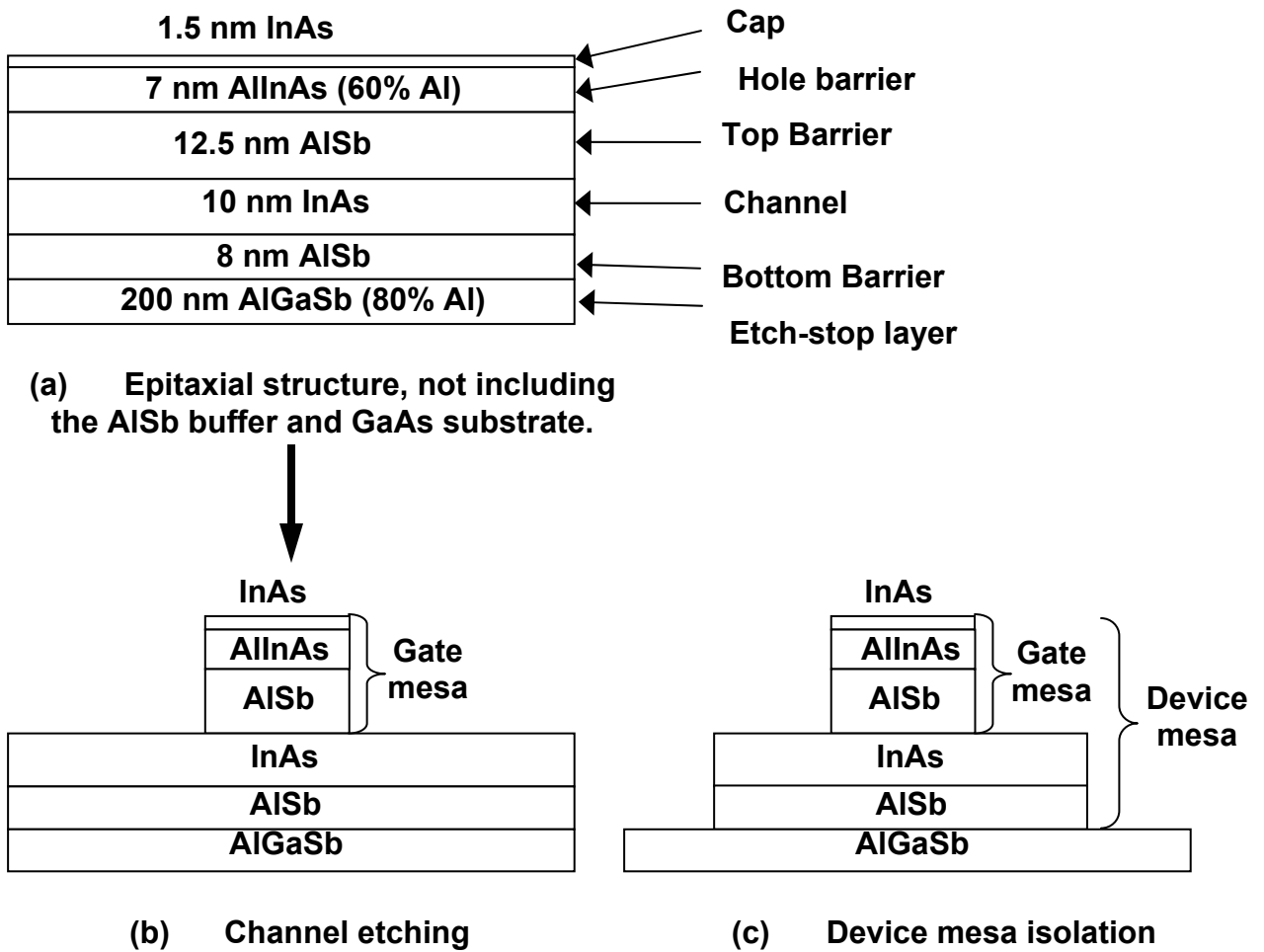
Figure 2.3.1 HEMT mesa formation. The active device layers are drawn to scale, no scale is intended in the horizontal direction.

**(d)   Source, drain and
gate metal deposition**
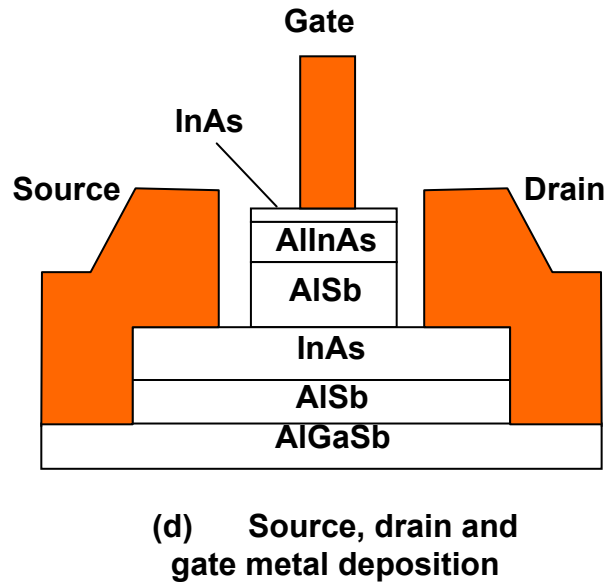
Figure 2.3.2 HEMT one-step metallization.Active device layers are drawn to scale, no
scale is intended in the horizontal direction or for the metal.

Figure 2.4(a) is a typical unit device layout designed using Mentor
Graphics IC Station. The contact pad geometry is designed for microwave-frequency
testing using 100 μm-pitch coplanar waveguide probes and has a characteristic
impedance of 50 μm for the GaAs substrate. The center-tapped gate feed is designed to
reduce the gate resistance and provide a symmetric input geometry. Figure 2.4(b) shows
an enlargement of the central device mesa.

Source pad

Gate pad

Source pad

200 µm

60 µm

40 µm

Drain pad

(a) Device with microwave testing pads.

Source

Gate feed

Source

Gate Length 1 µm

Mesa edge

Drain

Drain

Channel etch	**Metal contacts**

(b) Device mesa details.
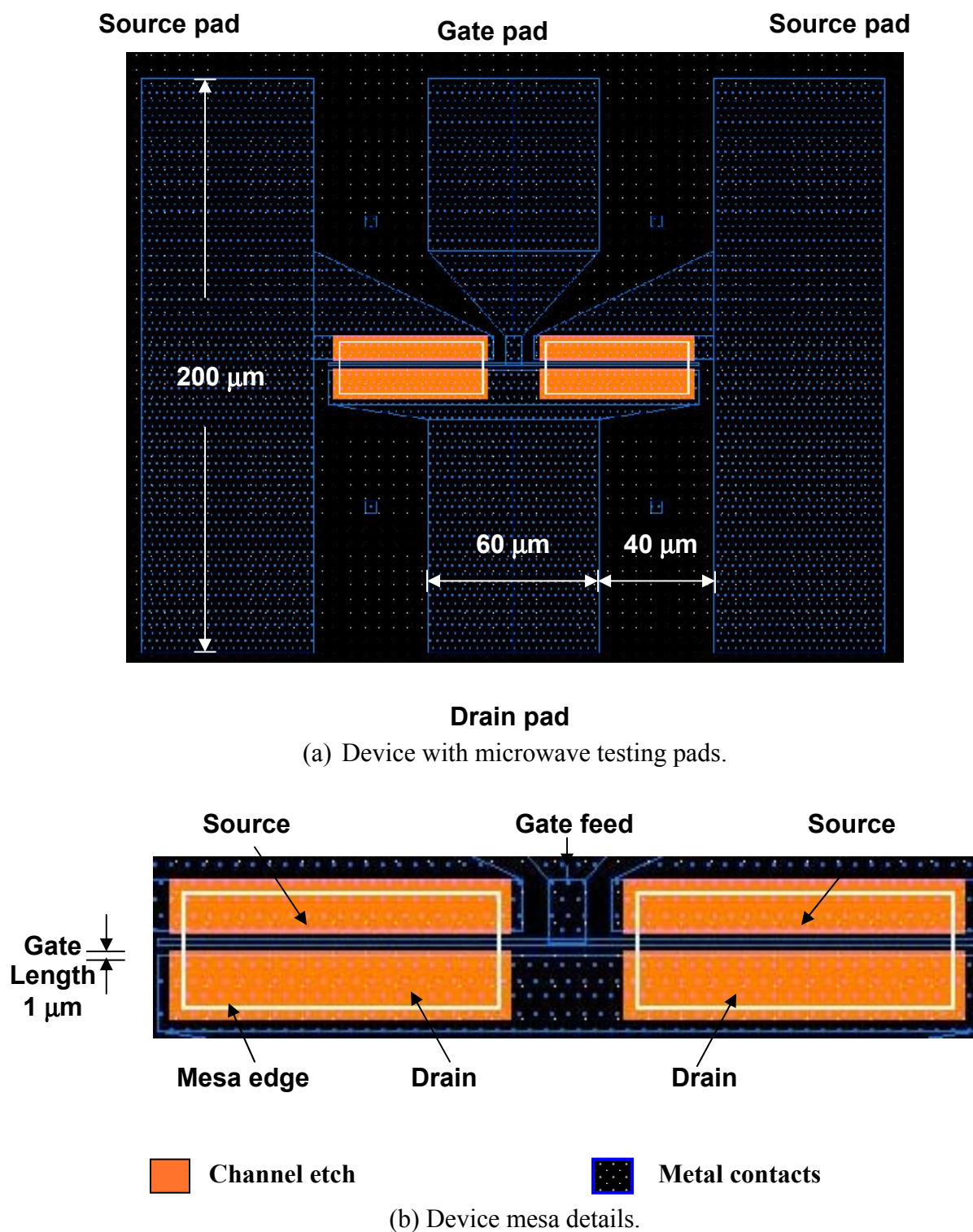
Figure 2.4 Layout of InAs/AlSb HEMT designed for microwave measurement: (a) metal pads and (b) mesa details for a pair of 50 µm wide devices.

The mask includes devices with gate widths of 10, 20, 40, and 50 μm, each of which has four different source-to-drain spacings: 4, 5, 6, and 7 μm. This mask set also provides test structures, including transmission line method (TLM) structures for contact resistance measurements, two 4 x 50 μm^2 fat FETs, and the metal pads for short and open microwave measurement calibration.

2.3   Gate metal deposition

Gate formation is a critical part of HEMT fabrication. One micron long Ti/Pt/Au gates are deposited in this work by electron beam evaporation. Figure 2.5 shows the steps of our lift-off process, outlined as follows: open a window in the photoresist where the metal is going to be deposited, evaporate the metal, dissolve the photoresist in acetone and lift-off the metal deposited on the photoresist. Successful lift-off is achieved by optimizing the image reverse technique to form an overhanging photoresist profile and define narrow openings (~1 μm in this work) in the photoresist. The detailed recipe applied to the image reversal process is included in Appendix B. Figure 2.6 shows a scanning electron microscope (SEM) image of a completed device with a 1 μm gate.

UV light source

Chromium mask

AZ5214-E photoresist

Substrate

(a) Primary exposure

Hot plate

(b) Reverse Bake

(c) Flood exposure

**Overhanging
photoresist profile**

(d) Develop

(d1) Metal evaporation

(d2) Metal evaporation

(e) Lift-off in acetone
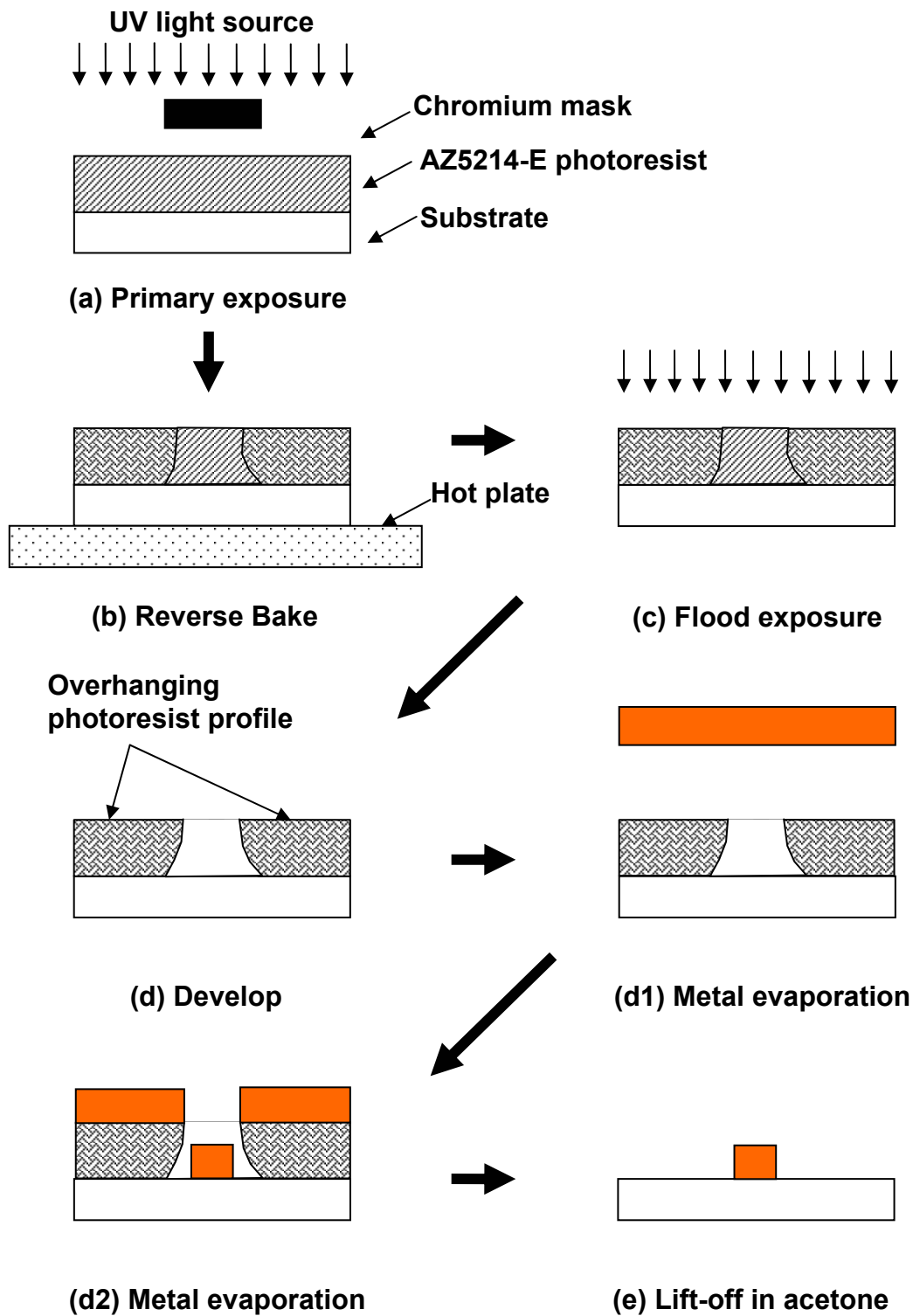
Figure 2.5 Lift-off process.

(a)

(b)
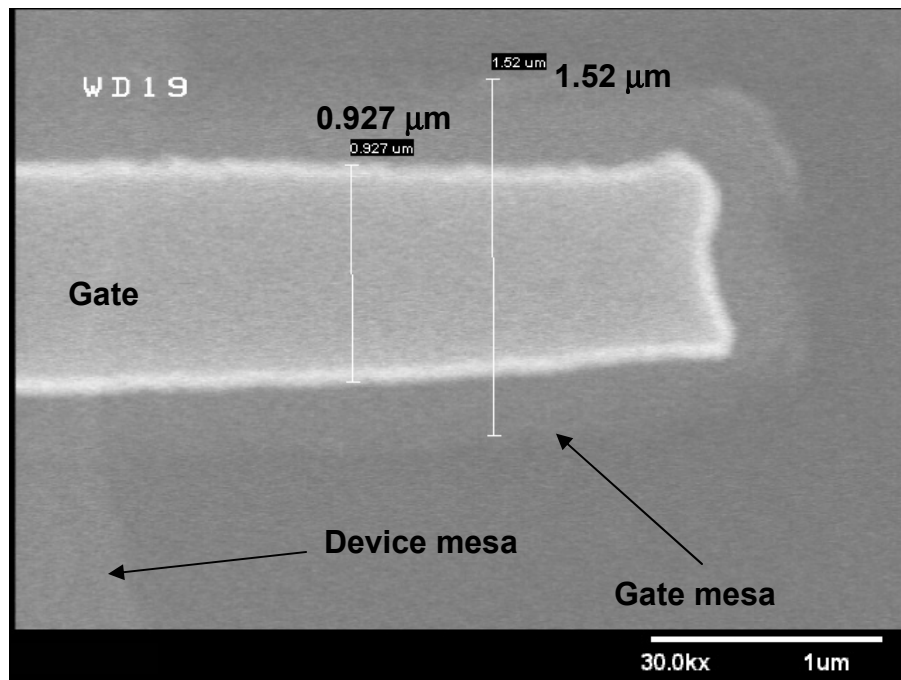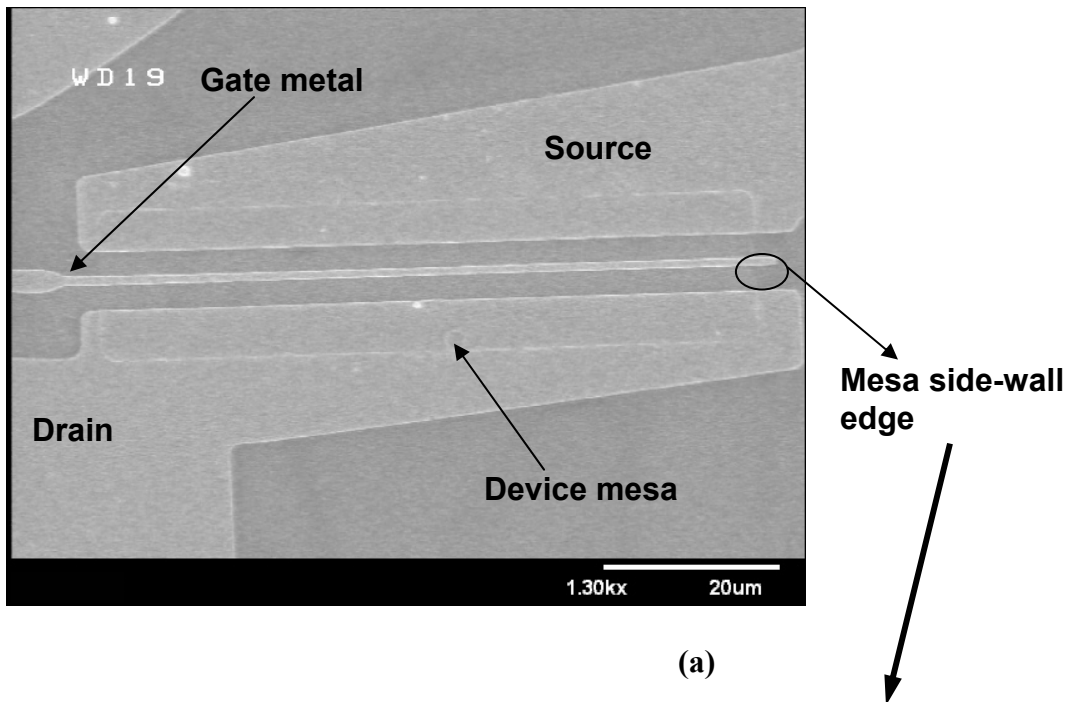
Figure 2.6 Scanning electron microscope images of an AlSb/InAs/AlSb HEMT formed by a one-step metallization: 50 µm HEMT and (b) magnification of the gate area at the mesa side-wall.

2.4   Device performance and data analysis

In this section, we provide electrical measurements of the fabricated InAs/AlSb HEMTs and analyze the findings. Measurements were made in the dark at room temperature using an Agilent 4155 semiconductor parameter analyzer on a Cascade Microtech 11861 probe station.

2.4.1   Common-source transistor characteristics

Figures 2.7 to 2.10 show common source transistor characteristics of four different width HEMTs from the same wafer. Clear gate control of the drain current is achieved, however the drain current cannot be pinched off.
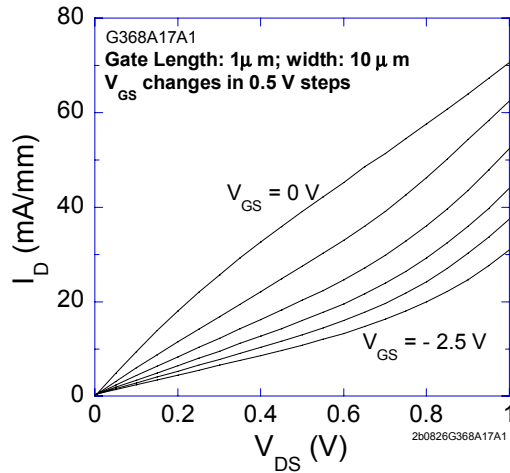
Figure 2.7 Common source transistor characteristics for a 10 μm wide InAs/AlSb HEMT.
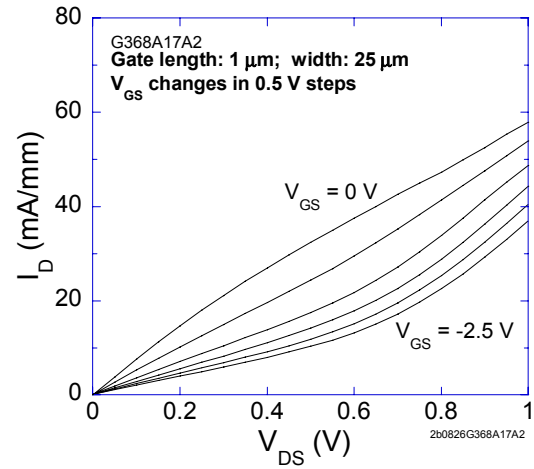
Figure 2.8 Common source transistor characteristics for a 25 μm wide InAs/AlSb HEMT.
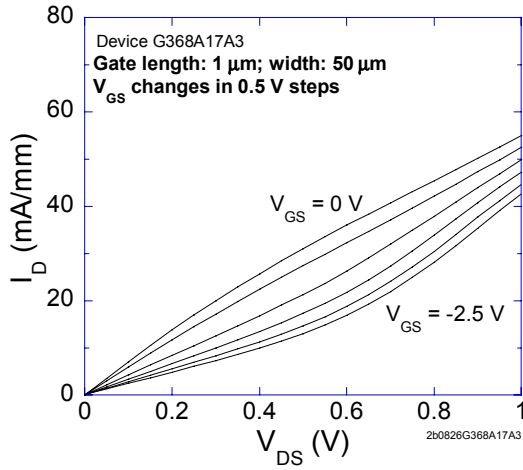
Figure 2.9 Common source transistor characteristics for a 50 μm wide InAs/AlSb HEMT.
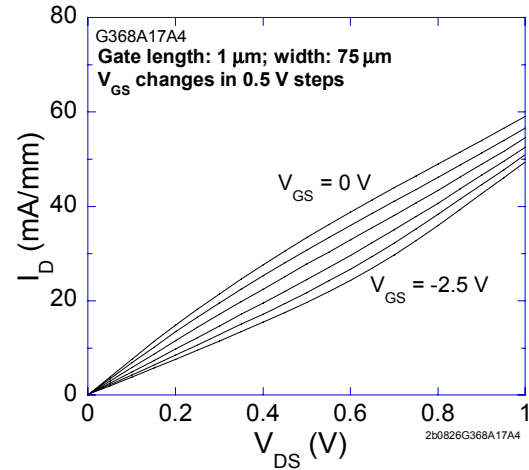
Figure 2.10 Common source transistor characteristics for a 75 μm wide InAs/AlSb HEMT.

The absence of pinch-off could result from the lateral etching of the AlSb barrier layer over the InAs channel as illustrated in Figure 2.11. During the mesa isolation process, the last etch is to selectively etch away the AlSb bottom barrier layer. At the same time the top AlSb layer is etched laterally. In the metallization lithography, AlSb etches in alkaline-based photoresist developer, AZ327 MIF, which is expected to cause further etching in the lateral direction. If the top AlSb layer etches significantly in the lateral direction, the InAs channel upper surface at the mesa side-wall maybe exposed. After metal evaporation, the gate would then contact part of the exposed channel at the mesa side-wall.

M.S. Thesis, April, 2003
Sb-Based High Electron Mobility Transistors: Wu Bin
 Processing and Device Characterization   University of Notre Dame
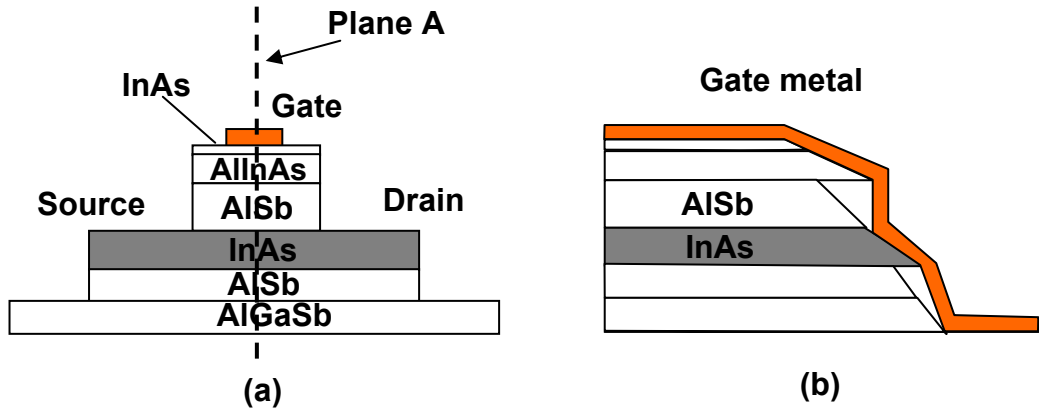
Figure 2.11 Side-wall cross-sectional views of the HEMT:
(a) device mesa and (b) cross-section parallel to the direction of the gate showing the
expected profile of the mesa edge.

      Metal-InAs contacts are typically ohmic. When source, drain, and gate
contacts are all touching the InAs channel, a gate metal to channel leakage path is created.
When there is a potential difference between the gate and the drain or source, there will
be leakage current along this parasitic path from the drain to the gate, I_{DG}, and source to
the gate, I_{SG}. In addition, because of the gate metal touching the InAs channel at the mesa
side-wall, the channel will never be fully depleted at the mesa edge. Consequently, a
there is always a drain current, I_{DE}, as shown in Figure 2.12.
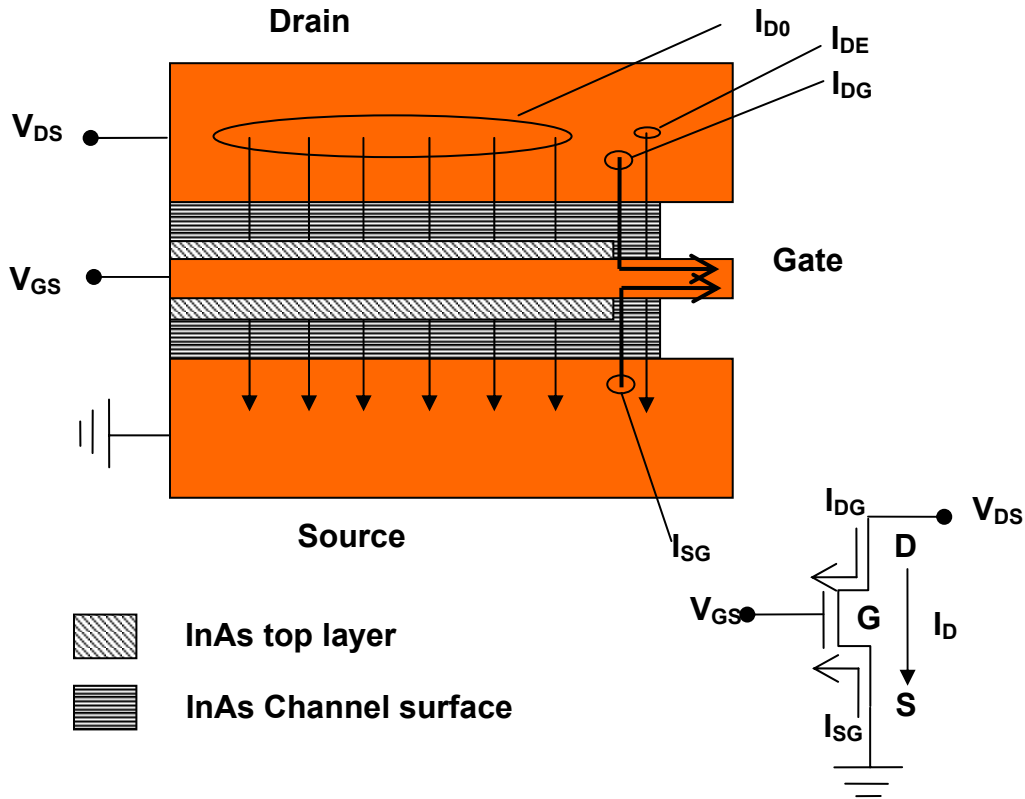
Figure 2.12 Gate metal to InAs channel short-circuiting effect.
(Source is grounded, $V_{GS} < 0$ and $V_{DS} > 0$)

According to Figure 2.12, the measured drain current, I_D, is the sum of I_{D0} and I_{DG} and. When gate bias is negative to deplete the channel, I_{D0} is turned off. But the other components, I_{DG}, IS_G and I_{DE} can still remain.

Identical transistors on the same wafer show different leakage characteristics, as shown in Figure 2.13. The gate current is less than 0.5 mA/mm in the transistor of Figure 2.13(a) and the drain current is turned off at the -1.25 V gate bias, while in (b) the gate current exceeds 6 mA/mm and the drain current can not be turned off.
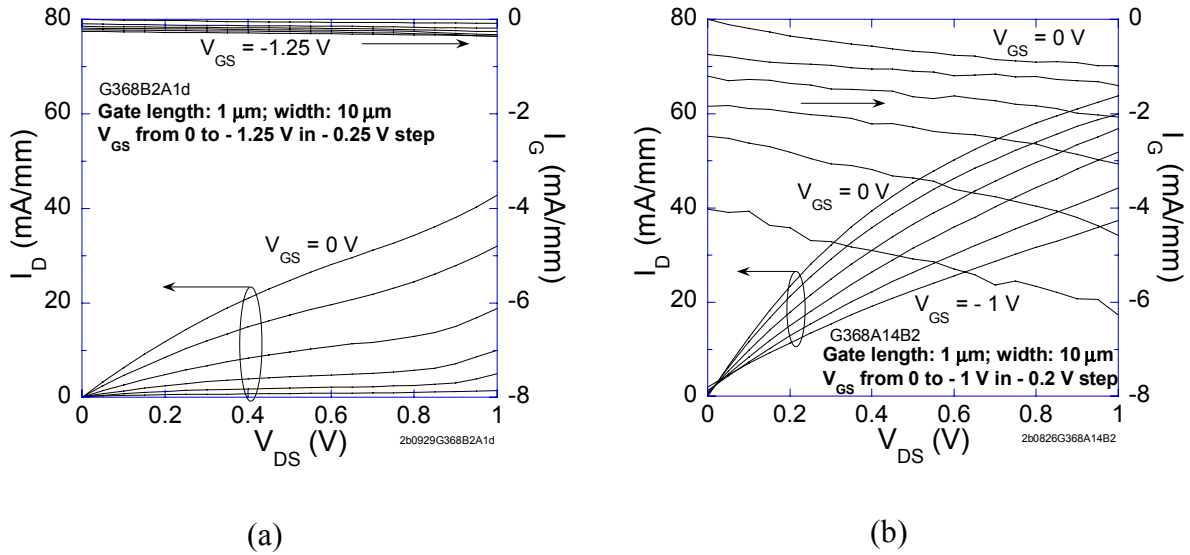
Figure 2.13 Common-source transistor characteristic of two identical 10 µm HEMTs.

In order to achieve the pinch-off of the drain current, a citric-acid-based etching was performed on the device shown in Figure 2.13(a) as the last etching step during the mesa isolation to significantly undercut the InAs channel under the AlSb top barrier layer. The deep lateral recess etching of the InAs channel is intended to guarantee that the upper surface of the channel is not be exposed at the mesa edge after the following photolithography developing process (which was done in the AZ327 MIF). If the process successful, the gate metal at the mesa side-wall will not contact the channel after the metal deposition, see Figure 2.14.
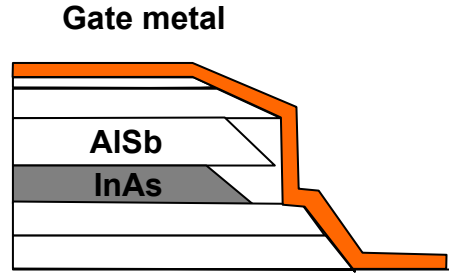
Gate metal

Figure 2.14 Gate metal profiles at the mesa side-wall with a significant undercut of the InAs channel.

2.4.2   Special process to avoid gate metal contact with the InAs channel

Different methods have been tried to avoid the gate metal contacting the InAs channel during the processing of InAs/AlSb HEMTs [11], [7], [14]. In our work, we have demonstrated improvements in the gate leakage current reduction and drain current control by significantly undercutting the InAs channel beneath the AlSb top barrier layer. However, this lateral etching is hard to control when the AZ327 MIF developer is used due to its high etch rate for AlSb. The following process flow was modified from [14] and is outlined as follows: etch down to the InAs channel, put on the source, drain and gate metal contacts, define and etch the mesa. In this case, all the metal contacts are placed on the cap layer. The gate metal does not contact the mesa side-wall.

This new process has been demonstrated on the heterostructure illustrated in Figure 2.15(a). Figure 2.15(b) shows the device geometry.

InAs 6 nm
15 nm $Al_xGa_{1-x}As_ySb_{1-y}$
10 nm InAs
1 μm $Al_xGa_{1-x}As_ySb_{1-y}$
200 nm AlSb
200 nm GaAs
200 nm GaAs

(a)

(b)
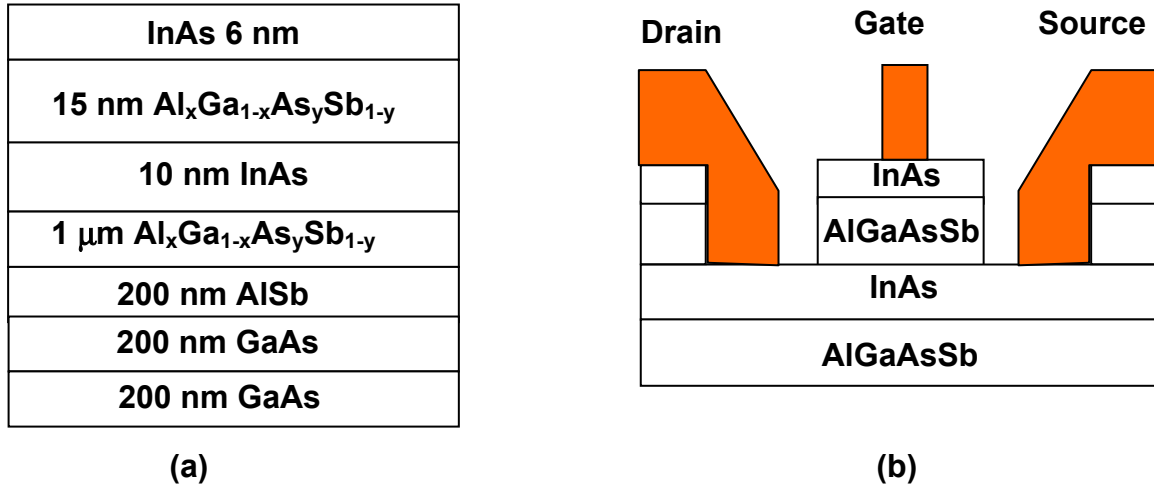
Figure 2.15 High electron mobility HEMTs fabricated with the mesa isolation performed as the last step: (a) epitaxial structure and (b) device geometry.

The wafer was grown by MBE system by Dr. Greg Triplett of Georgia Tech.. The mole fraction of Al is 0.8 which is chosen to achieve a type I straddling heterojunctions between the quaternary materials and InAs, and hence get more better holes blocking in the valence band [24]. The mole fraction of Sb is about 0.08 to 0.16, which is designed to provide a 6.1 Å lattice constant to match that of InAs [24]. As shown in Figure 2.14(b), all three metal contacts (source, drain and gate) of the device are located on the top InAs layer. The contacts are isolated from each other during the mesa isolation step. By this method, we achieved better control of the channel current, Figure 2.16, and an improved transconductance, g_m, of ~120 mS/mm compared to the other fabrication processed evaluated, Figure 2.17.
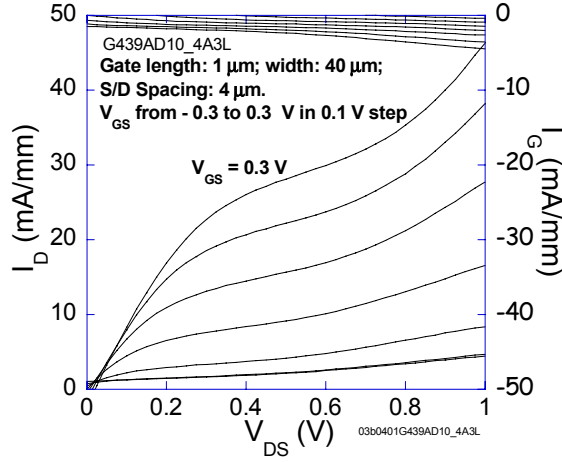
Figure 2.16 Common-source
characteristic of AlGaAsSb HEMT.
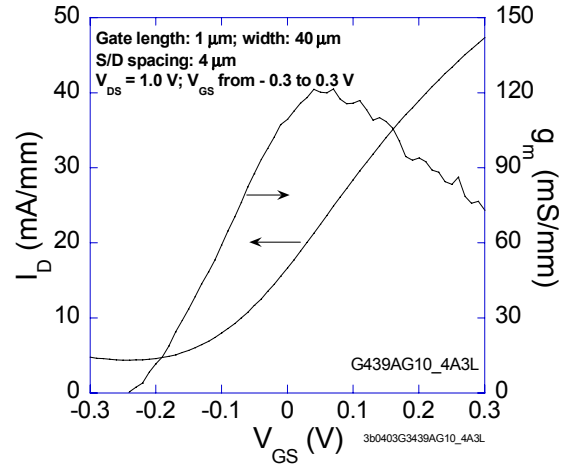
Figure 2.17 Transconductance and drain
current versus gate to source voltage.

2.4.3   Effect of source and drain resistance on output transconductance

Figure 2.18 is an equivalent circuit model for a HEMT where R_S is the resistance between the source contact and the channel region immediately under the gate.
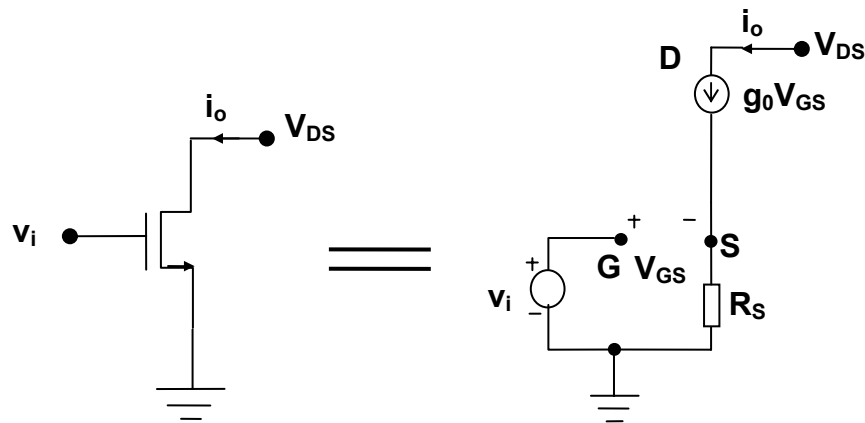
Figure 2.18 HEMT equivalent circuit.

Because R_S is not zero, the external transconductance, g_m, is reduced from the intrinsic transconductance g_0 to:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{i_0}{v_i} = \frac{g_0 V_{GS}}{V_{GS} + g_0 R_S V_{GS}} = \frac{g_0}{1 + g_0 R_S} \qquad (2\text{-}1)$$

Here, i_0 is the output current, and v_i is the input voltage applied between the gate and source of the HEMT. Figure 2.19 is a plot of Eq. (2-1), showing the dependence of the extrinsic transconductance on the source resistance where all values are normalized to the mesa width.
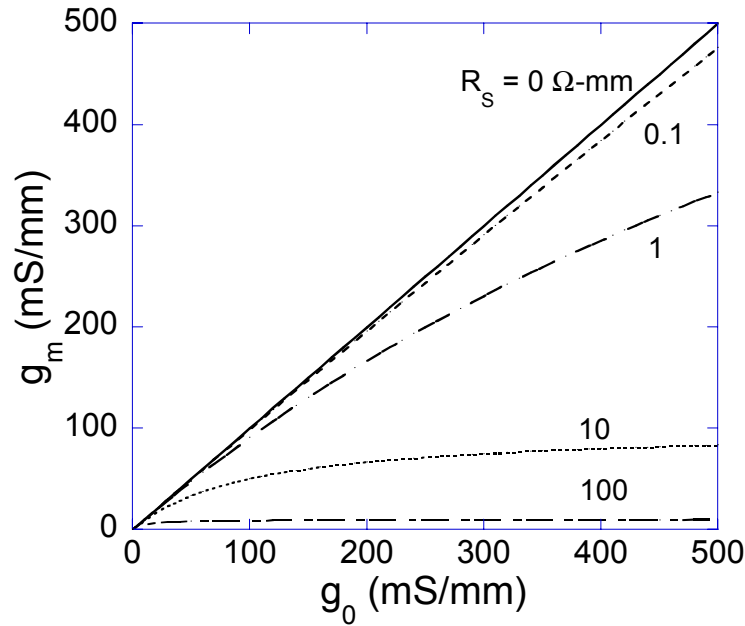
Figure 2.19 Plot of Eq. (2-1) to illustrate how extrinsic transconductance, g_m, changes as a function of source resistance R_S and intrinsic transconductance, g_0.

From Eq. (2-1), we can calculate the intrinsic transconductance of the devices by the following equation:

$$g_0 = \frac{g_m}{1 - g_m R_S} \qquad (2\text{-}2)$$

Figure 2.20 shows the external transconductance g_m and calculated intrinsic transconductance g_0, using Eq. (2-2), as a function of gate bias (from -1.5 to 0.5 V) when the source and drain voltage is 0.4 V for the transistor of Figure 2.13 (a).
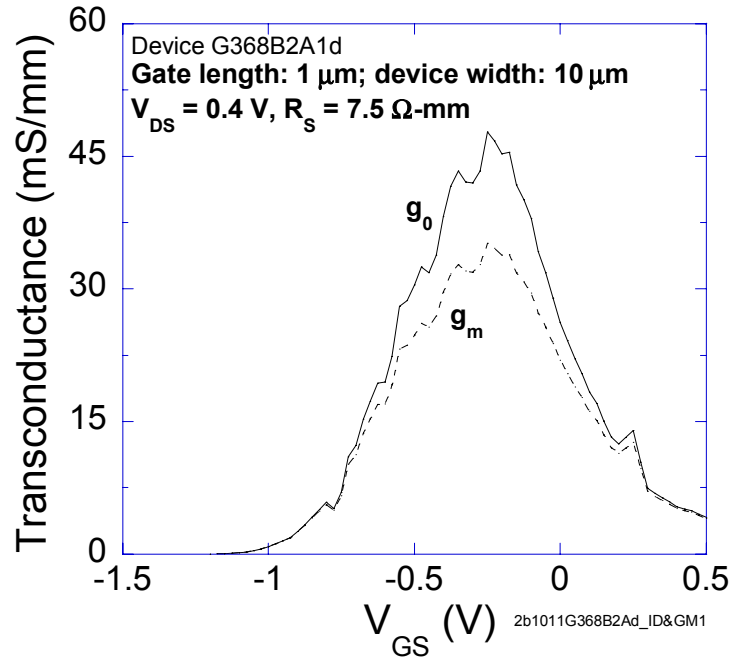
Figure 2.20 External transconductance, g_m, and intrinsic transconductance, g_0, vs. gate-source voltage.

Source resistance, R_S, is calculated according to Khan *et al.* [25]. From the steepest slope of the I_D-V_{DS} characteristics at the highest positive gate bias, we estimated $(R_S + R_{CH} + R_D)$ to be about 1530 Ω. The channel resistance $R_{CH} \approx L/(q\mu n_s W)$ where L is the gate length, q is the electronic charge, μ is the low field mobility, n_s is the maximum sheet carrier density in the channel, and W is the device width. From Hall-effect measurement results supplied by April Brown, we estimate get R_{CH} to be 30 Ω. Due to the symmetry of the designed device structure, $R_S \approx R_D$, giving R_S to be about 749 Ω. Normalized with the device width, R_S becomes 7.5 Ω-mm. In Figure 2.20, we estimate the peak intrinsic transconductance to be 52 mS/mm.

CHAPTER 3

WET OXIDATION FOR DEVICE ISOLATION

Overview

Wet oxidation of AlAs is used in the fabrication of surface emitting laser

to provide a high resistance current confining path [26]. If an insulating oxide of AlGaSb

could be formed, similar benefits could be achieved for AlSb/InAs HEMTs. We have

explored the wet oxidation of AlGaSb and show a single experimental result which

suggests that oxidized AlGaSb is conductive and not suitable for providing electrical

isolation.

3.1   Motivation for wet oxidation of $Al_{0.8}Ga_{0.2}Sb$

We have already shown in Figure 2.2 that metal does not adhere well to

the exposed AlSb surface and that photoresist developer attacks AlSb and $Al_{0.8}Ga_{0.2}Sb$.

Figure 3.1 shows an example of a wafer in which a poor metal adhesion on $Al_{0.8}Ga_{0.2}Sb$

exposed to AZ327 MIF developer was observed. Since a well-characterized wet

oxidation process has been developed at Notre Dame [27], we have oxidized

Al0.8Ga0.2Sb with the aim to create a stable, developer-resistant mesa floor. We

expected to obtain a stable oxide layer mainly consisting of Al_xO_y.

**Oxidized
AlSb**

**Metal peels off, exposing the underling
Al$_{0.8}$Ga$_{0.2}$Sb device mesa floor**
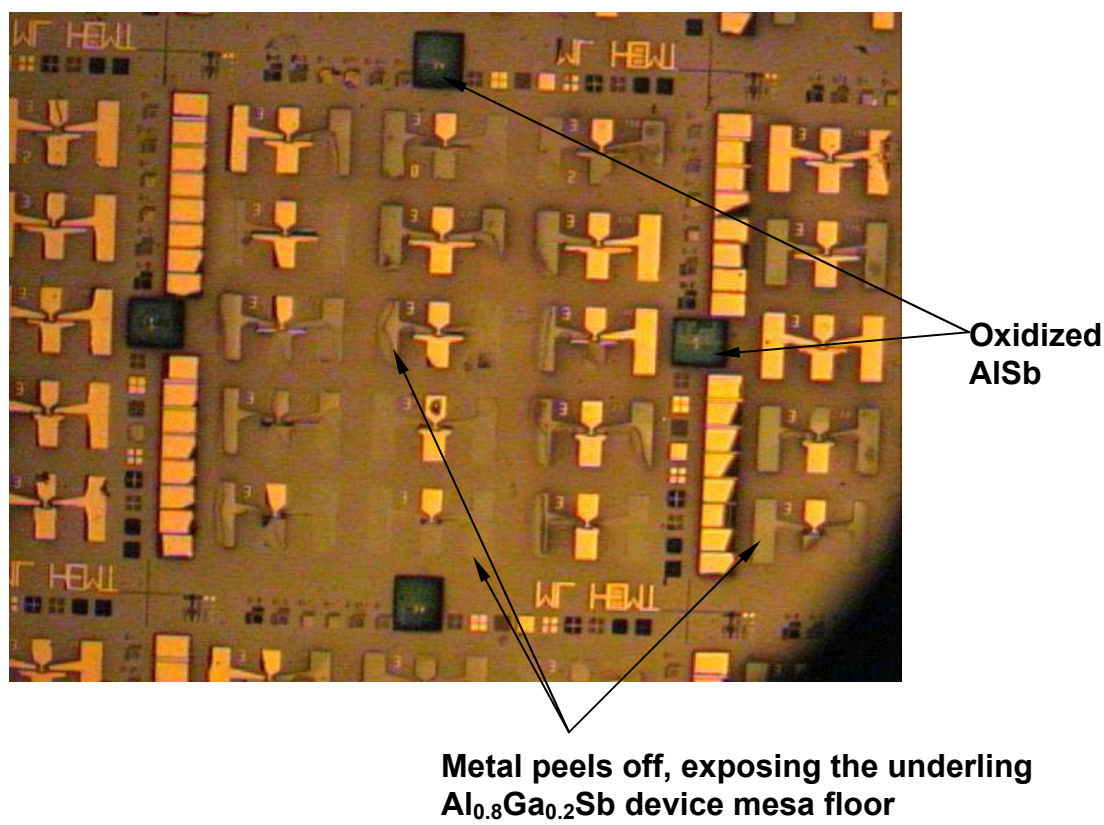
Figure 3.1 The developer AZ327 MIF attacks Al$_{0.8}$Ga$_{0.2}$Sb.

3.2   Wet oxidation of $Al_{0.8}Ga_{0.2}Sb$

The epitaxial structure of the sample Sb3157 studied is shown in Figure

3.2.

0.77 nm InAs

7 nm AlInAs (50% Al)
12.5 nm AlSb
10 nm
8 nm AlSb
200 nm $Al_{0.8}Ga_{0.2}Sb$
1.5 μm AlSb
200 nm GaAs
SI GaAs Substrate
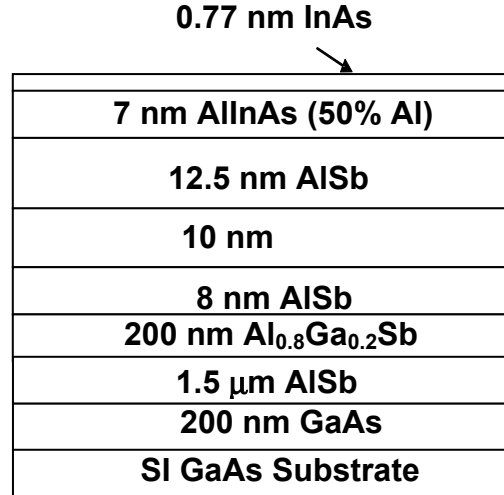
Figure 3.2 Epitaxial structure of Sb3157 with active layer drawn with scale.

The wet oxidation process and the experiment for testing the influence of

the AZ327 MIF developer on oxidized and unoxidized material is as follows: solvent

clean the sample; etch Sb3157 down to the $Al_{0.8}Ga_{0.2}Sb$ layer. (Citric acid solution for 40

s, HF 3 s, Citric acid solution 40 s, and HF 2 s); cleave the sample to 4 pieces, labeled

with control, B1, B2, and B3; wet oxidize B1, B2 and B3 at 350 ˚C, 400 ˚C, 450 ˚C for 2

minutes each, respectively; deposit Ti/Pt/Au (200 Å/200 Å/2000 Å) metal dots, 500 μm

in diameter and separated by 250 μm, on all the four samples with a shadow mask, which

was used to avoid exposure to developer; measure the electronic characteristic of all the

samples; put sample B2 into AZ327 MIF for 40 min; measure the electronic

characteristic of B2 again; use X-ray Photoelectron Spectroscopy (XPS) to analyze the

surface element composition of the four samples to confirm the etches did stop in

$Al_{0.8}Ga_{0.2}Sb$ layer.

Figure 3.3 compares the surfaces of control, B1, B2, and B3 samples. The

surface morphology changed as a result of the oxidation, as the oxidized surfaces became

shinier, but among the wet oxidized pieces no differences were apparent by optical

microscopy.
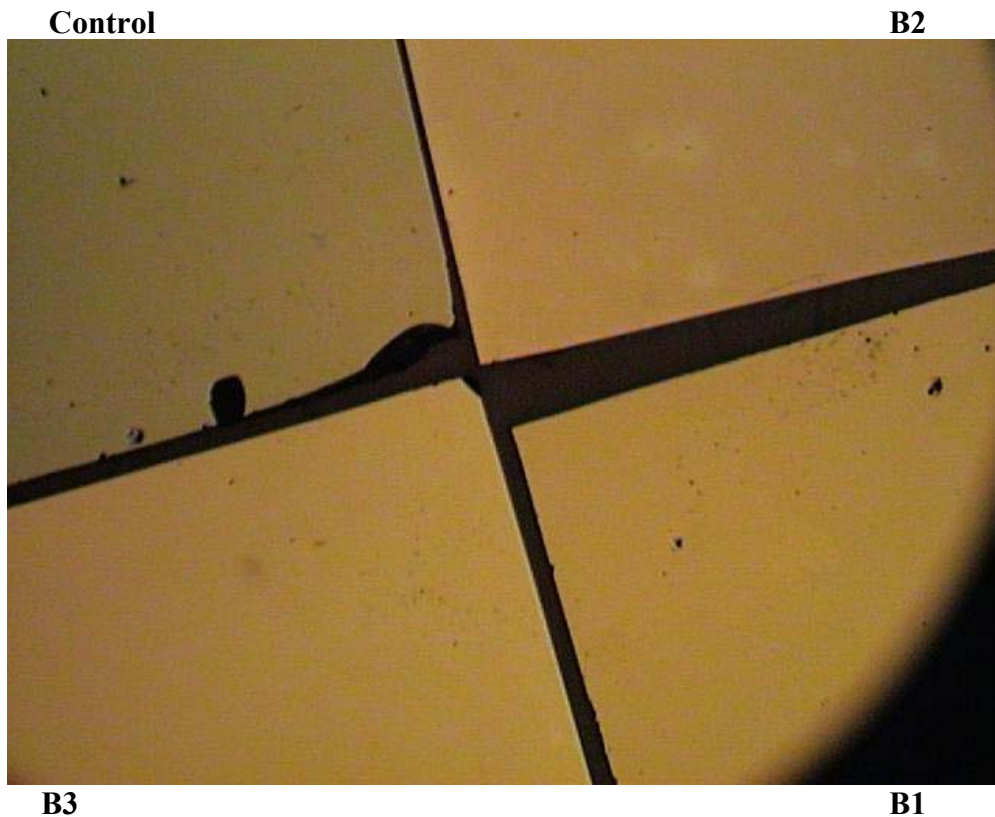
Figure 3.3 Optical micrograph comparing the surfaces of $Al_{0.8}Ga_{0.2}Sb$ samples: oxidized in the air (control) and wet oxidized at 350 ˚C (B1), 400 ˚C (B2), and 450 ˚C (B3) for 2 minutes.

Current-voltage measurements were taken between adjacent metal

contacts, 500 μm in diameter and, spaced 250 μm apart. We increased the current from 0

to 40 mA and measured the voltage difference. By controlling the current, the

characteristics were taken without destructive break down. The results obtained are

shown in Figure 3.4.
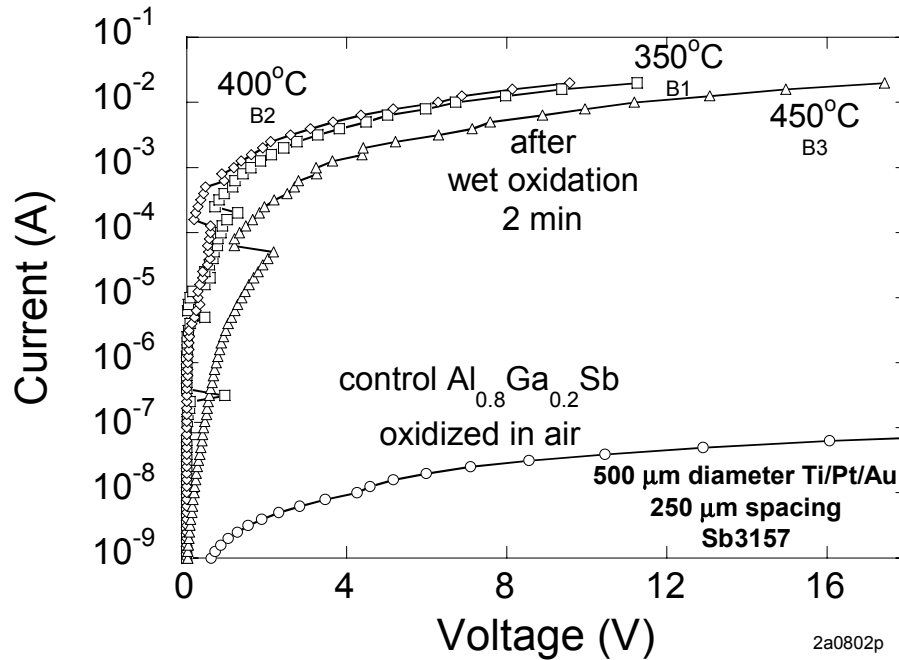
Figure 3.4 Current-voltage characteristic of air oxidized control sample and wet oxidized
samples.

We observed that the surface becomes more conductive after the wet

oxidation. The change in current for the same voltage point exceeds four to five orders of

magnitude for the 350 ˚C and 400 ˚C samples. The 450 ˚C wafer is less conductive than

the other oxidized samples in the low bias range, but consistent with the other wet

oxidized results at biases exceeding 3 V. The wet oxidation surfaces are electrically less

stable than the control. The S-shaped kinks along the curves could result from the

breakdowns of higher resistive paths between the two metal dots where breakdown

results in lowered resistance along the path. Another possible mechanism for the

breakdowns is local heating: the current crowds at a locally conductive non-uniformity

and heats it to cause a change towards more conductive state along the path.

In order to find out if the sample is resistive to AZ327 MIF developer after

wet oxidation, we put the 400 ˚C sample, B2, into AZ327 MIF developer for 40 minutes

and measured the I-V, Figure 3.5.
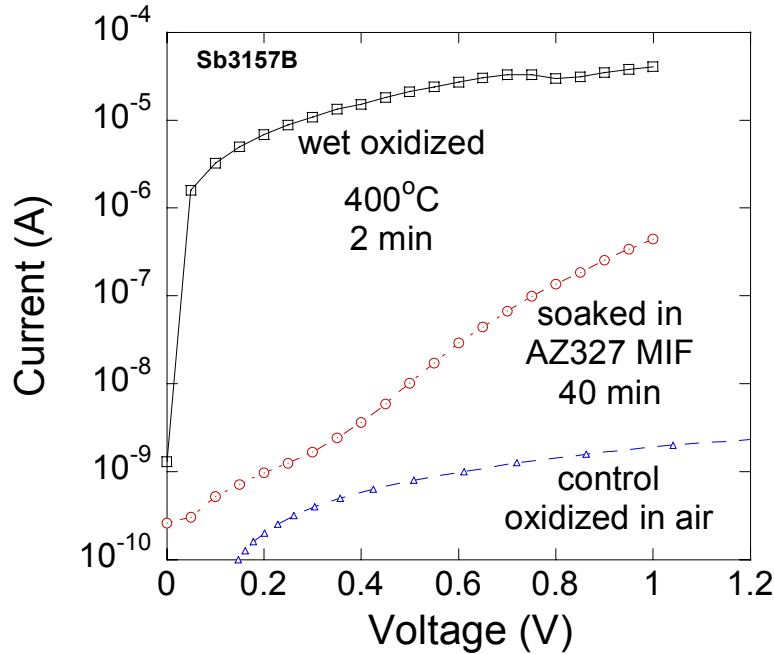
Figure 3.5 Current-voltage measurements of wet oxidized $Al_{0.8}Ga_{0.2}Sb$ and the changes
caused by soaking in AZ327 MIF developer.

The surface after developer treatment became more resistive. It may be because that the developer which removes the surface layer and exposes the resistive AlSb buffer underneath. The conclusion is supported by the observation that the surface of the B2 turned black and cracked in a few days after the developer treatment, consistent with exposed AlSb.

3.3   X-ray photoelectron spectroscopy analysis of wet oxidized $Al_{0.8}Ga_{0.2}Sb$

Surface analysis by X-ray photoelectron spectroscopy (XPS) was performed with a Kratos XSAM 800, using a 12 KV/12mA Mg Ka x-ray source is excited exciting electrons from core and valence levels of the constituent atoms near the surface of the sample, and photoelectrons are passed through an energy analyzer and directed to an electron multiplier and detector. Sweeping the input energy of the analyzer produces a spectrum of the number of ejected photoelectrons as a function of kinetic energy (KE). The KE of the electron is related to its binding energy (BE), $KE = h\nu - BE - WF$ where $h\nu$ is the known energy of the incident x-ray radiation and WF, is work function of the material. This technique can be used to characterize a wide variety of inorganic and organic materials. In our case, we want to know the chemical composition of the $Al_{0.8}Ga_{0.2}Sb$ surfaces before and after wet oxidation. The data was taken by Dr. Jianli He. Survey spectra, from 0 to 1200 eV BE, were collected with a resolution of 1 eV.

Figure 3.6 is the comparison of the overall spectrum of the four samples: control, B1, B2 and B3. The four sets of data were offset vertically for the convenience of the comparison.
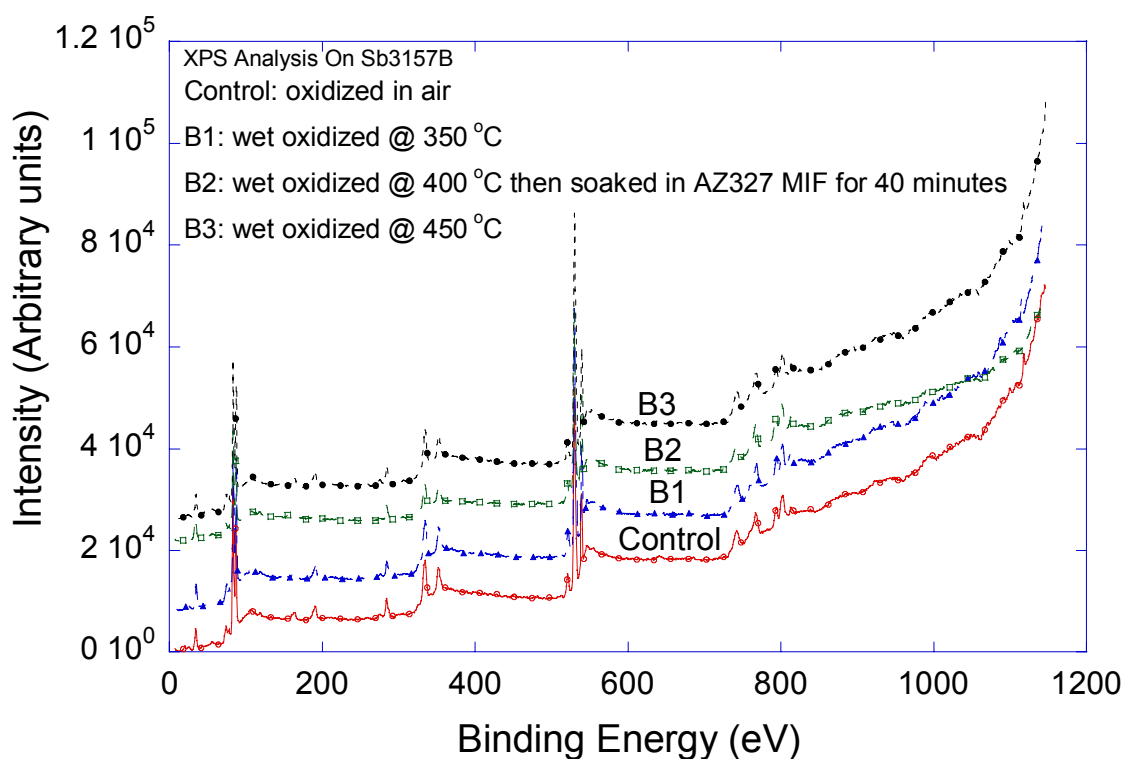
Figure 3.6 XPS survey spectrum of core-level photoelectron emission from the wet oxidized $Al_{0.8}Ga_{0.2}Sb$ surface.

The follow figures, Figures 3.7 and 3.8, are the enlarged spectra from 0 eV to 210 eV BE and from 1060 to 1140 BE, respectively.
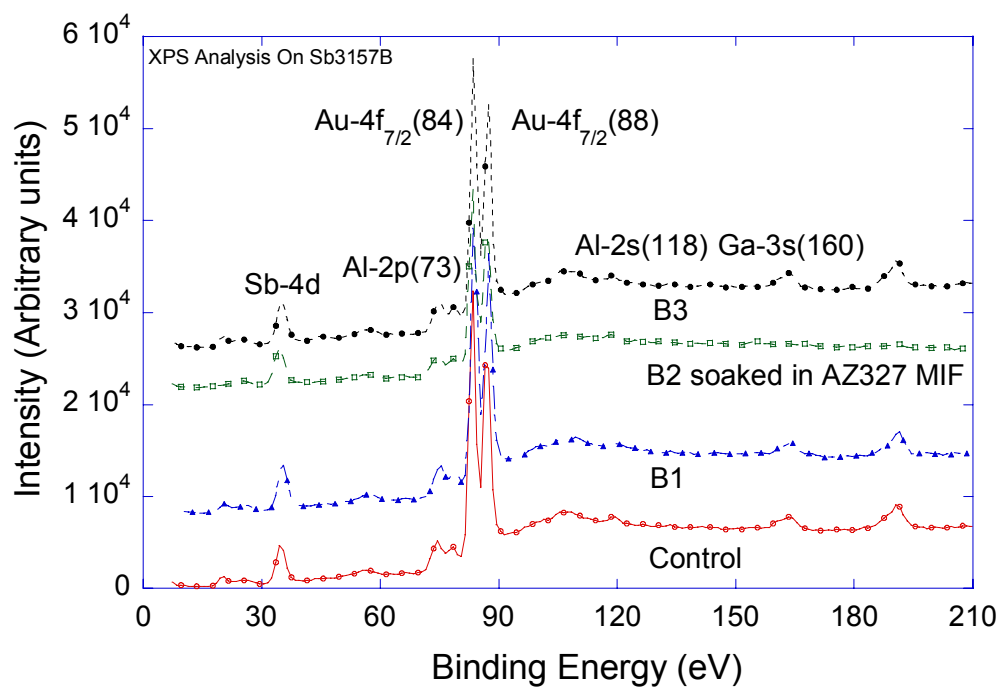
Figure 3.7 XPS core-level photoelectron spectra of Sb-4d, Al-2p (73), Al-2s (118), and Ga-3s (160).

In Figure 3.7, the Sb-4d, Al-2p, and Al-2s peaks were observed from all the four samples, while Ga-3s peaks were evident only from control, B1, and B3.
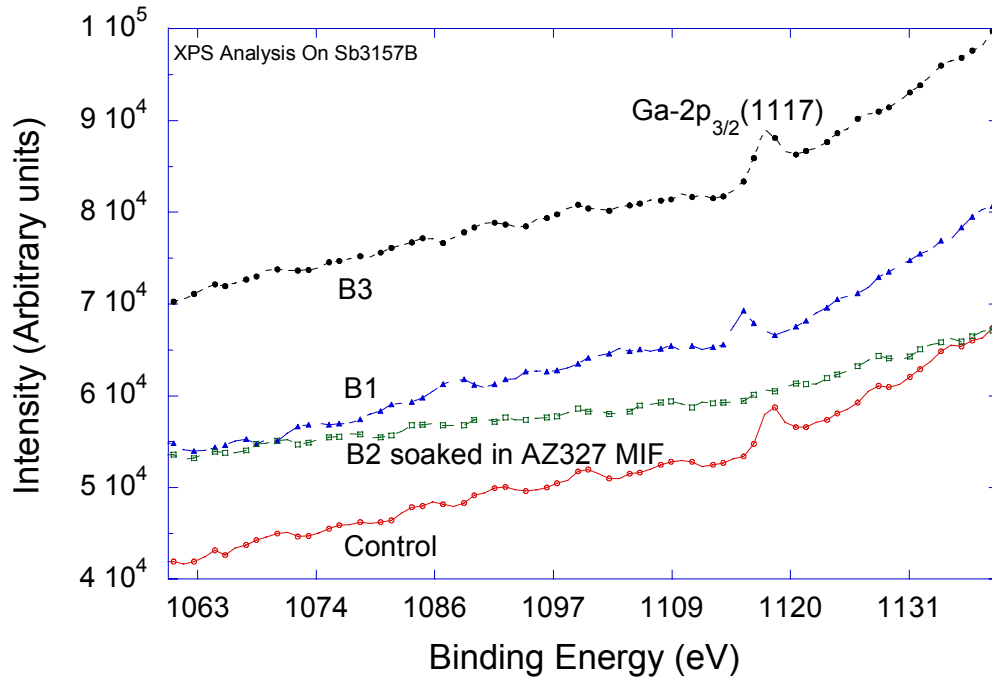
Figure 3.8 XPS core-level photoelectron spectra of Ga-2p$_{3/2}$ (1117).

In Figure 3.8, the Ga-2p$_{3/2}$ peaks were observed only from control, B1,

and B3.

XPS results of all four samples show signals from Al and Sb. We are sure

that the initial etches done to reveal the Al$_{0.8}$Ga$_{0.2}$Sb were completed correctly, because

we etched the whole wafer before cleaving it into pieces for the oxidations. We can also

be sure that all oxidations were made on Al$_{0.8}$Ga$_{0.2}$Sb. Figure 3.7 and 3.8 indicate that

there is no Ga near the surface of sample B2, which has been soaked in the AZ327 MIF

photoresist developer for 40 minutes and etched away more than 1200 Å. We can

conclude that the AZ327 MIF has removed the oxidized Al$_{0.8}$Ga$_{0.2}$Sb layer and exposed

the underlying AlSb buffer layer. This can also explain the change of the conductivity in

Figure 3.5, it is because of the change of the surface layer.

We think that the increase of the conductivity after wet oxidation is due to

the mechanisms of wet oxidation of $Al_{0.8}Ga_{0.2}Sb$. We suspect that pure Sb is one of the

products of the wet oxidation. The mechanism may be analogous to that which occurs

during thermal annealing of the oxide of GaSb [28]. In our case, near the $Al_{0.8}Ga_{0.2}Sb$

surface Sb_2O_3 may be formed, which subsequently reacts with GaSb via the reaction

$Sb_2O_3 + 2GaSb \rightarrow Ga_2O_3 + 4Sb$. Then the pure Sb may outdiffuse to the surface, causing

the significant conductivity increase.

CHAPTER 4

CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

Overview

This work has focused on the understanding of the processing and device properties of InAs/AlSb HEMTs. A single-metallization process has been realized by selective wet chemical etching. One micron gate was achieved by contact photolithography and lift-off. The I-V characteristics of the fabricated devices have been measured and analyzed. Wet oxidation of $Al_{0.8}Ga_{0.2}Sb$ showed a surprising and significant conductivity increase. Possible reasons were given with the help of XPS analysis.

4.1   Gate metal to InAs channel short-circuiting

The cause of the excessive gate leakage current was found to be direct contact between the gate metal and InAs channel at the mesa side-wall. This arises due to the different lateral etching rate between AlSb and InAs and the reaction between AlSb and common alkaline photoresist developers. This difficulty could be alleviated by the

availability of a selective, slow etchant for AlSb over InAs. This etchant should be able to

be integrated into our fabrication process. This study has partially been done. The best

chemical we have found so far is AZ327 MIF. This indicates that special care to account

for material etching during photoresist development is required.

One solution to avoid gate metal contacting the InAs channel is adopted

from [6]: first, define the source and drain ohmic contacts, and expose the InAs channel

by chemical wet etching, then deposit the ohmic contacts metal; second, perform

Schottky-gate metallization; last do the mesa isolation. In this case, all the metal contacts,

source, drain and gate, are all located on the top layer, hence the gate metal is separated

from the channel. This has been shown in Chapter 2 on the AlGaAsSb/InAs HEMT

fabrication. And we have achieved more drain charge control.

The other solution is keeping the present process sequence: a) channel

etching; b) mesa isolation and c) source, drain, and gate metal deposition. But we should

deposit the metal all over the sample during the metallization step, and then pattern the

metal by lithography and etching. This will avoid the exposure of mesa side-wall to

developer at the last step, metal deposition, of our present work. Refractory metal

Molybdenum has the potential to be used in this solution.

4.2   Source resistance degrades the performance of HEMTs

Equation 2-1 and the relative plot Figure 2.14 show the transconductance

will reduce from intrinsic transconductance, g_0, to external transconductance, g_m, with the

presence of source resistance, R_S. We know that the high source resistance will degrade

the intrinsic transconductance g_0 to a lower value g_m. It is obvious that this will also

influence the output drain current. So we need to reduce the source resistance R_S, channel

resistance R_{CH} and drain resistance R_D to improve g_m and I_D.

Source and drain resistances, R_S and R_D, can be reduced by optimizing the

contact resistance and gate-source spacing. For the optimization study, the works of

Dvorak [1] and Boos *et al.* [19] illustrate many approaches to this problem. Modifying

the mask design to shorten the source to drain spacing can reduce R_S and R_D.

Alternatively, adding a step to the present process, depositing ohmic contact metal right

after the channel etching, can also achieve the shorter distance between metal contacts on
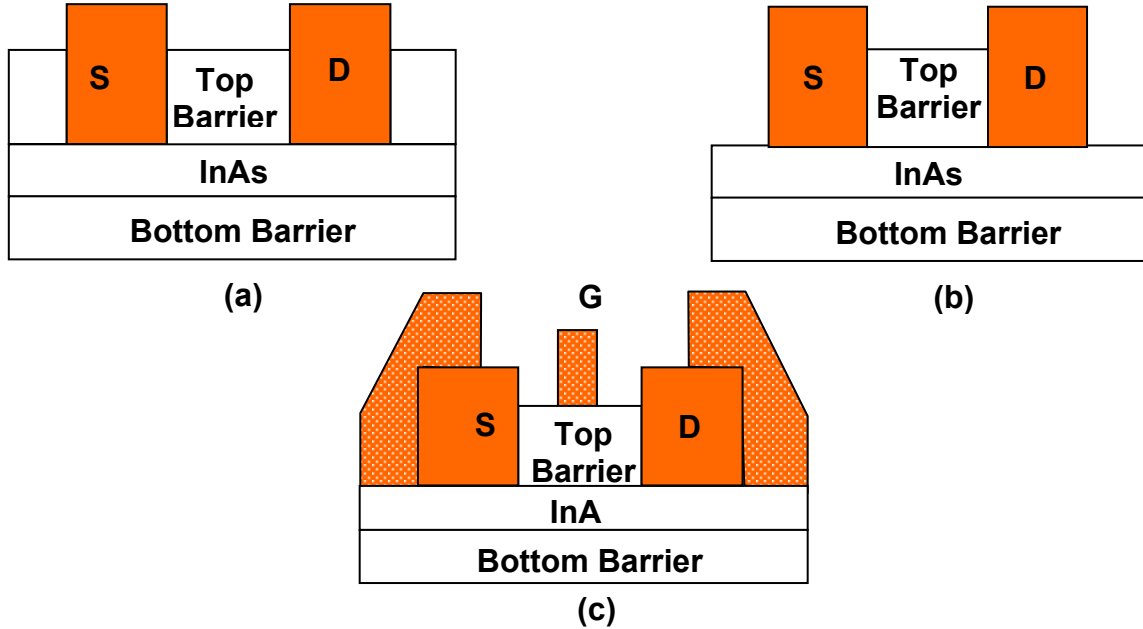
the mesa, as shown in figure 4.1.

Figure 4.1 A propose HEMT fabrication process to reduce the source resistance, R_S, by
reducing the source-drain contact spacing: (a) channel etching and source/drain ohmic
contact deposition, (b) mesa isolation, and (c) get metal and microwave measurement
bonding pad deposition.

As shown in Chapter 2, $R_{CH} = L/ (q\mu n_s W)$, reducing the channel length L while keeping the same source-drain spacing can be used to reduce the resistance under the channel. Sub-micron gate lengths can be achieved by E-beam lithography (EBL).

4.3   Wet oxidation of $Al_{0.8}Ga_{0.2}Sb$

Wet oxidations have been performed on the $Al_{0.8}Ga_{0.2}Sb$ surface. The results are surprising: the conductivity of the oxidized material increased in orders of magnitude. By the help of XPS surface analysis, we suspect it is the outdiffusion of the pure Sb during the thermal annealing of the oxide of $Al_{0.8}Ga_{0.2}Sb$ that is causing the increase of the conductivity. We still do not know the detailed oxidation mechanism of the wet oxidizing $Al_{0.8}Ga_{0.2}Sb$ process is at present unsolved and further study is required.

4.4 $Al_xGa_{1-x}As_ySb_{1-y}$ barrier layer scheme

The quaternary material AlGaAsSb is considered more durable against oxidation than AlSb by choosing an appropriate Ga mole fraction [24]. The lattice constant of AlGaAsSb can be matched to InAs with Sb mole fraction between 0.83 and 0.92. Near an Al fraction of 0.9, heterostructure AlGaAsSb/InAs heterojunctions transition from a type-II staggered band to a type-I straddling lineup [24]. This will add a valence band confinement for the holes and may help to reduce the gate leakage current. Evaluation of AlGaAsSb/InAs/AlGaAsSb HEMTs appears promising for achieving improved device transconductance.

APPENDIX A

InAs/AlSb HEMT PROCESSING TRAVELER

SOLVENT CLEANING

1. Cleave a sample and blow clean sample with N_2 gun. (Remove particles)

2. Soak the sample in cold acetone, hot methanol, and cold 2-propanol for 5 minutes (min) each. N_2 blow dry. Evaporate residual solvent on 110 ℃ hot plate (HP) for 5 minutes.

CHANNEL ETCHING

1. Spin on AZ5214-E photoresist (PR) at 5000 RPM for 30 s. (About 1.3 μm of PR)

2. Soft bake the sample at 110 ℃ for 30 s.

3. Edge bead removal:

   • Set the Karl Suss aligner to Soft Contact mode.

   • Expose for 2100 mJ/cm^2 with a well cut aluminum foil (~1.5mm from

each edges of the wafer).

- Develop for 30 sec in AZ327 MIF. Rinse in de-ionized water (DI) and

  blow dry in N_2.

- Switch sample and develop for additional 30 s to remove tweezers-mark.

- Use acetone-soaked fiberless swab to remove the PR residual.

4. Align the sample with "CHANNEL" mask in Karl Suss aligner.

5. Expose under Soft Contact mode, 175 mJ/cm^2.

6. Develop for 40 s in AZ327 MIF. Rinse the sample in DI and blow dry in N_2.

    Check the pattern transfer under a microscope. Alignment fingers should

    look clean.

7. Bake the sample at 110 ℃ for 2 min to harden the PR before etching.

8. Etch the sample in citric-acid-based solution to remove the InAs cap layer

    and the $Al_{0.6}In_{0.4}As$ layer. Then selectively etch the top AlSb barrier in

    AZ327 MIF. Shiny surface will be observed on completion.

9. Remove the PR in acetone. Solvent clean and N_2 blow dry the sample.

DEVICE MESA ISOLATION

1. Solvent clean the sample and hot plate bake the sample at 110 ℃ for 5 min.

2. Spin on PR at 5000 RPM for 30 s.

3. Soft bake the sample at 110 ℃ for 30 s.

4. Edge bead removal as in CHANNEL ETCHING.

5. Align the sample with "MESA" mask using Karl Suss aligner.

6. Expose, 175 mJ/cm^2 in Soft Contact mode.

7. Develop for 30 s in AZ327 MIF. Rinse the sample in DI and N$_2$blow dry.

8. Harden the PR before etching at 110 ℃ for 2 min on a hot plate.

9. Etch the sample in citric-acid-based solution to remove the InAs and Al$_{0.6}$In$_{0.4}$As layer. Remove the top AlSb barrier in AZ327 MIF. Then etch away the InAs channel layer by citric-acid-based solution. Finally use AZ327 MIF to remove the bottom AlSb layer. Be careful not to over etch through the Al$_{0.8}$Ga$_{0.2}$Sb to expose the underlying AlSb buffer.

10. Significantly undercut the InAs channel layer at the mesa side-wall, using Acetic acid: H$_2$O$_2$: DI (5: 10:100) to etch more than 40 s.

11. Remove PR with acetone. Solvent clean.

METAL DEPOSITION

1. Solvent clean and bake the sample at 110 on HP for 5 min.

2. Spin on the PR at 5000 RPM for 30 s.

3. Soft bake at 110 ℃ for 30 s on a HP.

4. Edge bead removal as in CHANNEL ETCHING.

5. Align the sample with "Gate" mask using Karl Suss aligner.

6. Primary expose, 150 mJ/cm^2 in Soft Contact mode.

7. Image-reversal-bake at 120 ℃ for 60 s.

8. Flood expose, 250 mJ/ cm^2.

9. Develop for 40 s in AZ327 MIF. Rinse the sample in DI and N$_2$ blow dry. Check the pattern transfer with the microscope. Gate region should look clean. If develop is not enough, additional time for developing is required. But be careful not to over do the developing in this step. (AZ327 MIF etches the AlSb layer pretty fast (~30 Å/s), it may expose the InAs channel at the mesa side-wall).

10. Load the sample into the FC1800 e-beam evaporator; pump until base pressure reaches below 1 x 10^{-6} Torr.

11. Evaporate 200 Å Ti, 200 Å Pt and 2000 Å Au respectively.

12. Soak the sample in acetone for 2 min and perform lift-off aided by syringe acetone spray.

13. Solvent clean the sample.

APPENDIX B

HEMT mask layout

The following Figures, (a), (b) and (c), are the full layout of the masks. The masks were designed using Mentor Graphics IC Station and were modified from Dr. Patrick Fay's pHEMTs masks to meet our requirements on DC and microwave measurements and device characterization.

Different sizes of devices, 10, 20, 40, and 50 µm, with different source to drain spacing, 4, 5, 6, and 7 µm can be fabricated. This mask set also provides test structures, including transmission line method (TLM) structures for contact resistance measurements, two 4 x 50 μm^2 fat FETs, and the metal pads for short and open microwave measurement calibration. The source, drain and gate bonding pads are designed for microwave-frequency testing using 100 µm-pitch coplanar waveguide probes and have a characteristic impedance of 50 µm for the GaAs substrate.
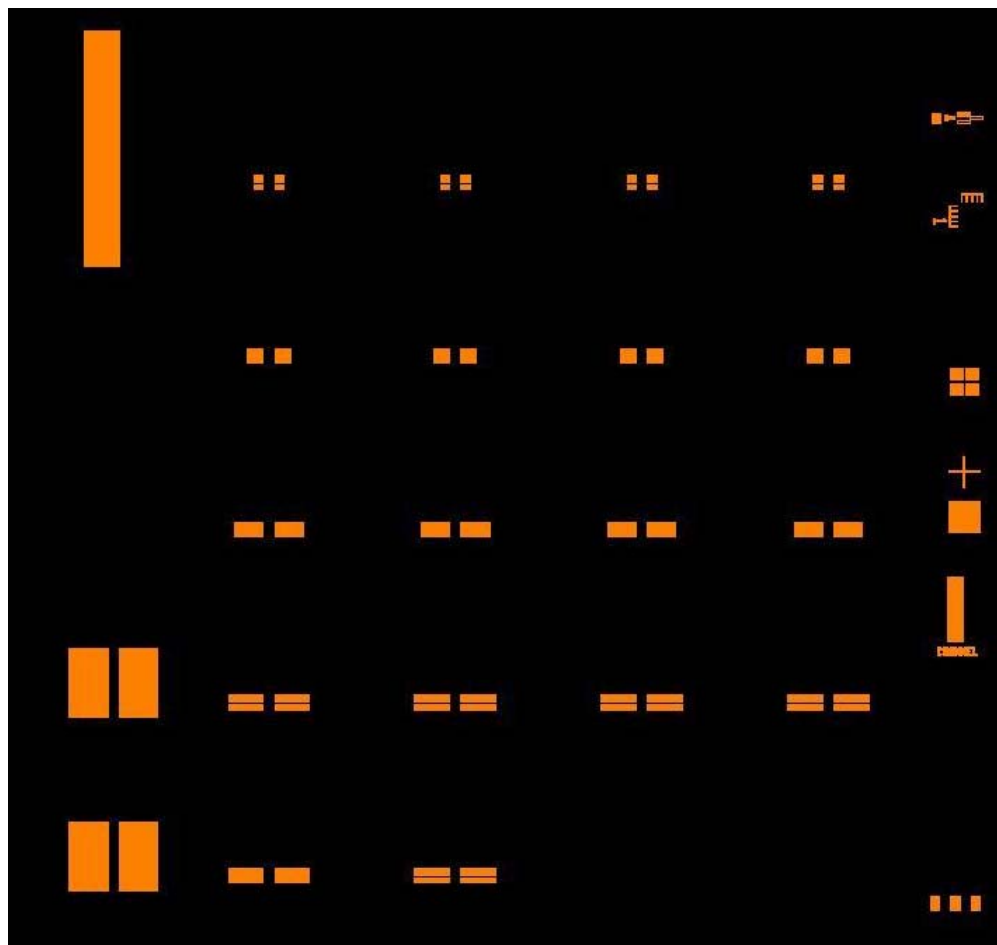
(a) Channel etching mask, "CHAN".
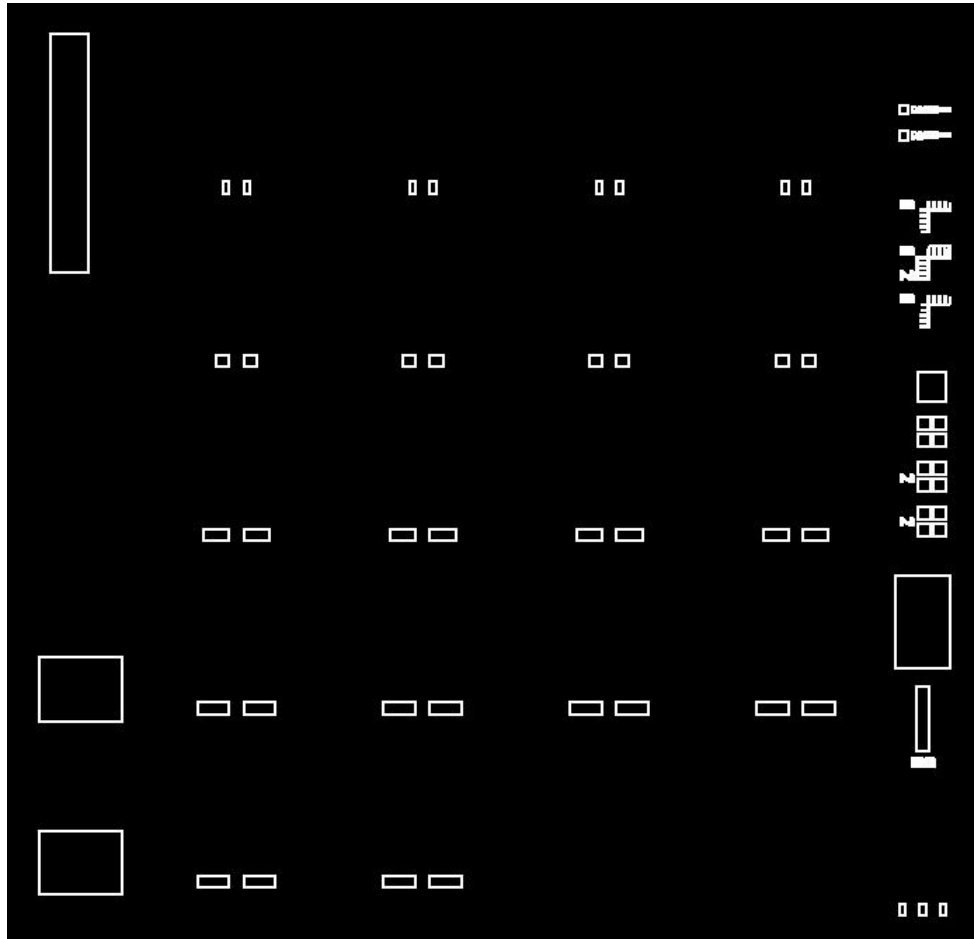
(b) Mesa isolation mask, "MESA".
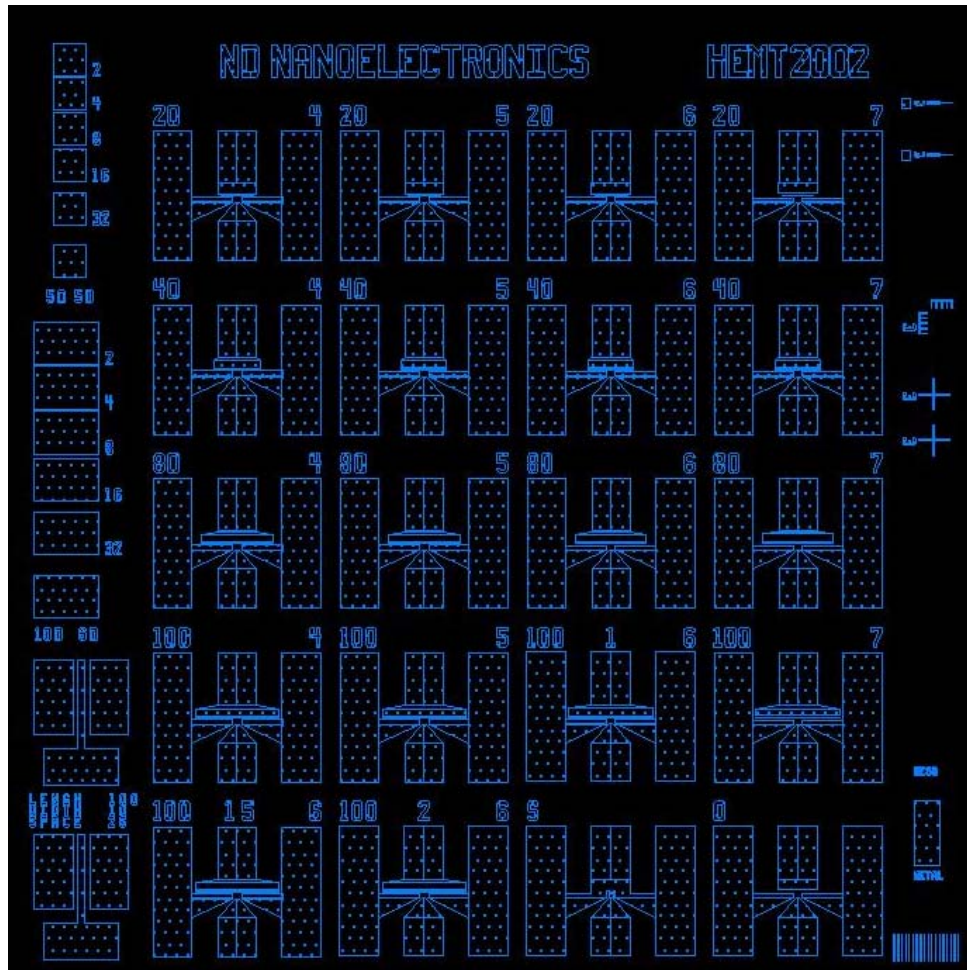
(c) Metal deposition mask, "METAL".

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