Esaki interband tunneling diodes have been demonstrated for the first time in the silicon/silicon-germanium system using ultra-high-vacuum chemical-vapor-deposition (UHV-CVD) for the Si/SiGe growth and $p^+$ doping, and proximity rapid thermal processing for the $n^+$ doping. The UHV-CVD heterostructure was grown epitaxially in a hot wall reactor at the University of Lund, Sweden. Two germanium contents were explored, 13.6% Ge and 27.6% Ge, with Esaki diodes being obtained for the 27.6% Ge concentration for a phosphorus diffusion temperature of 900 °C. The highest peak current density observed was 175 A/cm² with a peak-to-valley ratio of 2.58.
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CHAPTER 1

INTRODUCTION AND MOTIVATION

Rapidly increasing transistor density and circuit complexity have revitalized the need for solutions that can enhance circuit functionality while minimizing the number of transistors required. Power dissipation has become a major concern for high density, high frequency circuits. The tunnel diode with its multi-valued current-voltage relationship, high speed switching and low power operation is an attractive augmentation device for transistor technology [1].

The interband tunnel diode was discovered by Leo Esaki [2] in 1957. He observed a negative resistance region in the current-voltage characteristic of abrupt germanium $p$-$n$ junctions. Following the discovery, there was considerable work done on tunnel diodes in the 1960s due to the high switching speeds that the tunnel diodes were able to achieve compared to contemporary transistors. Here we present a few facts about Esaki diodes, their applications and the motivation for the current work.
1.1 The Esaki Tunnel Diode

Esaki tunnel diodes are heavily-doped $p^+ n^+$ junctions. The high doping levels lead to high electric fields and extremely thin depletion widths across which the electron can quantum-mechanically tunnel. At $p^+ n^+$ doping densities of around $10^{20} \text{ cm}^{-3}$ the built-in electric field in the Esaki diode exceeds $10^6 \text{ V/cm}$ with depletion widths in the order of 3 nm. The current-voltage (I-V) characteristic of a commercial Si tunnel diode fabricated by Microsemi Corporation [3] is shown in Fig. 1.1; this diode is no longer sold.

![Current-voltage characteristic of commercial Si tunnel diode](image)

Figure 1.1 Current-voltage characteristic of commercial Si tunnel diode [3]. Critical points on the I-V are characteristic labeled $I_p$, the peak current; $I_V$, the valley current; $V_p$, the peak voltage at which $I_p$ occurs; and $V_V$, the valley voltage at which $I_V$ occurs.

An early fabrication process for tunnel diodes was based on alloying of dopant rich metals onto heavily doped substrates of Ge [4], GaSb, Si or InP [5]. Recently, tunnel diodes have been demonstrated in SiGe [6] and III-V heterostructures grown by
molecular-beam-epitaxy [5]. Due to the nature of the fabrication processes used in the aforementioned works, integration of Esaki diodes with CMOS technology has not been possible.

1.2 SiGe Esaki Tunnel Diodes by Proximity Rapid Thermal Processing

The purpose of the current work is to develop Si-SiGe heterostructure Esaki diodes by proximity rapid thermal processing. Rapid thermal processing (RTP) is a low damage, low thermal budget doping technique which has been used to activate the dopants in Esaki diodes grown by low temperature molecular-beam-epitaxy (MBE) [7]. Proximity RTP can achieve very high doping levels, and ultra shallow junctions with low defects in comparison to ion implantation [8]. Proximity RTP is a simple process and shows promise for integration with CMOS technology; this has been one of the motivations for the present work and concurrent work being done on Esaki diodes at the University of Notre Dame.

At Notre Dame, Wang, et al. [9] demonstrated the first tunnel diodes in Si using proximity rapid thermal processing (RTP). Zhao [3] has fabricated tunnel diodes using RTP of dopants into oxide windows; this is a step in the direction of integration with CMOS technology.

The switching speed of a tunnel diode and hence its frequency of operation is proportional to its peak current density. Compared to Si, SiGe has a lower effective mass for holes and a lower bandgap and hence it can be used to improve current density by reducing the tunneling distance. However, a short tunneling distance also requires abrupt
The Esaki diode has not been used widely. Tektronix used the tunnel diode in the late 1960s in their sampling scope step generators with rise times of 25 ps [10]. Picosecond Pulse Labs still sell tunnel diode pulse generators capable of generating approximately 200 mV pulses with rise times of 20-45 ps [10].

With the development of a viable integration process of tunnel diode with CMOS technology it will be possible to explore circuit applications of tunnel diodes. One can envision using Esaki diodes for both analog and digital applications such as oscillators, mixers, detectors, amplifiers, pulse generators, flip flops, etc.,. Tunnel diode circuits are described by Scanlon [11] and Broekaert, et al. [12].

The aforementioned applications require high current density and low capacitance tunnel diodes. Going in the other direction, one can also utilize tunnel diodes with low current densities of around $10^{-6}$ A/cm$^2$ for embedded memory applications, as shown experimentally by Sorada, et al. [13]. The tunnel diode in conjunction with CMOS technology can lead to improvement in speed, area and power [1] as compared to CMOS only circuits.

There are many interesting circuits and applications that could evolve with the development and maturing of a tunnel diode integration process. Here, we propose a new application for tunnel diodes, on-chip fluid analysis [14].
1.3.1 A New Application of the Esaki Diode: On-Chip Fluid Analysis

Prof. Bernstein, from the University of Notre Dame, proposed a “laboratory-on-a-chip” blood monitoring system [15] which can analyze blood for constituents such as glucose, electrolytes, blood oxygen and carbon dioxide. Blood is introduced into channels in a semiconductor chip and moved by a microelectromechanical pump to an on-chip sensor. The pump requires a power source which is provided inductively from a power coil on an off-chip base unit to a pickup coil on the chip [16].

It has been proposed by Bernstein and Fay [17] that an LC resonant tank circuit can be used as a chemical sensor. If the value of the capacitance is made to change in response to an analyte, the resonant frequency of the tank will shift. The change in frequency can then be calibrated to determine the concentration of the analyte. In the proposed method [17], the resonant circuit is excited momentarily by an off-chip source and the resonant decay of the tank is then radiated to a receiver. The receiver measures the frequency of the decay to infer the capacitance and sense the fluid property.

For a nominal capacitance of 60 pF the inductance required for a resonant frequency of 2 GHz is 0.1 nH. At this frequency, integrated in-plane inductors have significant parasitic resistance which leads to power loss and makes it difficult to obtain tanks with a quality factor (Q) better than approximately 2. The quality factor of an LCR tank is the ratio of the energy stored in the tank to the energy lost per cycle. The oscillations from such a low Q tank lose energy and die out rapidly as shown in Fig. 1.2. With such a low Q, the resonant frequency would have to be inferred from only a few cycles of decay. By using the negative resistance of the tunnel diode to counter the resistive loss in the tank the oscillations can be extended [14].
1.3.2 Principle of Operation

The tunnel diode is connected in series with the LC tank as shown in Fig. 1.3(a). A sinusoidal voltage, $V_s$, at 1 MHz is provided by an on-chip pick-up coil. In the SPICE circuit simulation a resonant tunneling diode (RTD) model used to fit the measured I-V characteristic of a Germanium Power tunnel diode [18] has been used. A good fit was obtained in the forward direction; note that the RTD model gives a negative differential resistance (NDR) in the reverse direction as well, see Fig. 1.3(b). We ignore simulation results corresponding to the reverse characteristics, as the Esaki diode will exhibit an NDR only in the forward direction.

The principle of operation of the circuit is as follows: The tunnel diode has a DC instability in its (NDR) region [11]. This means that if the tunnel diode is DC biased in the NDR region of its characteristic, it will oscillate; the oscillations resonant with the LC
tank are selected. The 1 MHz bias source, \( V_s \), drives the tunnel diode through its NDR region where it oscillates at the resonant frequency of 2 GHz. The negative resistance of the tunnel diode compensates the tank resistance allowing the oscillations to be sustained.

Figure 1.4(a) shows the SPICE simulation results for the circuit of Fig. 1.3(a). It can be seen that the tunnel diode oscillates every time the source voltage enters the NDR of the tunnel diode. Since the tunnel diode model used has an NDR region for negative and positive voltages, oscillations occur during both the negative and positive cycles of the power supply. However, we expect oscillations to occur only for positive biases since the SPICE model is incorrect in the reverse direction. A closer inspection of the tank voltage in Fig. 1.4(b) shows that the tunnel diode has extended the duration of the oscillations to allow easier detection of the resonance frequency.
Figure 1.3 (a) LC tank circuit with a Q of 2 in series with a TD used to enhance the oscillation duration. (b) Simulated I-V characteristic of a Ge TD, obtained by fitting to a resonant tunneling diode SPICE model [18].
Figure 1.4 (a) SPICE simulation results for the circuit in Fig. 1.3(a), (b) A time scale expansion of the tank oscillations show that they occur at the desired frequency of 2 GHz.
1.4 Organization

Chapter 2 describes the physics behind the tunneling current and the factors governing the current density and heterostructure design. Chapter 3 discusses rapid thermal processing and diffusion in SiGe. Chapter 4 presents the fabrication, characterization and analysis of the Si/SiGe tunnel diodes. Conclusions and recommendations for further investigation are presented in Chapter 5. The equation for tunnel diode current density using the Wentzel-Kramers-Brillouin approximation is derived in Appendix A. Appendix B provides the detailed fabrication procedure. Appendix C presents data on wet etching of Si in 1NH₄OH: 2H₂O. Appendix D describes some results on etching experiments done on reactive ion etching of benzocyclobutene dielectric in SF₆: O₂.
CHAPTER 2

DEVICE PHYSICS AND HETEROSTRUCTURES

For $n$ and $p$ doping densities greater than $10^{19}$ cm$^{-3}$ Si is degenerate. At a doping density of $10^{20}$ cm$^{-3}$, fields higher than $10^6$ V/cm exist across a depletion region of approximately 3 nm leading to high tunneling current.

With these facts in mind we proceed to look into the tunneling probability in the Esaki diode and the physics of what gives the tunnel diode its unique current-voltage characteristic. In 1961, E. O. Kane derived relations for tunneling current density [19]. In this chapter we use the results of that work to outline the factors which determine the current density of a tunnel diode.

2.1 Tunnel Diode Current-Voltage characteristic

The behavior of the tunneling current in a degenerate $p^+ n^+$ junction can be understood by considering the computed energy band diagram of Fig. 2.1 shown at zero bias in Fig. 2.1(a). When a forward bias is applied, Fig. 2.1(b), electrons in the $n$-type semiconductor can tunnel through the narrow depletion width to the available states in the $p$-type semiconductor and the current increases; the peak current density is achieved
when the overlap between occupied states in the conduction band of the \(n\)-side and empty electron states in the valence band of the \(p\)-side is maximized.

![Graphs showing energy levels for different biases](image)

**Figure 2.1** Computed energy band diagram of an abrupt \( p^+n^+ \) junction with \( p \) and \( n \) dopant densities as \(1 \times 10^{20} \text{ cm}^{-3}\) for (a) zero bias, (b) forward bias of 100 mV, (c) forward bias of 295 mV, and (d) reverse bias of -350 mV. Simulations were done using W. R. Frensley’s BandProf program (a Poisson solver).
A further increase in the forward bias causes a decrease in the tunneling current density until $E_c$ on the $n$-side and $E_v$ on the $p$-side align, Fig. 2.1(c), and there are no more states available to tunnel to as the electrons now see the forbidden gap. Defects in the semiconductor however, can lead to states in the forbidden gap and defect assisted tunneling, a phenomenon known as the excess current. Increasing the bias, increases the thermionic current as the built-in barrier reduces. Figure 2.1(d) shows the reverse bias condition where Zener tunneling dominates and the current increases super-exponentially with reverse bias.

The diode current in the forward bias is therefore the sum of tunneling current (which dominates at low biases), excess current (present at intermediate biases and depends on the presence of defect states in the bandgap), and thermionic current (dominates at higher biases).

Tunneling can either be ‘direct’ or ‘indirect’ depending on whether the conduction band minima and the valence band maxima occur at the same point in $k$-space. The former mode can be seen in direct semiconductors like GaAs and GaSb while the latter occurs in indirect semiconductors like Ge and Si where the difference in momentum must be provided by scattering processes such as phonon and impurity scattering. Even though Si is indirect, the discussions in the thesis are limited to the direct tunneling mechanism as it is more intuitive and the results for current density in both mechanisms are similar [20].
2.2 Switching Speed

Since the depletion width of the Esaki diode is usually less than 10 nm, the capacitance is high, typically between 4 and 30 fF/µm² [5]. High frequency operation of the tunnel diode requires a high current density to change the charge on this depletion capacitance. Assuming a constant capacitance (a good first approximation as the depletion width does not change significantly over the bias range of a tunnel diode), the time required to change the charge on a capacitor $C$ from a stable bias point near the peak voltage, $V_p$, to a stable bias voltage $V_F$ beyond $V_p$ can be approximated as [21],

$$\tau = \left[ \frac{C}{I_p} \right] \frac{V_F - V_p}{1 - \left( \frac{I_v}{I_p} \right)}.$$  \hspace{1cm} (2.1)

The ratio $\left( \frac{I_p}{I_v} \right)$ is called the peak-to-valley ratio (PVR), and $\left[ \frac{I_p}{C} \right]$ is the speed index. The speed index varies over a wide range depending on the peak current density. From a compilation made by Seabaugh and Lake [5], the speed index varies between 0.003 and 31 mA/pF or mV/ps in Esaki diodes.

For a peak current density, $J_p$, of 0.1 mA/µm², with $C = 10$ fF/µm², $V_F = 900$ mV, and $V_p = 100$ mV, we plot the switching speed as a function of PVR in Fig. 2.2(a). Increasing the PVR beyond 3 is ineffective in increasing the speed of the device. Figure 2.2(b) shows that greater decrease in switching time occurs with increase in the speed index. An optimized device is one in which the peak current density is maximized while capacitance and valley current are minimized. The valley current depends on the concentration of energy levels in the forbidden gap.
Figure 2.2 Dependence of switching time on (a) PVR for a speed index of 10 mV/ps, and on (b) speed index for a PVR of 3.

Since the tunnel current density increases exponentially with decreasing depletion width and the capacitance increases inversely with depletion width, the speed index is improved by decreasing the depletion width. The highest current density in a SiGe based
Esaki tunnel diode has been achieved by R. Duschl, et al. [6] who obtained a current density of 0.126 mA/µm² in Si/SiGe tunnel diodes grown by molecular-beam-epitaxy.

2.3 Peak Tunneling Current Density

The tunneling current density through a potential barrier depends on the tunneling probability which is a function of the barrier width, barrier height and the effective mass of the carrier. The tunneling probability, given by the Wentzel-Kramers-Brillouin method, can be expressed as [22] (Appendix A)

\[ T_x \equiv \exp[-2\int_a^b |k(x)| \, dx], \]  

(2.2)

where \(|k(x)|\) is the absolute wave vector of the carrier, and \(a\) and \(b\) are the classical turning points. Since the tunneling probability depends exponentially on the tunneling distance, even small changes in the depletion width of a \(p^+n^+\) junction can improve the current density dramatically. For instance, a decrease of 2 nm in the depletion width increases the tunneling probability by a factor of \(\exp[-2k(-2 \times 10^{-9})]\). For an electron wave vector, \(k = \sqrt{\frac{2m^*_eE}{\hbar^2}} = 2.7 \times 10^9/\text{m} \) (assuming \(E \equiv E_g = 1.1\, \text{eV}\), conductivity effective mass \(m^*_e = 3 \left( \frac{2}{m^*_t} + \frac{1}{m^*_l} \right)^{-1} = 0.26 m_o\), the transverse effective mass, \(m^*_t = 0.19 m_o\), and the longitudinal effective mass, \(m^*_l = 0.98 m_o\), the tunneling probability is increased by a factor of \(5.6 \times 10^4\).
Figure 2.3 Parabolic potential barrier. The incoming electron has an energy $E$; the points $a$ and $b$ are the classical turning points in the longitudinal direction $x$.

If we assume a parabolic barrier for tunneling and an incoming electron with energy $E$, as shown in Fig. 2.3, then the tunneling probability is [22]

$$T_e \equiv \exp(-\frac{\pi m^* E_g^{3/2}}{2\sqrt{2}q\hbar F}),$$

(2.3)

where $F = \left(\frac{qV_{bi}N^*}{2\varepsilon_s}\right)^{1/2}$ is the average electric field of an abrupt junction, $qV_{bi}$ is the built-in potential energy that can be approximated by the bandgap, $N^*$ is the effective doping of the junction given by $N^* = \frac{N_A N_D}{N_A + N_D}$, where $N_A$ and $N_D$ are the doping densities of the $p$-type and $n$-type semiconductors, $m^*$ is the effective mass of the carrier, $E_g$ is the bandgap, and $\hbar$ is $\frac{h}{2\pi}$ where $h$ is Planck’s constant.

To obtain a high tunneling probability we need a low carrier effective mass, low bandgap and a high electric field. However, decreasing the bandgap reduces the built-in barrier and increases the thermionic component of the current thereby reducing the peak-to-valley ratio. For this reason SiGe, which has the lower bandgap than Si, is usually sandwiched between Si layers which reduce the thermionic emission current.
Pseudomorphically grown SiGe on Si has compressive strain due to the mismatch in lattice constants. For instance, Si$_{0.7}$Ge$_{0.3}$ has a lattice constant of 5.50 Å as compared to 5.43 Å for Si. The induced strain modifies the E-k relation, reducing the density-of-states effective mass of holes [23] and the bandgap of SiGe. This makes SiGe an attractive candidate for the tunnel diode. Further, from the technological point of view, SiGe epitaxy is becoming increasingly commonplace.

Equation (2.3) does not take into account the effect of transverse energy states. If the total energy is split into transverse and longitudinal energy components, the carrier has less energy in the tunneling direction or, in other words, the tunneling barrier increases relative to the electron energy. Accounting for the transverse energy $E_\perp$ decreases the tunneling probability by a factor of $\exp(-\frac{2E_\perp}{E})$ where $\bar{E}$ is a constant given by [22]

$$\bar{E} = \frac{4\sqrt{2}q \hbar F}{3\pi n^{*1/2} E_g^{1/2}}. \quad (2.4)$$

This factor also indicates the importance of reducing the bandgap and effective mass in order to obtain a high tunneling probability.

The tunneling current density can be expressed as (Appendix A)

$$J_t = \frac{qm^*}{2\pi^2\hbar^2} \exp\left[ -\frac{\pi n^{*1/2} E_g^{3/2}}{2\sqrt{2\hbar q F}} \frac{\bar{E}}{E} \right] D, \quad (2.5)$$

where $D$ is the overlap integral with units of energy, and is approximately equal to $q V_p$, where $V_p$ is the peak voltage, at maximum tunneling current [24].
Using the values of effective mass for light holes in strained $p$-type SiGe [23], listed in Table 1, in Eq. (2.5) for the tunneling effective mass, we can compare the current density obtained if one uses SiGe in the tunnel junction instead of Si. This is shown in Fig. 2.4.

TABLE 2.1

EFFECTIVE MASS OF LIGHT HOLES IN SiGe FOR VARIOUS Ge CONCENTRATIONS

<table>
<thead>
<tr>
<th>Ge content (%)</th>
<th>5</th>
<th>10</th>
<th>20</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m_{lh} / m_o$</td>
<td>0.19</td>
<td>0.16</td>
<td>0.10</td>
<td>0.045</td>
</tr>
</tbody>
</table>

Compiled from reference [23].

Figure 2.4 Comparison of peak current density in SiGe and Si tunnel diodes vs. Ge content.
The above comparison shows that using a Ge content of 30% could give an improvement of about 400 times in the peak current density relative to the Si homojunction diode for $n$ and $p$ doping densities of $4 \times 10^{19}$ cm$^{-3}$. The improvement that results from the use of SiGe is dependent on the doping density. At low doping densities, the depletion width is high and therefore reducing the depletion width using SiGe increases current density rapidly (due to the exponential dependence of tunneling probability on barrier width). As the doping increases, the depletion width in Si itself is narrow enough to obtain high current densities and the change brought about by SiGe is not as drastic. However, simulations still show an increase of about 30 in the current density for doping densities of $1 \times 10^{20}$ cm$^{-3}$ at 30% Ge content. Figure 2.5 illustrates the above argument for the case when the Ge content is 30%. These simulations have incorporated the effective mass and bandgap of SiGe while calculating the current density using Eq. (2.5).

![Figure 2.5 Comparison of peak current density in SiGe and Si tunnel diodes as a function of doping density. A symmetric abrupt doping profile is assumed.](image-url)
2.4 Tunnel Diode Heterostructure Design

In this work we use a Si/SiGe heterostructure for the tunnel diode fabrication. The diode consists of a highly doped $p^+$ starting substrate upon which either intrinsic or partially doped SiGe was epitaxially grown, and capped with a few nanometers of undoped Si. The Si and SiGe top layers were then doped $n^+$ by proximity rapid thermal diffusion. The final device structure after the diffusion and before contact evaporation is shown in Fig. 2.6.

![Diagram of Si/SiGe heterostructure tunnel diode](image)

Figure 2.6 The Si/SiGe heterostructure tunnel diode.

The thickness and position of the SiGe layer needs to be designed carefully in-order to get the best depletion width and highest current density possible. This can be understood from the following band diagram simulation, Fig. 2.7(a), where the position of the junction has been varied relative to the SiGe position. The simulations show an increase of 2 nm in the depletion width if the doping position varies by only 10 nm. This can reduce the tunneling probability by a factor exceeding $10^{-4}$. Figure 2.7(b) emphasizes the importance of controlling the doping parameters in proximity rapid thermal diffusion. Raising the diffusion temperature increases the diffusion coefficient leading to a slow gradient in the dopant concentration profile. This again leads to higher depletion widths.
The simulation results in Figure 2.7(b) show a change of 9 nm in the depletion width when the gradient changes from 5 nm per decade to 25 nm per decade.

Figure 2.7 Silicon/silicon-germanium heterostructure band diagrams for varying (a) doping position and, (b) active dopant slope. Simulations were done using D. W. Winston’s SimWindows program (a Poisson solver).
RAPID-THERMAL PROCESSING AND DIFFUSION IN SILICON-GERMANIUM

Rapid thermal diffusion from spin-on diffusant sources is an alternative to ion implantation. Zagozdzon-Wosik, et al. [8] give a good account of doping techniques used for shallow junction formation, their advantages and disadvantages. In ion implantation a transient-enhanced diffusion (TED) phenomenon occurs during the annealing of defects formed during the implantation; as a result junction depths are deeper than expected from bulk diffusivity models. Rapid thermal diffusion, from spin-on dopant sources spun directly onto a process wafer, should generate fewer defects and produce shallower junctions. A low defect concentration is also in aid of lower excess current and higher peak-to-valley ratio in Esaki diodes. Rapid thermal diffusion from spin-on-diffusants does have disadvantages relative to ion implantation, particularly in the removal of the spin-on diffusant after annealing and obtaining uniform-spin coating. Proximity rapid thermal processing reduces the problem related to deglazing or residue removal and lends itself toward a more uniform doping process and is chosen as the focus of our fabrication approach.

Incorporation of SiGe in the tunnel diode heterostructure affects the diffusivities of boron and phosphorus. Silicon-germanium enhances the diffusion of phosphorus [25],
while it retards the diffusion of boron [26] for Ge contents less than 40%. The enhancement in phosphorus diffusivity is small compared to the decrease in the boron diffusivity; this fact can be used to our advantage.

3.1 Proximity Rapid Thermal Processing

In our process, a spin-on diffusant (SOD) is spun over a wafer, called the source wafer, a 16-18 Ωcm $p$-type Si wafer. We use Emulsitone’s Phosphorosilicafilm $1 \times 10^{21}$ SOD with a P concentration of $10^{21}$ cm$^{-3}$. To remove the volatile organics in the SOD, the source wafers are baked in air for 20 minutes at 200 °C. The temperature is chosen based on the work in reference [8], which shows that the sheet resistance of the processed wafers is the low for a bake temperature between 150 and 200 °C for RTP experiments done in the range 50 - 600 °C. The source wafer and the device wafer are placed on top of one another, separated by quartz spacers of 0.25 to 0.45 mm, sandwiched between the wafers at the wafer edge. A Modular Process Technology RTP600S rapid thermal processor (RTP) is used; we employ spike anneal temperature profile. In the RTP600S wafers are simultaneously illuminated from both sides using tungsten halogen lamps in the presence of a gas flow. We have used N$_2$ at a flow rate of 2 SLPM. The temperature is monitored either by a thermocouple in contact with the backside of the device wafer or a using a built-in optical pyrometer. A schematic diagram of the RTP sample chamber is given in Fig. 3.1.

Figure 3.2 shows a schematic plot of a typical spike anneal profile. The spike anneal has a ramp up period, a hold period and then a fall period. The RTP600S allows control of the heating rate and hold period, while the cooling rate is dictated by the
system which is water cooled. The heating rate used uniformly for all experiments was 30 °C/s. Wang, et al. [9] successfully employed a 30 °C/s ramp rate in her Esaki process. In the recipe used for this work, the hold time was 1 s.

![Figure 3.1](image1.png)

Figure 3.1 Schematic diagram of the proximity rapid thermal annealing arrangement: (a) tungsten halogen lamps, (b) quartz spacer, (c) quartz tray with pins to hold wafer, (d) source wafer with spin-on diffusant layer, (e) device wafer, and (f) quartz chamber.

![Figure 3.2](image2.png)

Figure 3.2 Schematic diagram of a typical spike anneal profile. There are three parts in the profile: (a) ramp up period, (b) hold time and, (c) fall period.

The following figure shows the secondary ion mass spectroscopy (SIMS) results [27] for phosphorus diffusion into Si substrates by proximity RTP, for peak temperatures
of 900, 1000 and 1100 °C, using a ramp rate of 30 °C/s and a hold time of 1 s. Also shown is diffusion at 900 °C for varying ramp rates of 50 °C/s and 70 °C/s. These SIMS results are important for design of experiments and design of SiGe layer thicknesses.

![SIMS results of phosphorus diffusion by proximity rapid thermal diffusion for temperatures of 900, 1000 and 1100 °C using a ramp rate of 30 °C/s and a hold time of 1 s. Also shown are data for diffusion at 900 °C with ramp up rates of 50 and 70 °C/s.](image)

The phosphorus concentrations at the surface, exceeds the equilibrium solid-solubility limits for these temperatures; we assume that the electrically-active concentration will be limited by the solubility and that the excess is interstitially distributed. This high P concentration could also be an artifact of the SIMS measurement resulting from mass interference by SiH- bonds which has the same mass as phosphorus. The SiH- bonds could be formed during the buffered HF treatment performed just prior to loading into the RTP chamber.

It is instructive to know a few details of the kinetics of proximity RTP. The discussion that follows is from the work of Grabiec, et al. [28]. Proximity RTP consists
of several steps. Phosphorus, from the SOD layer out-diffuses to the surface, evaporates as a phosphorus oxide, $\text{P}_4\text{O}_{10}$, and is transported by gas phase diffusion to the device wafer. The oxide is adsorbed and a redox reaction follows in which the dopants are released and the Si is oxidized. The dopants then diffuse into the wafer. The thin oxide formed has to be removed after diffusion via etching in buffered HF. Figure 3.2 illustrates the process just described.

![Figure 3.4 Schematic representation of dopant fluxes during proximity RTD. The various fluxes are: $J_{d1}$, diffusion into source wafer; $J_{o1}$, diffusion within the SOD glass to SOD/Si interface; $J_o$, diffusion to the SOD surface; $J_e$, evaporation; $J_g$, gas-phase transport; $J_a$, adsorption, surface diffusion and reaction; $J_{d2}$, diffusion into the processed wafer (Adapted from Grabiec, Zagozdzon-Wosik and Lux [28]).](image)

The effect of the gap between the source and the device wafers was studied in [28]. The sheet resistance of phosphorus-diffused Si for temperatures $\leq 950 \text{ °C}$ was found to be independent of the gap, while at higher temperatures the sheet resistance increased by a factor 3 as the gap increased from 0 to 4 mm. Intuitively, reducing the gap should make gas phase transport easier and hence should decrease the sheet resistance. However, different mechanisms control the RTP process at different temperatures. At
lower temperatures, the process is limited by the activation energy required for reaction at the surface, while at higher temperatures the gas phase transport is the limiting factor. Hence at higher temperatures, bringing the wafers closer helps the gas phase transport thereby improving the doping efficiency.

Another important consideration is the presence of oxygen. At lower temperatures, increasing the oxygen content in the gas flow increases the sheet resistance of the device wafers [28]. This is because, competing oxidation of the processed wafer by P$_4$O$_{10}$ and O$_2$ impedes the redox reaction of P$_4$O$_{10}$ and therefore results in reduced dopant release.

3.2 Diffusion in SiGe

Dopant diffusivities in semiconductors depend on the concentration of vacancies and interstitials [29]. The presence of Ge has both a chemical and a strain-mediated effect on defect concentration and hence on diffusion. The chemical influence is based on the fact that the heat of sublimation of Ge is lower than that of Si [25], i.e., the atomic bonding energy of SiGe is lowered by the presence of Ge. Therefore both interstitial (I) and vacancy (V) concentrations in SiGe increases relative to Si. Biaxial compressive strain has opposing influences on I and V concentrations. Compressive strain increases the V concentration and decreases the I concentration [25].

Phosphorus diffuses via interstitials, hence the diffusivity in stressed SiGe depends on the relative strengths of the opposing influences of chemistry and stress.
Pakfar [25] notes that phosphorus diffusion does not increase significantly up to a 30% Ge mole fraction.

The diffusion of boron in SiGe is more complicated. The diffusion of boron decreases as Ge concentration is raised up to 40% Ge, and then increases for higher Ge contents [30]. The coupling between B and Ge is cited for the lowered boron diffusivity for Ge contents below 40%. A shift of diffusion mechanism from B-Ge pairing and interstitialcy diffusion to a vacancy-mediated mechanism is thought to be responsible for the increase in B diffusivity above 40% Ge [30].

The significant points of note for the Esaki diode are that the in-diffused phosphorus profile is not affected much by Ge content, while the diffusion of boron is retarded by the Ge content up to 40%, by a factor exceeding 10 at 40%. Hence, along with the attractive features of low effective mass and lower bandgap, SiGe also offers steeper B profiles than possible in Si-only Esaki diodes.
CHAPTER 4

DEVICE FABRICATION, CHARACTERIZATION, AND ANALYSIS

4.1 Epitaxial growth

To avoid defect-assisted tunneling currents a low-defect process is desirable for SiGe Esaki diodes. Defects in the device could lead to low PVR or the absence of an NDR due to defect-assisted tunneling through the forbidden gap, see Fig 4.1. The current that flows via this route, is called the excess current.

Figure 4.1 Excess current flow via energy states in the bandgap [31] is illustrated in this schematic energy band diagram of the tunnel diode.

The Si/SiGe heterostructures for this work were grown by ultra-high-vacuum chemical-vapor-deposition (UHV-CVD) at the University of Lund, Sweden. The UHV-CVD approach was chosen because it has a faster throughput than molecular beam epitaxy (MBE). It is possible to obtain doping levels higher than $10^{20}$ cm$^{-3}$. Transmission
electron microscopy studies have shown that sharp heterointerfaces can be achieved using UHV-CVD. Figure 4.2 shows the structure that was grown.

![Layer diagram of Si-SiGe heterostructure grown by UHV-CVD.](image)

Figure 4.2 Layer diagram of Si-SiGe heterostructure grown by UHV-CVD.

Even though high $p$-type doping densities have been achieved in layers grown by UHV-CVD, $n$-type layers pose a problem. Once phosphorus (the $n$-type dopant for Si) is introduced into the chamber, it is not easy to purge the chamber of phosphorus, leading to P doping of subsequently grown layers. For this reason, we have chosen to use only boron in the UHV-CVD epitaxy and introduce phosphorus by proximity rapid thermal diffusion.

The base pressure during the epitaxial growth was $9 \times 10^{-6}$ mTorr. Silane ($\text{SiH}_4$) and germane ($\text{GeH}_4$) were used as sources for the SiGe epitaxy. The $p$-type dopant source was diborane ($\text{B}_2\text{H}_6$). The substrates used were 100 mm boron doped wafers with resistivity of approximately 1 m$\Omega$-cm. The wafers were loaded at a lower temperature of 450 °C, to allow for the formation of the nucleation layer, and then ramped up to 620 °C for growth. During this period however, there is a formation of an undoped layer of less than 10 nm.
In the current work the maximum temperature the wafers were exposed to, occurred during the proximity rapid thermal processing. The growth temperature does not exceed 650 °C, while diffusion temperatures up to 900 °C were used. For this reason, the SiGe layer thickness was chosen to be around the critical layer thickness corresponding to a growth temperature of 900 °C. The critical layer thickness for SiGe, with 30 % Ge, is ~10 nm for 900 °C and ~30 nm for 650 °C [32].

4.2 Device Fabrication

After epitaxial growth the wafers were split into quarters for processing. We give a brief description of the process here; the details of the process are given in Appendix B. The quarters were first RCA-cleaned and then followed by a native oxide etch in buffered HF. The SOD was spun on the source wafers and baked in air to remove the solvents. Phosphorus was then diffused into the device wafers via proximity RTP using a spike anneal profile. In some cases, the top Si layer of the device quarter was etched in a hot (75 °C) solution of 1NH₄OH: 2H₂O, see Appendix C, before diffusion. After diffusion, the device wafers were cleaned in buffered HF for 5 minutes to remove the SOD residue [3]. The wafers were then blanket-evaporated with aluminum, for the front contact, using an Airco Temescal FC-1800 electron beam evaporator. The Al was patterned by contact optical lithography on AZ5214 photoresist used in the positive tone. Karl Suss MP3 contact aligners were used for exposure and AZ327 MIF as the developer. The wafers were then etched in the aluminum etchant Cyantec Al-12 (HNO₃, HPO₃). The photoresist was removed using acetone and ethanol at room temperature, and the devices were then mesa isolated using reactive ion etching (RIE) of Si by SF₆ with Al as the etch mask (SF₆
does not etch Al because Al fluorides are stable and nonvolatile). Figure 4.3 is a schematic of the process flow.

![Figure 4.3 Schematic of the tunnel diode process flow: (a) starting substrate, (b) proximity rapid thermal diffusion of phosphorus from a spin-on-diffusant, (c) after Al evaporation, lithography, and developing, (d) after Al etch, (e) after photoresist (PR) removal in acetone and methanol, and (f) after RIE etch of Si in SF₆.](image)

4.3 Experiments

The epitaxial structure in Fig. 4.2 was grown with the thicknesses $a = 0$ nm, $b = 25$ nm and $c = 10$ nm. Three sets of wafers were used for the experiments with (a) a Ge mole fraction of 13.6% and a boron concentration of $7 \times 10^{19}$ cm$^{-3}$, and (b) a Ge mole fraction of 27.6% and a boron concentration of $9 \times 10^{19}$ cm$^{-3}$, as determined from SIMS measurements, see Fig. 4.4, and (c) a Ge mole fraction of 13.6% and a boron concentration of $2 \times 10^{20}$ cm$^{-3}$, as estimated by the growers. The SIMS measurements were made on samples which had phosphorus diffused at 750 °C with 1 s hold time, 30 °C/s ramp rate and an N$_2$ flow rate of 2 SLPM. Note that the boron profile in the SiGe
layer falls initially at 6 nm/decade in Fig. 4.4(b), sample with 27.6% Ge, as compared to 12 nm/decade in Fig. 4.4(a), the sample with 13.6% Ge.

Figure 4.4 The SIMS results for wafers with Ge contents of (a) 13.6%, and (b) 27.6%, after phosphorus diffusion at 750 °C. The phosphorus in the bulk as seen in the SIMS is not due to the presence of phosphorus but due to the detection limit of the SIMS measurement. The dip in B concentration at about 2000 Å in (a) is because the epitaxial growth was started here and diborane flow was reduced to allow for Si nucleation.

The electrical characterization of the devices was done using a front-to-back measurement, where one contact was made to the top surface A, and the second contact to the back surface which is held by vacuum to a wafer chuck. A Cascade Microtech 11861 model probe station and tungsten probes were used for measurement. The current-voltage measurements were made using the Agilent 4155B semiconductor parameter analyzer.

4.3.1 Experiments to Establish the Process Control Variables

Wang, et al. [9] fabricated Esaki diodes using a phosphorus-diffusion temperature of 900 °C. In this work we examined a lower phosphorus-diffusion temperature of 750 °C, and varied RTP control variables such as hold time and gas flow. The diodes
fabricated at 750 °C did not show an NDR region in the I-V characteristic. Figure 4.5 shows the I-V characteristics of experiments done on the wafers with 13.6 % Ge content and boron concentration of $7 \times 10^{19}$ cm$^{-3}$. Diodes were fabricated using a spike anneal for the phosphorus diffusion, with 1 s hold time and 2 SLPM of N$_2$ for the gas flow. Here we compare these diodes with those fabricated by increasing the hold time in Fig. 4.5(a), and changing the gas flow in Fig. 4.5(b). Increasing the hold time from 1 s to 3 s to drive in the dopants, did not show a substantial change in the current density, see Fig. 4.5(a). Reducing the gas flow from 2 SLPM to 0 SLPM during the ramp-up and hold periods of the spike anneal, decreased the current density, Fig. 4.5(b). This could be because the presence of gas flow is necessary to purge the chamber and yield good diodes. The gas flow before the ramp-up period was 6 SLPM of N$_2$ for 10 s, while that after the hold period was 2 SLPM of N$_2$.

![Figure 4.5](image)

Figure 4.5 Current-voltage characteristics of experiments done on wafers with Ge mole fraction of 13.6%, boron concentration of $7 \times 10^{19}$ cm$^{-3}$, and phosphorus-diffusion temperature of 750 °C. Here we compare diodes fabricated using (a) 1 s and 3 s hold times during the RTP, (b) 2 SLPM N$_2$ gas flow and 0 SLPM gas flow during the ramp-up and hold periods of the RTP.
It can be seen from Figure 4.5, that the diodes have a reverse bias current higher than the forward bias current for biases between -0.6 V and 0.6 V. When doping levels on either the n-side or the p-side are not high to raise the valence band maximum on the p-side above the conduction band minimum on the n-side, a forward tunneling current cannot develop. The reverse current can still be strong due to zener tunneling. Such diodes are referred to as backward diodes.

The ideality factor ($\eta$) for a p-n junction (from $\exp\left(\frac{qV}{\eta kT}\right)$) is a measure of the contribution of the diffusion component and the generation-recombination (G-R) component to the total diode current. The $\eta$ for a pure diffusion current is 1, which corresponds to a 60 mV/decade slope in the I-V characteristic, while that for a single trap G-R current is 2 with the slope equal to 120 mV/decade. The G-R current dominates for biases below $\sim \frac{kT}{q}$ or 0.21 V at room temperature. A diode with both diffusion and G-R components would have an $\eta$ between 1 and 2 [33].

The diodes fabricated in the current work, see Fig.4.5, start with a 200 mV/decade slope at low biases before changing into a 100 mV/decade slope which corresponds to $\eta = 1.67$. This would mean that there is some recombination current. However, the 200 mV/decade slope at low voltages cannot be explained by a single trap state G-R current. Experiments were done on samples with the Si cap layer removed. The diodes showed an increase in current density, see Fig. 4.6(a). This indicated that the top layer in the present design was too thick and was removed for subsequent experiments to bring the P and B dopant profiles closer to each other. A band diagram simulation of the experiments
shown in Fig. 4.6(a) is given in Fig. 4.6(c). The simulations show a decrease of 2.5 nm in the depletion width upon removal of the Si cap layer. The simulations used P and B profiles close to those obtained from the SIMS measurement, Fig. 4.6(b).

Figure 4.6 Comparison of diodes with and without the Si cap layer processed using a phosphorus diffusion temperature of 750 °C, 1 s hold, and 30 °C/s ramp rate: (a) current-voltage characteristic of the diodes, (b) the SIMS results of wafers with Ge content of 13.6% and phosphorus-diffused at 750 °C, and (c) band diagram simulations of the diodes using P and B profiles based on the SIMS profiles in (b). The terms Na and Nd refer to the boron and phosphorus dopants respectively. Simulations show a decrease of 2.5 nm in the depletion width when the Si cap layer is removed.
4.3.2 Experiments Using Higher Phosphorus Diffusion Temperatures

We conclude that 750 °C is too low a phosphorus-diffusion temperature for the heterostructure design used; at this temperature, the phosphorus concentration profile is not deep and/or high enough to reach the boron profile at high dopant concentrations. This is confirmed by the SIMS measurements shown in Figures 4.4 and 4.6(b). The reason for obtaining backward diodes, Fig. 4.6(a) for example, is the steep slope of the phosphorus concentration profile, see Fig. 4.6(b). However, the boron concentration at the junction is less than or equal to $4 \times 10^{18}$, Fig. 4.6(b), resulting in depletion widths too wide for tunneling in the forward direction.

For subsequent experiments, we used phosphorus-diffusion temperatures higher than 750 °C. Figure 4.7 shows the I-V characteristics of experiments done on the wafers with: (a) Ge mole fraction of 13.6% with a boron concentration of $7 \times 10^{19}$ cm$^{-3}$, Fig. 4.7(a), and (b) Ge mole fraction of 13.6% with a boron concentration of $2 \times 10^{20}$ cm$^{-3}$, Fig. 4.7(b). All experiments used an RTP recipe with 30 °C/s ramp rate, 1 s hold time and 2 SLPM N$_2$ for the gas flow. The Si cap layer was removed in all the experiments. For the wafers described in (a), increasing the temperature to 850 °C caused a decrease in the current density due to worsening dopant profile slopes. Raising the temperature to 900 °C increased the current density due to the profiles meeting at higher junction concentration. Also shown is the I-V of a diode processed at 750 °C, which has already been discussed.

For the wafers described in (b), we obtained backward diodes for a phosphorus-diffusion temperature of 900 °C; a few diodes also exhibited an NDR region. Figure 4.7(b) shows two diodes from the sample processed at 900 °C. The diode with higher current density has a peak current density of 0.7174 A/cm$^2$ and a PVR of 1.0025.
Increasing the phosphorus-diffusion temperature to 940 °C caused the current density to decrease, see Fig. 4.7(b), due to poorer dopant profile slopes which cause the depletion width to increase. This can be understood from the band diagram simulations shown in Fig. 2.7 (b), where dopant profiles with 5 and 25 nm/decade slopes are compared. The diodes with 13.6 % Ge and boron concentration of $2 \times 10^{20} \text{ cm}^{-3}$, processed at 750 °C, do not show tunneling behavior for positive or negative biases. The ohmic-like nature of the I-V, Fig. 4.7(c), suggests a compensation of phosphorus by boron at 750 °C. This suggests that not all the phosphorus seen in the SIMS measurement is electrically active, possibly due to phosphorus being present as interstitials and not in substitutional sites. However, since the exact B concentration is not known, it is not possible to make a conclusion about the experiment.
Figure 4.7 Current-voltage characteristics of experiments done on wafers with (a) Ge mole fraction of 13.6%, boron concentration of $7 \times 10^{19}$ cm$^{-3}$, and (b) Ge mole fraction of 13.6%, boron concentration of $2 \times 10^{20}$ cm$^{-3}$. All experiments used an RTP recipe with 30 °C/s ramp rate, 1 s hold time and 2 SLPM N$_2$ for the gas flow. The Si cap layer was removed in all the experiments.

The wafers with 27.6% Ge and boron concentration of $9 \times 10^{19}$ yielded tunnel diodes for a phosphorus-diffusion temperature of 900 °C. The best peak current density was seen on the sample with the Si cap layer removed; the tunnel diode shown in Fig.4.8 has a peak current density of 175 A/cm$^2$ and a PVR of 2.58. We obtained a few low current density tunnel diodes on the sample which had the Si cap layer, Fig. 4.8 shows the I-V characteristics of two diodes from this sample. The diode with higher current density has a peak current density of 0.989 A/cm$^2$ and a PVR of 1.286. These results again indicate that the Si cap layer in the present design is too thick to obtain high current density tunnel diodes at the temperatures used. The diode fabricated at 750 °C is a forward diode.
Figure 4.8 Current-voltage characteristics of experiments done on wafers with Ge mole fraction of 27.6% and boron concentration of $9 \times 10^{19} \text{ cm}^{-3}$. All experiments used an RTP recipe with 30 °C/s ramp rate, 1 s hold time and 2 SLPM N₂ for the gas flow.

We now compare diodes from the three different wafer sets processed identically. Figure 4.9(a) is a comparison of diodes fabricated at 750 °C. The wafers with 13.6% Ge and B concentration of $7 \times 10^{19} \text{ cm}^{-3}$ (shown as A) gave backward diodes at 750 °C, while those with 27.6% Ge and B concentration of $9 \times 10^{19} \text{ cm}^{-3}$ (shown as C) gave forward diodes. This is attributed to the reduction of B out diffusion due to the higher Ge content in the latter case. At 750 °C, the phosphorus does not diffuse deep and the junction is formed just 2 to 3 nm below the surface, where the boron concentration is low as seen from the SIMS measurements. Using a higher Ge mole fraction possibly reduces the boron concentration at the junction due to the “blocking” effect of SiGe. Hence, for sample C we obtain forward diodes at 750 °C even though it has a lower bandgap owing to the higher Ge content. The diodes with 13.6% Ge and boron concentration of $2 \times 10^{20}$ cm$^{-3}$ (shown as B), processed at 750 °C, show an ohmic-like behavior, which could be because of compensation of phosphorus by boron.
Figure 4.9(b) shows a comparison of diodes fabricated at 900 °C. These I-V results are the best seen on each sample. We address the issue of non-uniformity shortly. The wafer set A (13.6% Ge and boron concentration of $7 \times 10^{19} \text{ cm}^{-3}$) gave backward diodes, but with a lower current density than the diodes from wafer set B (13.6% Ge and B concentration of $2 \times 10^{20} \text{ cm}^{-3}$); this is attributed to the higher boron concentration in B. The best tunnel diodes were obtained on the sample from C (27.6% Ge and B concentration of $9 \times 10^{19} \text{ cm}^{-3}$) because of the higher Ge content in these wafers which gives a lower bandgap and possibly steeper boron profiles due to the reduction in boron out-diffusion.

The samples processed at 900 °C show non-uniformity in the I-V characteristics. Figure 4.10 shows the local non-uniformity seen in the sample with 27.6% Ge and B concentration of $9 \times 10^{19} \text{ cm}^{-3}$ fabricated using a phosphorus-diffusion temperature of 900 °C. These diodes have a diameter of 150 µm devices and are separated by 150 µm each.
The non-uniformity is attributed to the spin-on-diffusant (SOD) thickness variation caused by spinning of the SOD over “quarter” wafers. The non-uniformity is greater in samples processed at 900 °C than at 750 °C. In the former case the depletion widths are narrow, and hence we are sensitive to process variations because of the exponential dependence of tunneling probability on the depletion width. At 750 °C the depletion width is too wide and hence we are not in the forward tunneling regime where the current density is more sensitive.

Figure 4.10 Local non-uniformity of I-V characteristic seen on the sample with 27.6% Ge and B concentration of $9 \times 10^{10}$ cm$^{-3}$ processed using a phosphorus-diffusion temperature of 900 °C. The diodes are 150 µm devices separated by 150 µm.

To conclude, it is clear that the heterostructure design has to be optimized to match a high junction concentration with a steep dopant profile slope to yield higher current densities. The design should exploit the “blocking” of boron diffusion by SiGe to obtain steep slopes. The distance between the P and the B profiles has to be reduced.
CHAPTER 5

CONCLUSIONS AND FUTURE DIRECTIONS

5.1 Conclusions

The present work demonstrates the fabrication of tunnel diodes in the Si/SiGe heterostructure, combining the techniques of ultra-high-vacuum chemical-vapor-deposition for epitaxial growth, and proximity Rapid Thermal Processing (RTP) for shallow junction formation. Wafers with 27.6% Ge content yielded tunnel diodes owing to the lower bandgap than samples with 13.6% Ge, and possibly due to reduction of boron out-diffusion at higher Ge content which gives steeper B slopes at the junctions. The highest current density observed was 175 A/cm² with a peak-to-valley ratio of 2.58. A large variation in current density was observed around the wafer; this is attributed to the non-uniform spin-on diffusant thickness. Increasing the boron concentration to higher than 7 x 10¹⁹ cm⁻³ in the 13.6% Ge samples gave poor results probably due to compensation of phosphorus by boron.

Experiments were done for temperatures between 750 °C to 940 °C for the phosphorus diffusion by proximity RTP. The optimum temperature for fabrication of the Esaki diodes using the present heterostructure design was found to be 900 °C. The
experiments show that it is necessary to match a high junction concentration with a good
dopant profile slope. The experiments have given considerable insight into the important
factors concerning Esaki diodes. In-order to obtain higher current densities, future design
of the heterostructure needs to be done carefully with these factors in mind.

5.2 Future Directions

In order to obtain concentration profiles with steeper slopes one could use arsenic
for the $n$-type dopants. Eguchi, et al. [34] notes that the diffusivity of As in Si$_{0.8}$Ge$_{0.2}$ is
three times lower than that of phosphorus and could be better for shallow junction
formation compared to phosphorus.

Another possible way to achieve better slopes is to use SiGeC in the place of
SiGe. SiGeC reduces the diffusion of Boron and Phosphorus [35]. This is because
introducing carbon reduces the number of interstitials and increases the number of
vacancies, and hence SiGeC retards the diffusion of dopants such as P and B which
diffuse via interstitials. The SIMS results shown in Fig. 3.3 show a steeper slope in the
phosphorus concentration profile for a ramp rate of 50 °C/s compared to 30 °C/s.
Increasing the ramp rate is another possible direction for obtaining better dopant slopes.

A complete characterization of this work needs more SIMS analysis of the
phosphorus and boron diffusion at temperatures of interest. The position of the boron
profile can be varied and the current-voltage characteristics for each experiment can be
obtained. Figure 5.1 shows the band diagram simulations of a proposed experiment in
which the distance between the boron profile and the surface is varied. The simulated
structure has a Si cap layer below which we have 10 nm of SiGe, of which 5 nm is doped
$p^+$. The cap layer thickness is varied to bring the profiles closer; the thicknesses are 10
The depletion width changes from 7.64 nm for the 10 nm cap layer to 5.27 nm for the 0 nm cap layer. The depletion width for each case is shown in the plot. The data from the electrical characterization and the SIMS measurements would provide a conclusive picture of what fraction of the dopants seen in the SIMS analysis are electrically active at the junction.

Figure 5.1 Effect of changing the distance between P and B profiles by changing the Si cap layer thickness: (a) assumed doping profiles of P and B for the purpose of band diagram simulations, with a maximum active concentration of $10^{20}$ cm$^{-3}$ for P and B, and (b) Band diagram simulations for varying Si top layer thickness for the structure which has Si cap over 5 nm of undoped SiGe over 5 nm of $p^+$ SiGe. The depletion width for each case is shown. Simulations were done using D. W. Winston’s SimWindows program (a Poisson solver).

To conclude, this study is a step in the direction of obtaining high current density, high speed tunnel diodes, using a simple fabrication process which may be integrated with transistor technology. The ultimate aim being to provide design versatility in circuit applications and to solve the major issues concerning the VLSI industry today, namely transistor density and power dissipation.
APPENDIX A

DERIVATION OF CURRENT DENSITY OF AN ESAKI DIODE

A.1 Wentzel-Kramers-Brillouin Approximation

The tunneling of an electron through a potential barrier in the presence of an electric field is a quantum-mechanical process seen in metal-semiconductor junctions and p-n junctions in highly doped semiconductors. The derivation of current density due to tunneling requires knowledge of the tunneling probability. The Wentzel-Kramers-Brillouin (WKB) approximation is often used for the tunneling probability and can be derived from the Schrödinger equation [36].

The time independent Schrödinger equation is:

\[
-\frac{\hbar^2}{2m^*} \frac{d^2 \psi(x)}{dx^2} + V(x)\psi(x) = E\psi(x),
\]

where \( V(x) \) is the potential energy, \( E \) is the energy of the electron, \( \psi(x) \) is the wave function, \( x \) is the position and \( m^* \) is the effective mass of the electron.

The WKB approximation basically assumes that the variation in the potential energy \( V(x) \) is slow with respect to the wavelength of the electron, \( \lambda \). The solution to Eq. (A.1) is

\[
\psi(x) = A \exp(\pm k(x)|x|),
\]

where \( k(x) \) is the wave number.
where, \( k(x) = \sqrt{\frac{2m^*(x) - E}{\hbar^2}} \); we keep the decaying exponential solution to Eq. (A.1) and discard the exponentially increasing solution as nonphysical.

Assuming \( V(x) \) is constant between \( x \) and \( x + dx \) allows us to assume that \( k(x + dx) \) is equal to that at \( k(x) \).

\[
\psi(x + dx) = A \exp(-|k(x)|(x + dx)) \quad (A.3)
\]

and

\[
\frac{\psi(x + dx)}{\psi(x)} = \exp(-|k(x)|dx). \quad (A.4)
\]

Therefore the wave function, of an electron tunneling between points \( a \) and \( b \) of a slowly varying potential, at the position \( b \) can be related to that at \( a \) by

\[
\frac{\psi(b)}{\psi(a)} = \exp\left(-\int_a^b |k(x)|dx\right) = \exp\left(-\int_a^b \sqrt{\frac{2m^*(x) - E}{\hbar^2}} dx\right). \quad (A.5)
\]

Therefore the tunneling probability is

\[
\left|\frac{\psi(b)}{\psi(a)}\right|^2 = \exp\left(-2\int_a^b |k(x)|dx\right) = \exp\left(-2\int_a^b \sqrt{\frac{2m^*(x) - E}{\hbar^2}} dx\right). \quad (A.6)
\]

If \( T_t \) is defined as the tunneling probability, then

\[
T_t = \exp\left(-2\int_a^b |k(x)|dx\right). \quad (A.7)
\]

### A.2 Tunneling Current Density of the Esaki diode

Here we derive the relation for current density in an Esaki diode for tunneling through a parabolic potential barrier in the longitudinal direction of transport. The current density in the longitudinal direction in the energy range \( dE_x dE_{\perp} \), where \( E_x \) is the energy...
associated with momentum in the longitudinal direction $k_x$ and $E_\perp$ is energy associated with the transverse momentum $k_\perp$, can be expressed as

$$dJ_x = \frac{2q}{h} dE_x N_t F(E) T_t,$$  

(A.8)

where $\frac{2q}{h}$ is the current per unit longitudinal energy [5], $N_t$ is the number of transverse states, $F(E)$ is the Fermi function, and $T_t$ is the tunneling probability.

If we consider a ring in the transverse k-space then the number of transverse states $N_t$ in the ring is the density-of-states in 2-dimensional k-space multiplied by the area of the ring.

$$N_t = \frac{1}{(2\pi)^2} (2\pi k_\perp dk_\perp)$$  

(A.9)

Equation (A.8) therefore becomes

$$dJ_x = \left(\frac{2q}{h} dE_x\right) \frac{1}{(2\pi)^2} (2\pi k_\perp dk_\perp) T_t F(E).$$  

(A.10)

Rearranging,

$$dJ_x = \left(\frac{q}{h/2\pi} dE_x\right) \frac{1}{(2\pi)^2} (2k_\perp dk_\perp) T_t F(E).$$  

(A.11)

Now, since the transverse masses in Si are equal, the transverse energy can be conveniently expressed as, $E_\perp = \frac{\hbar^2 k_\perp^2}{2m^*}$, which means that

$$2k_\perp dk_\perp = \frac{2m^*}{\hbar^2} dE_\perp.$$  

(A.12)

Hence
\[ dJ_x = \left( \frac{q}{\hbar} \frac{dE_x}{dE_y} \right) \frac{1}{(2\pi)^2} \left( \frac{2m^*}{\hbar^2} dE_{\perp} \right) T \cdot F(E) \]

\[ dJ_x = \frac{q m^*}{2 \hbar^3 \pi^2} dE_x dE_{\perp} T \cdot F(E) \]

(A.13)

Considering that for the electrons to tunnel through we need empty states or holes available on the \( p \)-side,

\[ dJ_x = \frac{q m^*}{2 \hbar^3 \pi^2} dE_x dE_{\perp} T \cdot F(E) (1 - F(E)) \]

(A.14)

Figure A.1 Band diagram of a \( p^+ n^+ \) junction showing the tunneling points \( a \) and \( b \). The applied voltage is \( qV \) and the bandgap is \( E_g \).

The net current is the difference between the current flowing due to electrons from conduction to valence band and from valence to conduction band. Assuming that the mass on the \( n \)-side and the \( p \)-side are equal, and using a change of variable from \( E_x \) to total energy \( E \) using the fact that
\[ E = E_x + E_\perp \]  \hspace{1cm} (A.15)

\[ dJ_x = \frac{qm^*}{2\hbar^3 \pi^2} dE_x \, dE_\perp \, T_x \left[ F_x(E_x)(1 - F_x(E_\perp)) - F_y(E_x)(1 - F_y(E_\perp)) \right] \]  \hspace{1cm} (A.16)

\[ dJ_x = \frac{qm^*}{2\hbar^3 \pi^2} dE_x \, dE_\perp \, T_x \left[ F_x(E_x) - F_y(E_\perp) \right] \]  \hspace{1cm} (A.17)

The tunneling probability for a parabolic barrier, derived in reference [22], is

\[ T_x \cong \exp \left( -\frac{\pi m^{*1/2} E_x^{1/2}}{2\sqrt{2}\hbar F} \right) \exp \left( -\frac{2E_\perp}{E} \right), \]  \hspace{1cm} (A.18)

where \( E \) is a constant given by

\[ \bar{E} = \frac{4\sqrt{2}q\hbar F}{3\pi m^{*1/2} E_y^{1/2}}. \]

Combining equations A.18 and A.17 and integrating over the transverse and total energies to obtain the current density,

\[ J_x = \frac{qm^*}{2\hbar^3 \pi^2} \exp \left( -\frac{\pi m^{*1/2} E_x^{1/2}}{2\sqrt{2}\hbar F} \right) \int \left[ \int \exp \left( -\frac{2E_\perp}{E} \right) dE_\perp \right] \left[ F_x(E_x) - F_y(E_\perp) \right] dE_x \]  \hspace{1cm} (A.19)

Integrating over \( E_\perp \) with limits \( 0 < E_\perp < E_1 \) or \( 0 < E_\perp < E_2 \), depending on which is smaller because the transverse energy must be conserved. For instance, if the electron energy is \( E_1 \), then the maximum transverse energy it can have and still tunnel in the longitudinal direction is \( E_1 \). This transverse energy must be conserved during tunneling, which means if \( E_2 \) (maximum transverse energy it can have after tunneling) is less than \( E_1 \), then only those electrons with transverse energy of up to \( E_2 \) on the \( n \)-side can tunnel. The limits on the total energy is given by the voltage applied, \( qV \).
\[ J_t = \frac{q m^*}{2 \hbar^3 \pi^2} \exp\left(-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}q\hbar F}\right) \int \left[1 - \exp\left(-\frac{2E}{E}\right)\right] \left[F_c(E_1) - F_v(E_2)\right] dE \]  

(A.20)

where \( E_x \) is the smaller of \( E_1 \) and \( E_2 \) from Fig. A.1.

If we define \( D = \int \left[1 - \exp\left(-\frac{2E}{E}\right)\right] \left[F_c(E_1) - F_v(E_2)\right] dE \), called the overlap integral, then the \( J_t \) simplifies to [22]

\[ J_t = \frac{q m^*}{2 \hbar^3 \pi^2} \exp\left(-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}q\hbar F}\right) \left(\frac{E}{2}\right)^{1/2} D. \]  

(A.21)

We use Eq. (A.21) for the calculation of tunneling current density in our comparison of SiGe and Si Esaki diodes. For the current density in a SiGe tunnel diode we use the effective mass and bandgap of SiGe corresponding to the Ge mole fraction used.
APPENDIX B

DETAILED TUNNEL DIODE PROCESS DESCRIPTION

Remove spin-on diffusant (SOD) from refrigerator 24 hours before use
- Cleave wafer into quarters and label

Clean-up

1. RCA1 (1 NH₄OH: 1 H₂O₂: 5-10 DI: ) bath, 75 °C, 10 min. Rinse 2 min in DI
2. RCA2 (1 HCl: 1 H₂O₂: 5-10 DI: ) bath, 70 °C, 10 min, Rinse 2 min in DI
3. Etch off surface oxide in buffered HF (BHF) 25 s
4. Rinse in DI water and blow dry in N₂

Si Etch

8. Prepare 100 ml NH₄OH: 200 ml H₂O (Si etchant)
9. Etch Si for required time (etch rate 141 nm/min)

Source Wafer Preparation

10. Coat a dummy wafer with IPA. Spin 1000 rpm 10 s, 3000 rpm 30 s (To prevent SOD from adhering to spinner)
11. Spin phosphorus SOD Emulsitone 1 x 10²¹ on wafers. Spin program: 1000 rpm 10 s, 3000 rpm 30 s
12. Hot plate bake source wafers at 200 °C for 20 min to remove organic solvents in SOD. NOTE: baking the phosphorus SOD film causes fumes, so perform bake in a vented place

Removing Oxide Before Diffusion

13. Dip in BHF for 30 s just before loading into rapid thermal processor RTP600S to remove native oxide
Phosphorous Proximity Rapid Thermal Diffusion

14. Load wafers into RTP600S for proximity diffusion. Program the RTP for a ramp rate of 30 °C/s, 1 s hold time, and 60 s fall time, with a N₂ flow rate of 2 SLPM.
15. After diffusion, clean device wafers in BHF for 5 minutes to remove SOD residue.

Oxidation/Post-diffusion Bake

16. Hotplate bake 200 °C, 1 hr. (removes H, promotes Al adhesion)

Evaporation of Front Al contact

17. Evaporate 3000 Å of Al at a base pressure below 1.5 x 10⁻⁶ Torr
18. Measure the Al thickness

Pattern for Al contact Etching

19. Spin photoresist adhesion promoter HMDS at 1000 rpm 10s, 3000 rpm 30s
20. Spin on photoresist (PR) AZ 5214-E at 1000 rpm 10s, 3000 rpm 30 s (PR thickness 1.4 - 1.5 µm)
21. Soft bake at 90 °C, 1 min to remove solvents
22. Measure lamp intensity of Karl Suss. Expose the wafers for 180 mJ/cm² using the SIRT2 mask
23. Develop in AZ327 MIF developer, 35-38 s, and rinse in DI water, and blow dry
24. Dip into Cynatec Al-12 aluminum etchant for 3-5 min. The etch rate is about 600-800 Å/min. Rinse in DI water twice and blow dry (Al etchant viscous, a thorough rinse is required)
25. Soak in acetone and methanol for 30 s each to remove the PR

Mesa Isolation Etch

26. Etch Si by RIE using SF₆ at a flow rate of 26 sccm, pressure of 30 mTorr, RF power of 200 W for 20 s (Expected etch depth = 0.23 µm).
APPENDIX C

SILICON WET ETCHING IN 1NH₄OH: 2H₂O

In this work, it was required to etch a 10 nm Si layer with high selectivity against etching SiGe. The etch recipe used was 1NH₄OH: 2H₂O kept at 75 °C. This etch recipe was based on the work of Wang, et al. [37] which shows a selectivity of 267:1 for 10 weight percent of NH₄OH in water at 75 °C. The etch rate is 64 nm/min for Si, and 0.24 nm/min for Si₀.₇Ge₀.₃.

Since NH₄OH is highly volatile, care has to be taken that the conditions for each etch experiment is kept the same. The wafers were first RCA cleaned, followed by a native oxide etch in buffered HF (BHF) for 30 s. The etch solution was prepared using 100 ml NH₄OH: 200 ml H₂O and then heated at 75 °C. The Si etch was performed consistently 10 minutes after preparing the etch solution. Gold/ titanium was used as the etch mask for this experiment. After the etch, the Si surface was hydrophilic, indicating the presence of an oxide. Wang, et al. notes the formation of such a porous oxide through which the OH⁻ diffuse through and attack the Si surface. This oxide was removed by a short (25 s) BHF etch. The etching experiments were performed on four different samples etched for 20 s, 40 s and 60 s. The etch calibration, obtained in our lab is presented in Fig. A.1. The etching of Si using this solution is slow to start in the first 15 s, after which
the etch rate is 197 nm/min. If the etch graph is forced to fit through zero, Fig. A.1., the etch rate is 141 nm/min. The two points shown for each etch time correspond to two etch depth measurements at different positions on the same sample. This etch recipe was used for etching the Si cap layer in our devices. The etch times used for the devices were between 30 and 40 s. Because this etch is selective against SiGe we used slightly etch times higher than required to ensure removal of the Si cap layer.

Figure C.1 Etching of Si using 1NH₄OH: 2H₂O at 75 °C.
APPENDIX D

BENZOCYCLOBUTENE DIELECTRIC REACTIVE ION ETCHING IN SF$_6$/O$_2$

A low $\varepsilon$ interlayer dielectric with the resolution of 1 $\mu$m is desired for future processing of tunnel diodes. Benzocyclobutene (BCB), a product of Dow Chemicals, with a $\varepsilon$ of 2.65 was chosen as the dielectric. Benzocyclobutene is a silicon-containing spin-on polymer. The presence of silicon gives BCB good adhesion to Si [38] while having a lower dielectric constant compared to SiO$_2$. It is possible to etch less than 1 $\mu$m trenches in BCB using projection lithography [39]. Benzocyclobutene can be etched by reactive ion etching (RIE) in O$_2$ ambient, but the etch rate is slow, approximately 5 nm/min, because O$_2$ does not etch the Si in BCB [38]. Therefore a halogen based etchant such as SF$_6$ or CF$_4$ must be used along with O$_2$. The oxygen etches the organic content of BCB and SF$_6$ etches the Si.

The photoresist AZ5214 was used as a mask. It was decided to use the SF$_6$/O$_2$ mixture to etch BCB in the present work. We have measured the etch rates of BCB, Si, and photoresist (PR), since the Si and PR removal are also important for any device application. The RIE etch recipe used was an SF$_6$/O$_2$ mixture with flow rates of 3.3/30 sccm. The pressure in the chamber was 300 mTorr and the power was 54 W. The DC bias voltage for these conditions varied between 32 and 34 V. The Si, BCB and PR were
etched simultaneously for 1, 3, 4 and 5 minutes on separate pieces. Figure D.1 shows the etch configuration including the substrate being etched and the mask layer.

The wafers were prepared as follows. The Si wafers were RCA cleaned and then etched in BHF for native oxide removal. On the sample for BCB etch calibration, the adhesion promoter for BCB, AP3000, was spun at 1000 rpm for 10 s and 3000 rpm for 30 s. Benzocyclobutene was spun over the adhesion promoter at 1000 rpm for 10 s and 5000 rpm for 30 s. The BCB is then cured at 300 °C by rapid thermal processing in the RTP600S using a ramp rate of 22 °C/s and a hold time of 53 s with a N₂ flow rate of 10 SLPM during the ramp up and hold periods and 20 SLPM during the cooling period. This recipe gave a BCB thickness of about 0.9 - 1.0 µm. Then photoresist was spun over the BCB for masking and was patterned via contact lithography. The spin recipe was 1000 rpm for 10 s and 4000 rpm for 30 s which gave a PR thickness of 1.3 µm. The energy of exposure used was 180 mJ/cm². After each etch the PR is removed using acetone and methanol treatment. Since the photoresist-protected BCB is not etched, this step can be profiled to obtain an etch depth.

An evaporated Al layer, patterned and etched, was used as the mask for Si etching. The difference in the height of Al and the Si surface gives the Si etch depth. For the calibration of PR etch rate, the PR was spun on Al and then patterned. After etching the PR, the difference in PR height and Al surface gives the etch rate.
Figure D.1 Schematic description of the reactive ion etching of (a) Si, (b) photoresist, and (c) benzocyclobutene in SF$_6$/O$_2$. The left and right drawings show the before and after etch configurations, respectively.

Figure D.2 shows the etch rates for Si, BCB and PR. The etch rates of BCB and PR are comparable, 185 and 156 nm/min respectively. The etch rate of Si is slow, 8 nm/min. The error bars shown on the graphs show the etch depth variation over the samples. The samples used were quarters from 100 mm wafers. Two measurements were taken for each sample, from the middle and the edge of the quarter.
Figure D.2 Etch depth vs. time for (a) Si, (b) BCB, and (c) AZ5214 photoresist.
BIBLIOGRAPHY


