CALL FOR PAPERS

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Special Topic on
Steep Slope Transistors for Energy-Efficient Computing & More

Guest Editor: Alan Seabaugh, University of Notre Dame, seabaugh.1@nd.edu

Editor-in-Chief: **Azad Naeemi**, Georgia Institute of Technology, azad@gatech.edu

Aims and Scope: Tunnel field-effect transistors (FETs) and other low-subthreshold-swing steep-slope (SS) transistors hold promise to outperform complementary metal-oxide semiconductor technology (CMOS) at low voltage and realize more energy-efficient logic for computation. The aim of this special topic is to highlight experimental advances and ideas that make SS transistors attractive for integration with CMOS, to realize better power-performance logic. Aspirational characteristics for n- and p-type steep transistors can be summarized as follows: drain currents exceeding 200 μA/μm at a supply voltage below 0.4 V, with SS less than 60 mV/decade beginning near 1 μA/μm and spanning more than 4 decades. Papers describing theory and modeling of transistors which can meet and surpass these goals are of interest, as are papers which assess the full design stack from devices to circuits and architecture to applications to identify system bottlenecks and inform technology development for computing, communications, or other applications. Materials approaches are not restricted to Si CMOS and can be based on any semiconductor technology and incorporate multiferroic or other performance boosters. New approaches based on three-dimensional integration, heterogeneous integration, processing, or insights from manufacturing are also within the scope of this issue to advance understanding and progress in SS transistors.

Topics of Interest:

- Steep slope transistors with path to outperform CMOS at low voltage
- Experimental progress, theory, and modeling
- Si, III-V, III-N, two-dimensional semiconductors and heterojunctions
- Multiferroic, including ferroelectric, and & other slope boosters
- Alternative materials/device design approaches
- 3-D integration, heterogeneous integration, processing, manufacturing
- Full-stack design to inform technology development

Important Dates:

- Open for Submission 1 June 2023
- Submission Deadline 1 Sept. 2023
- First Notification 1 Oct. 2023
- Revision Submission 15 Oct. 2023
- Final Decision 15 Nov. 2023
- Online Publication 1 Dec. 2023