NANOSCALE SOLID POLYMER ELECTROLYTES IN METAL–INSULATOR–CONDUCTOR SYSTEMS FOR LOGIC AND NEUROMORPHIC DEVICES

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Abstract

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This research aims at using ions to add new functionality to semiconductor devices. Electrically-insulating, ion-conducting polymers, such as poly(ethylene oxide) (PEO), with ion salts like cesium perchlorate ($CsClO_4$), are known as Solid Polymer Electrolytes (SPEs). These can be coated on a semiconductor and internal or applied electric fields can move the ions to the semiconductor interface, where they attract charge carriers of opposite polarity to form an electric double layer (EDL). This can be used to reversibly configure the semiconductor surface charge carrier profiles, e.g. to form *p*-*n* and tunneling junctions and to convert metal-oxide-semiconductor field-effect transistors (MOSFETs) from *n*-FETs to *p*-FETs to tunnel FETs (TFETs). SPEs can also dope 2D crystals and carbon nanotubes (CNTs), which are difficult to dope substitutionally. SPE capacitors with an added charge retention layer could lead to new forms of digital and analog memory at the scaling limits of the polymer. Additionally, capacitor or transistor structures may be used as weight storage devices to accelerate the training of deep

learning systems, as well as in other neuromorphic devices based on coupling ions and electrons. However, EDL devices have various fundamental and technological limitations. It is important to understand the EDL formation and dissipation speeds, polymer thickness limitations, and forms of ion encapsulation to enable further lithography.

This research is intended to deepen the understanding of the static and dynamic response of ultrathin PEO in metal insulator semiconductor (MIS) and metal insulator metal (MIM) structures with and without $CsClO_4$. While SPEs are typically studied in micron-thick films, this dissertation explores decananometer thicknesses for their potential to increase the ion response time, since certain bulk properties, e.g. PEO's ionic conductivity, are known to change in polymers confined in one dimension.

Record-thin films of PEO:$CsClO_4$ are demonstrated on commercial Si-on-insulator wafers and carbon nanotubes (CNTs) on quartz. Spin-coated PEO:$CsClO_4$ as thin as 7.8 nm, a physical thickness relevant to nanoscale device applications, is characterized in cross–sectional images by transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS), to reveal the coating of structures with nanometer features. Through EELS analysis, the polymer's amorphous carbon character is distinguished from the sp^2–hybridized carbon of the CNT. With SiO_2 evaporated over the PEO, Cs is observed to be contained within PEO, indicating encapsulation by the SiO_2, which can serve as a capping layer for further lithography. EELS mapping reveals the unbiased accumulation of Cs at the PEO/SiO_2 interface due to the built-in electric

field. In the coating of 2-nm-diameter CNTs, EELS mapping shows that PEO:$CsClO_4$ closely surrounds the CNT wall, with no indication of interlayers, as desired for electric double layer formation used in transistors and memory.

These nanometric SPE films are modeled in COMSOL Multiphysics, using the Poisson and Nernst-Planck equations modified to account for a finite ion size. The films' static and dynamic behavior in response to a constant bias, a voltage step, and a bipolar triangular pulse train is simulated and compared to measurements in ultrathin PEO:$CsClO_4$ MIM capacitors.

The impedance–frequency and capacitance–voltage characteristics of PEO MIS capacitors at thicknesses relevant to transistor technology are measured with and without $CsClO_4$. Basic understanding of the impedance frequency and voltage characteristics of this MIS system is established in spin-coated films in the thickness range from 6 nm to 19 nm, as determined from capacitance and TEM measurements. Estimates of the dielectric constant, energy band diagram, charge trap density, and conductivity in ultrathin PEO are obtained. Simple equivalent circuits based on resistive and capacitive elements that reflect the physical system are used to model the measured impedance frequency trends and compare films with and without $CsClO_4$ in the polymer matrix. This study reveals the physical characterization and the simulated and measured electrical properties of PEO near the limits of thickness scaling, toward memory and neuromorphic device applications.

This is for Adriana Olivia Serrano Córdova and Carlos Fernando González Guerra, my wise and loving parents, for Gerónimo González de la Garza, the kind and inspiring physician I am lucky to call my grandfather, and for everyone who believed in me.

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SYMBOLS AND ABBREVIATIONS

a	Effective ion diameter
A	Area of top electrode, labeled "gate"
AFM	Atomic force microscopy
C	Capacitance
c_{+0}, c_{-0}	Initial molar concentration of cations, anions in mol/m^3
c_{+MAX}, c_{-MAX}	Max. molar concentration of cations, anions
C_B	Bulk capacitance in F
C_E	EDL circuit parameter in F, $C_E = C_{EDL1}C_{EDL2}/(C_{EDL1}+C_{EDL2})$
C_{EDL}	EDL capacitance in F
C_G	Geometric capacitance in F
CNT	Carbon nanotube
C_P	Parallel capacitance density
$CsClO_4$	Cesium perchlorate salt
D_+, D_-	Diffusivity of cations, anions in cm^2/s
E_C	Minimum conduction band energy in eV
EBL	Electron-beam lithography
EDL	Electric double layer
EDLT	Electric double layer transistor
EELS	Electron Energy Loss Spectroscopy
E_G	Band gap energy in eV
E_V	Maximum valence band energy in eV
f	Frequency
FET	Field-effect transistor
G	Conductance, $1/R$
G_P	Parallel conductance per unit area
HRTEM	High–resolution transmission electron microscopy
I	Current
I_D	Drain current
J	Current density (I/A)
k_B	Boltzmann constant
MIM	Metal insulator metal
MIS	Metal insulator semiconductor
MOSFET	Metal oxide semiconductor field-effect transistor
Mw	Molecular weight
MWCNT	Multi-walled carbon nanotube

n	Frequency exponent
n_{+0}, n_{-0}	Initial volumetric concentration of cations, anions in ions/cm^3
n_{+MAX}, n_{-MAX}	Max. volumetric concentration of cations, anions
N_A	Avogadro's number
N_D	Donor atoms/cm^3
N_T	Number of charge traps per unit area
NP	Nanoparticle
P	Charge polarization
PEG	Poly(ethylene glycol)
PEO	Poly(ethylene oxide)
Q	Charge
q	Electronic charge magnitude (1.60219×10^{-19} C)
R_0	Resistance parameter of the frequency-dependent resistance
R_B	Bulk resistance
SEM	Scanning electron microscopy
SPE	Solid polymer electrolyte
SR	Slew rate
SS	Subthreshold swing
SWCNT	Single-walled carbon nanotube
T	Temperature
t_{bulk}	Thickness of the PEO bulk
TEM	Transmission Electron Microscopy
T_g	Glass transition temperature
t_{PEO}	PEO thickness
$t_{PEO,C-V}$	PEO thickness extracted from C–V data
t_{SiO2}	SiO_2 thickness
t_{Stern}	Thickness of the Stern layer
V	Voltage, electrostatic potential
V_{BG}	Back-gate voltage
V_D	Drain voltage
V_G	dc gate voltage applied to top electrode
V_{IN}	Voltage bias
VLSI	Very large scale integration
V_S	Source voltage
V_{th}	Thermal voltage at 300 K
Z	Impedance
$\|Z\|$	Impedance magnitude
$z_\pm$	Valence of cation, anion
ΔE_c	Conduction band offset
ΔV	Voltage difference
ε	Permittivity
ε_0	Permittivity of vacuum ($8.854187817\times10^{-14}$ F/cm)
ε_{PEO}	Dielectric constant of PEO
ε_r	Relative dielectric constant

θ_Z	Phase impedance
ρ	Resistivity
σ	Conductance
Φ_M	Metal work function
χ	Electron affinity
Ω	Resistance

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CHAPTER 1:

INTRODUCTION

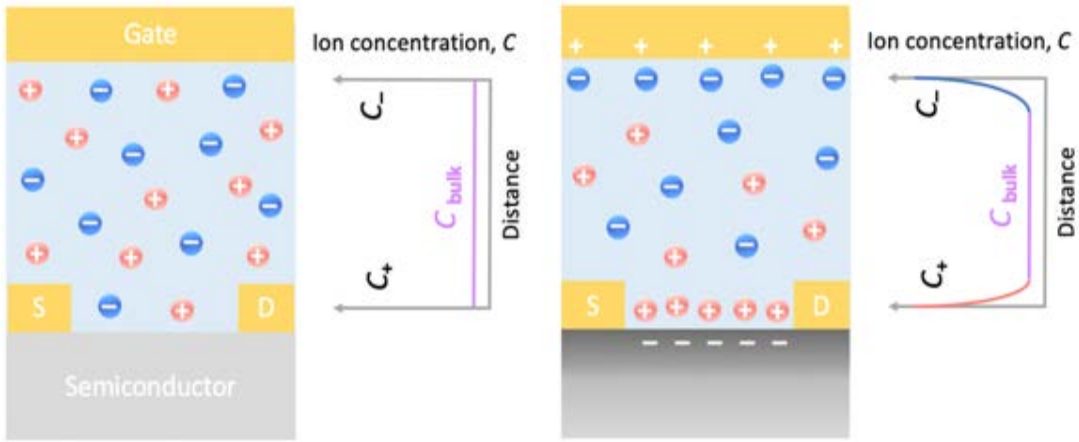
The aim of the proposed research is to utilize ions to add new functionality to semiconductor devices and electronics. Electrically-insulating, ion-conducting polymers such as poly(ethylene oxide) (PEO) with ion salts like lithium perchlorate ($LiClO_4$) or cesium perchlorate ($CsClO_4$) are systems which can be coated on semiconductors. The salts dissociate into cations (positive ions, such as Li^+ or Cs^+) and anions (negative ions, like ClO_4^-) intercalated between polymer chains and these ions move in response to internal and applied electric fields. Ions at a conductor or semiconductor surface create an electric double layer (EDL) as they induce a counter charge at the interface. On a semiconductor this can lead to accumulation or inversion layers and this has been used to configure and reconfigure the surface charge carrier profiles, for instance to convert metal-oxide-semiconductor field-effect transistors (MOSFETs) from *n*-FETs to *p*-FETs to tunnel FETs (TFETs) [1]. In a metal-polymer-metal or metal-polymer-semiconductor capacitor, the ions act to increase the capacitance of the structure and this could lead to new forms of digital and analog memory at the scaling limits of the ion conductor. Capacitor or transistor structures configured for nonvolatility could have application as weight storage devices to accelerate the training of deep learning systems as is being explored using ferroelectric oxides [2]. New device functions are also being investigated for neuromorphic computing applications based on coupling ions and electrons [3].

1.1 Prior art and applications of solid polymer electrolytes

In MOSFETs, a metallic gate is used to induce charge in a semiconducting channel. By applying a positive gate voltage on a *p*-type semiconductor, the semiconductor carrier type can be inverted as electrons are induced in the near surface layer. The inversion layer charge density, n_S, is related to the applied voltage and the oxide capacitance. With conventional insulators (SiO_2, HfO_2, Al_2O_3), sheet carrier densities of approximately $n_S \sim 10^{13}$ cm^{-2} can be induced. To induce more carriers and produce a higher on–current at the same gate voltage, the gate capacitance needs to be increased. Since the parallel plate capacitance is $C = \varepsilon_0 \varepsilon_r A / t_{OX}$, where ε_0 is the permittivity of vacuum, ε_r is the dielectric constant of the insulator, A is the gate electrode area, and t_{OX} is the insulator thickness, the capacitance is increased by thinning the dielectric or using higher κ dielectrics. This approach for increasing the MOSFET drive current has reached scaling limits but continues to be explored in new channel materials and dielectrics.

Consider the implications of using an ion-conducting solid polymer dielectric as the gate dielectric in a MOSFET, Fig. 1.1. In the absence of internal and applied electric fields, cations and anions are randomly distributed throughout the polymer, Fig. 1.1(a). When a positive gate voltage is applied between the gate and the semiconductor, anions (negatively charged ions) are attracted to the gate, while cations (positively charged ions) are driven toward the semiconductor, where they repel positive charge carriers (holes) and attract electrons, Fig. 1.1(b). Thus, two EDLs are formed: one at the metal/polymer interface and another at the polymer/semiconductor interface. In highly concentrated electrolytes, the separation between the accumulated ions in the polymer electrolyte and

the induced charge carriers at the solid surfaces are related to their atomic separations, which are at the scale of ~0.3 nm, leading to a capacitance density exceeding 10 μF/cm^2. Since the charge of each ion in the EDL is approximately matched by an induced charge in the conductor, the double layer screens the bulk of the electrolyte from the electric field, Fig. 1.1(b). This means that the voltage drops substantially across the two EDLs in approximately equal proportions in a symmetric structure. Remarkably, EDL sheet charge carrier densities have been reported in the range from 10^{14} – 10^{15} cm^{-2} [4] [5] [6] [7] and capacitance density even exceeding 100 μF/cm^2 has been reported [7]. While these high capacitance densities are intriguing, ions in transistor gates are generally undesirable due to the slow ion response (discussed in section 1.2.1) and the concern that ions can out-diffuse and accumulate in surrounding devices.



(a) (b)

Fig. 1.1: Schematic diagram of a metal / polymer electrolyte / semiconductor gate stack with source (S) and drain (D) contacts and the concentration of anions, C_-, and cations, C_+, across the polymer thickness. (a) In the absence of a built-in electric field in the system, the ions are randomly distributed with a homogeneous concentration across the polymer, C_{bulk}. (b) A positive gate voltage attracts anions and repels cations toward the semiconductor, where they attract electrons to the semiconductor surface. Note that under bias the voltage drops predominantly across the EDLs.

1.1.1 Polymer-based ion conductors

Polymer electrolytes are ion conductors that consist of a polymer matrix with dissolved salts that dissociate into mobile cations and anions. This distinguishes them from single-ion polymer electrolytes known as ionic polymers (which can be subdivided into so-called ionomers and polyelectrolytes, with the latter having a higher ion concentration that the former) in which only one ion polarity is free to move, while the other is chemically bound to the polymer chain [8]. In contrast, when both cations and anions are mobile, each of these can be used to induce carriers of the opposite charge polarity in the channel. Polymer electrolytes can be deposited into transparent, flexible, thin films that are solvent-free and easier to process [9] and integrate into a solid–state stack than liquid electrolytes[1].

In this dissertation, the focus is on solid polymer electrolytes (SPEs). These can form dry films with higher mechanical strength than gel polymer electrolytes, in which a liquid electrolyte impregnates the polymer matrix (leading to disadvantages such as the release of volatiles and higher reactivity with the metal contacts [9] [10]). SPEs have been amply used to make high energy density batteries, fuel cells, electrochromic devices, and sensors [11]. Prominent examples of SPEs include the polymer hosts poly(acrylic acid) (PAA), poly(ethylene imine) (PEI), and poly(ethylene oxide) (PEO, also called poly(ethylene glycol) (PEG) when its molecular weight is < 20,000 kDa), as well as the salts lithium perchlorate ($LiClO_4$), cesium perchlorate ($CsClO_4$) [12], and $KClO_4$ [13]. It should be noted that certain properties of SPEs (e.g. ionic conductivity,

[1] Known as ionic liquids, they consist of a salt dissolved in an organic or aqueous solvent.

thermal stability, mechanical strength, flexibility, etc.) can be improved by adding plasticizers, inorganic fillers, or nanomaterials, in which case they are labeled as composite polymer electrolytes [9] [10], Fig. 1.2.

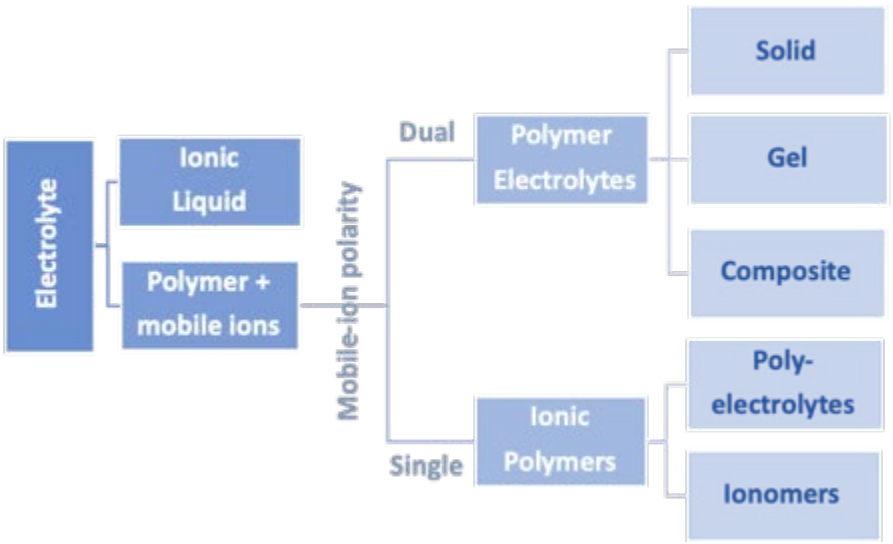


Fig. 1.2: Classification of electrolytes based on their physical state, mobile-ion polarity, and composition.

1.2 Selected applications of SPEs in metal-insulator-conductor devices

One of our original motivations for using SPEs was to reversibly induce strong doping densities in beyond–silicon materials, particularly two-dimensional (2D) crystals and carbon nanotubes (CNTs), which are difficult to dope substitutionally (replacing atoms of the crystal lattice by elements that donate or accept charge carriers). Using SPEs, sheet electron and hole densities above 10^{14} cm^{-2} have been induced in 2D crystals, surpassing the capability of substitutional doping in bulk semiconductors [1].

In transistor structures, a longitudinal electric field can be created by applying a bias between source and drain metal contacts contacting a semiconductor channel coated by

an ion containing polymer. Side electrodes/gates can be used to generate electric fields to position the ions along the channel. Once the ions are positioned the temperature can be lowered to lock (freeze) the ions in place to implement the desired channel conductivity and characterize the resulting transistor behavior. Semicrystalline polymers, such as PEO and polyvinyl alcohol (PVA), have a polymer matrix with amorphous and crystalline regions. In the former, the polymer chains are randomly oriented and constantly wiggling, thereby allowing ions to pass through, while in the latter regions, the polymer chains are aligned and folded into a tight structure that renders them immobile and blocks ions. Ion locking is enabled by cooling the SPE below its glass transition temperature, T_g, at which point its amorphous chains stop wiggling, thereby arresting ion motion throughout the polymer matrix [14, 15] and preserving the ion-induced carriers, as if the semiconductor was doped. The resulting device can then be characterized without hysteresis from ion motion. Warming above T_g restores the ion mobility. By applying suitable electric fields to control the density and polarity of the ions, the same channel can be reconfigured to form *n*-regions, *p*-regions, and *p-n* junctions.

PEO:$CsClO_4$ has been used to form and study *p-n* junctions in 2H-$MoTe_2$ [14], *p-i-n* junctions in WSe_2 [16], as well as *n*-type and *p*-type FETs in 2H-$MoTe_2$ [14], MoS_2 [5, 17] and WSe_2 [18]. Doping profiles for tunneling devices have also been produced, including tunnel diodes, such as WSe_2 Esaki tunnel junctions [19, 20], and TFETs. The doping profile of the single MoS_2 nanoribbon transistor has been shown to be reconfigurable to switch between *n*-FET, *p*-FET, and TFET [1].

Simulations of TFETs with various channel materials show that the best performance (i.e. highest on–current at 0.5 V gate-to-source voltage) is provided by CNT

channels [21]. This was one of our original motivators, to use SPEs to form tunnel junctions in CNTs to realize the CNT TFET. There are various reports in the literature of CNT FETs that have been doped and gated using SPEs. For instance, SPEs based on PVA were used to change the conduction type of an individual SWCNT channel from *p*– to *n*–type [22]. Polymer electrolyte gating of a single-walled CNT (SWCNT) channel using PEO:$LiClO_4$ was reported by Lu *et al.*, achieving subthreshold swings between 70–120 mV/decade [23], while Siddons *et al.* measured as low as 62 mV/decade [24]. Ozel *et al.* reported conduction type changes and electrolyte gating of SWCNT–network transistors also using PEO- and PEO-based electrolytes [25]. Our work using these ion-containing polymer dielectrics has shown that steep subthreshold swings can result when the delay due to the ionic response is commensurate with the sweep rate used in the characterization [26] [27]. In light of these findings, it is hard to know whether the early reports of low subthreshold swings are due to tunneling.

Work at Notre Dame by postdoctoral researcher Huamin Li used PEO:$CsClO_4$ to dope SWCNT FETs. This background is provided to set the context for the dissertation research. The drain current vs. back-gate voltage (I_D–V_{BG}) curves of 32 back-gated devices before PEO:$CsClO_4$ deposition are shown in Fig. 1.3. The CNT-on-quartz wafers [28] were provided by Greg Pitner from Prof. Philip Wong's group at Stanford University. FETs were fabricated by transferring the CNTs onto an Al_2O_3/HfO_2 dielectric formed by atomic layer deposition on a *p*-Si substrate. Transfer characteristics were then measured by back-gating, using the substrate as the gate electrode. Both metallic and semiconducting CNTs are present in the Stanford CNT growth process and this can be seen in Fig. 1.4. The transfer characteristics of the semiconducting channels show *p*-FET

characteristics, which are typically observed in CNTs. Most of the semiconducting CNTs show an I_D in the 10^{-8} – 10^{-7} A range at V_D = –0.5 V and V_{BG} = –0.5 V.

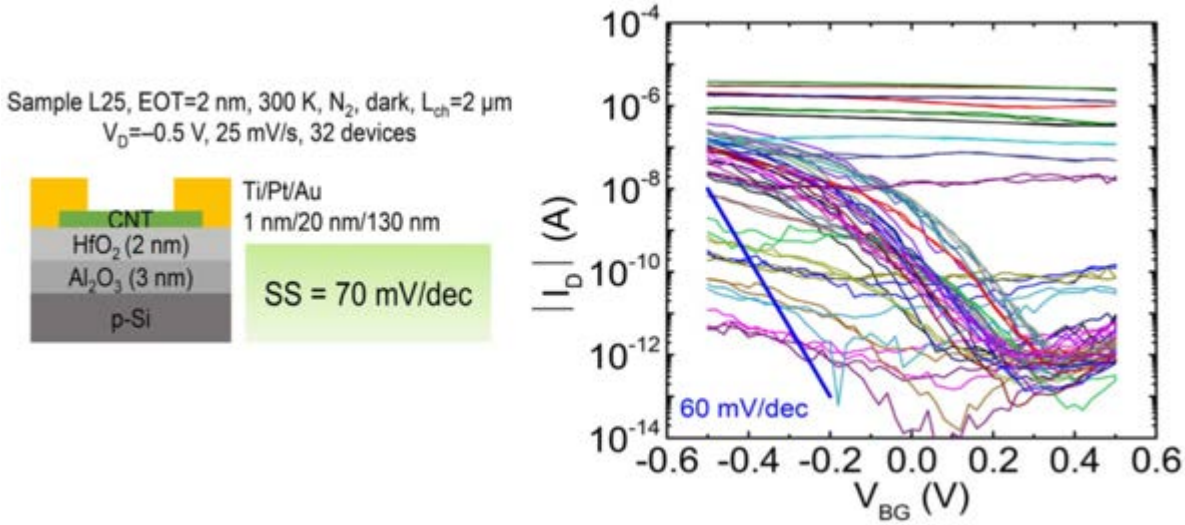


Fig. 1.3: Measurements of the transfer characteristics of 32 CNTFETs showing semiconducting and metallic CNT channels. Measurements and schematic diagram by Huamin Li, Notre Dame.

After PEO:$LiClO_4$ deposition, Huamin Li used a doping procedure to position and freeze ions in the PEO for measurements below the glass transition temperature. These measurements are displayed in Fig. 1.5. Side–gates were biased at either –2 V or +2 V at 40 °C for 1 hour to form an EDL that induces holes (or electrons) in the CNT to produce a *p*-type (*n*-type) CNT FET. While holding the side gate and terminal biases, the CNT was cooled down below the polymer's glass transition temperature. The resulting *p*–type CNT FET showed similar currents after ion doping and the subthreshold swing (SS) increased from ~70 to 100 mV/decade. The *n*-type CNT FET reached similar on-currents to the *p*-FET but could not be turned off within the same range of back-gate voltages under study. This dependence has been seen using other channel materials such as MoS_2

[1] and could indicate that the Cs^+ becomes intercalated between the CNT and the back-gate oxide, where they screen the back-gate field.

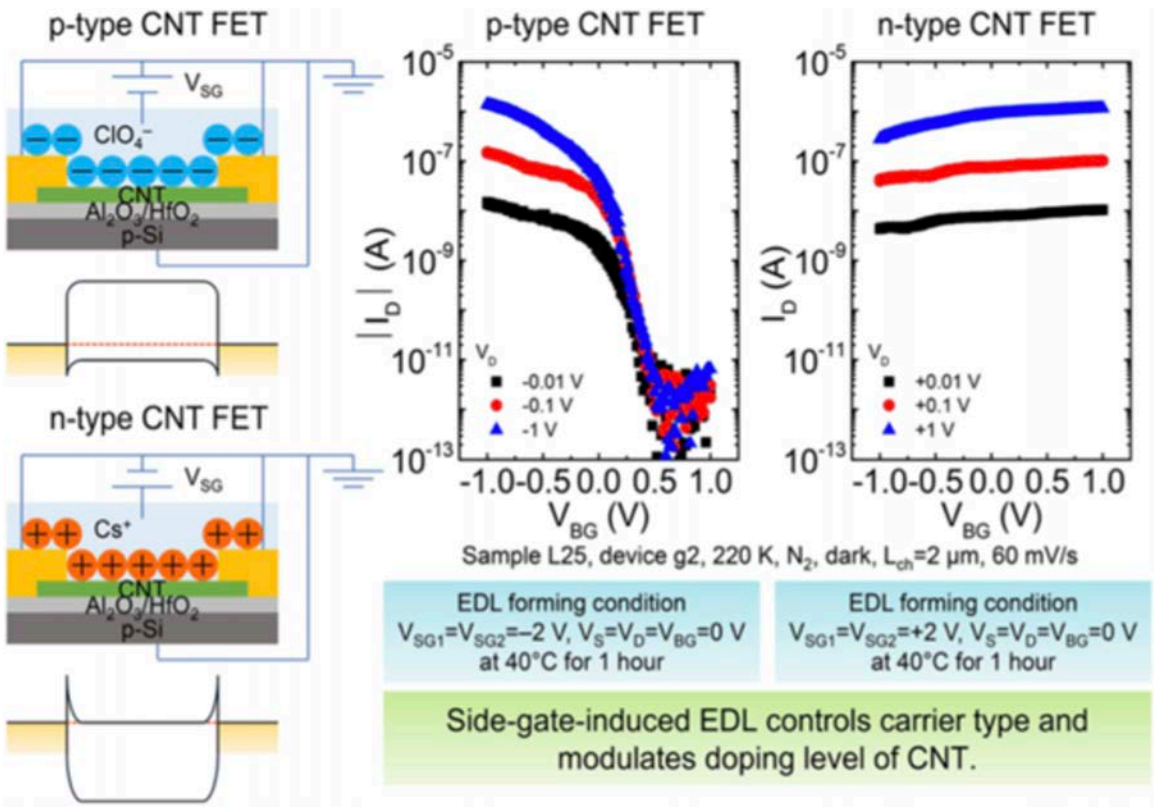


Fig. 1.4: Measurements of back-gated CNT FET after depositing PEO:$CsClO_4$ (~ 1 μm thick), after side-gating and freezing the ions into position by cooling below the glass transition temperature. The channel conduction type is initialized by setting $V_S=V_D=V_{BG}=0$, and a side-gate voltage V_{SG} on two co–planar side gates as indicated The transfer characteristics, I_D–V_{BG}, were measured after cooling to 220 K. Measurements and schematic diagrams by Huamin Li, Notre Dame.

The same PEO:$CsClO_4$ was used to form a *p–i–n* junction on a CNT FET, Fig. 1.5. The source and drain contacts were biased at $V_S = -V_D = 1$ V for 1 hour, followed by cooling to 220 K. At this temperature, the transport characteristics show a current rectifying ratio of ~10^3. The transfer characteristics of the back-gated device show a subthreshold swing of 50 mV/decade at 220 K (extrapolated to 68 mV/decade at 300 K).

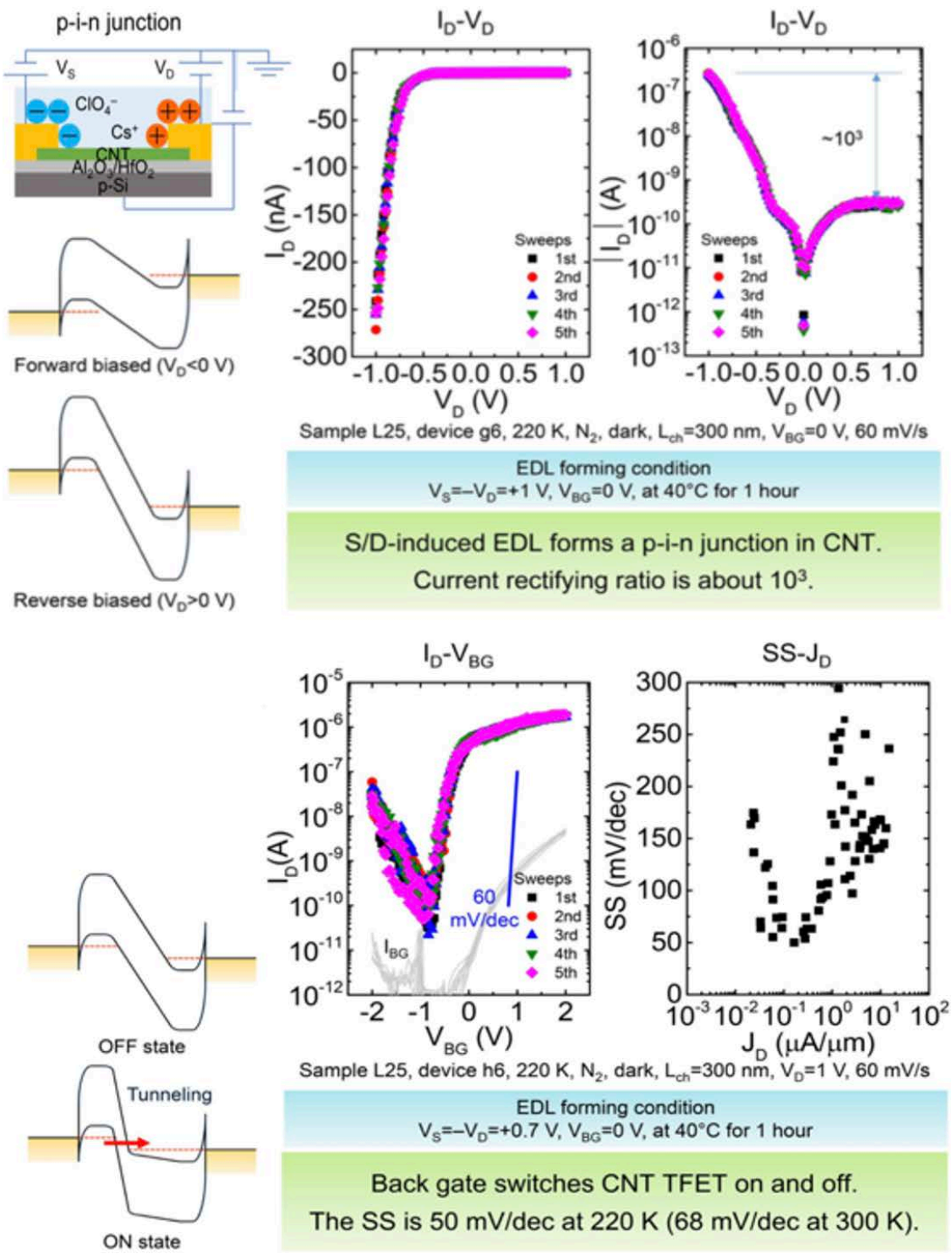


Fig. 1.5: Experiments to form a *p–i–n* junctions on a CNT FET using PEO:$CsClO_4$. The junction is formed by EDLs of opposite polarity induced at the S/D FET contacts. Current-voltage ($I-V$) characteristics were made after freezing the ions in place at 200 K. Measurements and schematics by Huamin Li, Notre Dame.

While the use of ions to modulate the conductivity (doping) of CNT channels is demonstrated, the performance of *n*, *p* and TFETs has not yielded sufficient degeneracy and doping abruptness to yield interband tunnel junctions. This calls for experimental work to characterize the energy band relationships of PEO:$CsClO_4$ in metal insulator semiconductor (MIS) and metal insulator metal (MIM) structures at PEO thicknesses relevant for devices.

An ideal or "universal" memory is of wide technical interest, combining high speed (100 ps), endurance (10^{16} cycles) and low energy (0.5 fJ/bit), as in static random access memory (SRAM) with high density (1 Tbit/cm^2) and nonvolatility as achieved in flash memory [29]. Unfortunately, ions of the type considered have no apparent application in universal memory. However, there may be ways to use SPEs for analog and neuromorphic device applications; for example, $Ba(CF_3SO_3)_2$-doped PEO capacitors have been used to simulate synaptic plasticity [30].

Seabaugh and Fullerton patented a memory structure that introduces nonvolatility into a solid-polymer-based memory [31]. In this structure, an ion conducting dielectric (e.g. an SPE or a solid monolayer electrolyte made of crown ethers (CE) complexed with Li^+ ions) is sandwiched between a conductor and a semiconductor to modulate the conductance of a FET channel. The physical operation of this configuration was explored from first-principles calculations in [32]. The channel conductance is used to read the state of the memory.

Another type of emerging memory combines CMOS and memristors (memory resistors) in a passive crossbar architecture [29]. Memristors are 2-terminal devices whose resistance changes in response to voltage pulsing, which can be varied in

amplitude, polarity, and duration. The programmable current-voltage relation cannot be replicated by combinations of resistors, capacitors, and inductors [29]. Memristors have been implemented with SPEs, for instance using PEG and its inherent mobile cation, hydrogen ions, in a crossbar architecture as part of the gate stack of a CNT–network FET [33]. In this case they function as an artificial synapse. A positive gate bias drives hydrogen cations toward the CNT-network interface, where they attract electrons in the CNTs. An electrochemical reaction between the hydrogen ions and the CNTs modifies the CNT bandgap between 0 and 3.2 eV, which changes the channel current in a way that simulates the current through a post-synaptic neuron. An SPE such as PEO:$CsClO_4$ could be utilized in a similar way, although its dynamics would be affected by also having Cs^+ cations, which could induce even more electrons in the channel than H^+ alone, though without the electrochemical reaction, as well as also having counter ions (ClO_4^-), which would add the functionality of attracting holes in the CNTs when using a negative gate bias.

1.2.1 Ion response time

A crucial speed limitation of EDL devices stems from the fact that their performance is governed by ion mobility. The mobility of ions in PEO is low[2], ~3×10^{-7} cm^2/Vs. This means that the transit time for an ion to traverse 1 nm of PEO at an electric field of 1 V/nm (10 MV/cm) is 33 ns. This is faster than flash memory, which has a write speed of 10 μs – 1 ms, and slower than dynamic RAM, with read and write speeds of

2 From the measured conductivity of PEO:$LiClO_4$, 10^{-5} S/cm [34] for a salt concentration of $2\times10^{20}/cm^3$.

~10 ns [35] [36]. Lower the electric field by a factor of a 1000 and increase the PEO thickness by a factor of 1000 and you get the response speeds often observed in measurements: ~1–100 s for the EDL to fully form (with a charge density of ~10^{13} cm^{-2}) in ~1 μm thick PEO:$LiClO_4$ on a graphene FET using an electric field of ~2 mV/nm [37].

A report by K. Xu and coworkers [38] showed experimentally that a 7 ms pulse with an electric field of 6.7 mV/nm can produce an EDL with an estimated charge density in the order of 10^{14} cm^{-2}, in 15 μm thick PEO:$CsClO_4$ on a graphene FET. Still, millisecond speeds are generally too slow for electronic applications. According to molecular dynamics simulations of graphene/PEO/graphene capacitors with 15-nm-thick PEO:$LiClO_4$, the EDL formation could be achieved in nanoseconds using electric fields of 50 mV/nm in a scaled device [38] placing this in a range of interest for electronics. However, this remains to be demonstrated experimentally. There is some question about whether the diffusivities used in this work were too optimistic (~10^{-8} cm^2/s) compared to other published work for $LiClO_4$ (10^{-12} cm^2/s [39]) and $CsClO_4$ (10^{-11} cm^2/s, consistent with measurements in this thesis).

1.3 Increasing the EDL charging speed

1.3.1 SPE thinning can increase ion mobility

Thinning a semicrystalline SPE film can in principle alter its ionic conductivity by changing the ion mobility. The physical behavior of polymers confined in one or more dimensions can cause the polymer properties to diverge from the bulk properties. This may include a change in conductivity, glass transition temperature, kinetics and degree of crystallization, morphology, moisture absorption, dewetting, and/or permeability [40]. It

has been reported that thinning down a PEO film below ~200 nm reduces its degree of crystallinity [41]. This means a greater percentage of the film is composed of amorphous regions, which are the ones through which ions can move, leading to enhanced ion mobility and faster ion response than in bulk PEO.

1.3.2 Electrical factors

In addition to the ion mobility, the initial charging speed of the EDL also depends on the applied electric field. Thinning the SPE allows the use of lower voltages to produce the same electric field, or higher fields at the same voltage to make ions drift faster. However, the electric field should not be large enough to produce a displacement current that heats the electrodes or interconnects. In addition, the field should be low enough to avoid driving any electrochemistry that modifies the electrodes and/or the electrolyte (under ~ 1 V/nm). Nonreversible electrochemistry could cause fatigue and degrade repeatability of the electrical response.

If there is a work function difference between the capacitor's electrodes, the built-in electric field will cause EDLs to form even in the absence of an applied bias. Thus, it is likely that in any device structure there will be surface electric fields and contact-induced potential differences which will result in ion accumulation and depletion. This can be expected to induce asymmetry in the pulse response.

Once the EDLs form, the speed of their response can be described with an *RC* circuit. Measurements and modeling of transistors and capacitors utilizing PEO and PEO:$CsClO_4$ are described in [26]. That work establishes a simple *RC* model, in agreement with measurements, which gives insights on the thickness targets for future

development of PEO devices. It shows that the dynamics of metal PEO metal capacitors can be represented by a series *RC* circuit where the *R* is the bulk resistance, controlled by ion conductivity, and a capacitance *C* representing the lumped capacitances of the two EDLs.

As the dielectric is thinned, it is possible to geometrically reduce the *R* to zero. At this dimension, the PEO capacitor consists of two coupled EDL capacitors each with their own controlling shunt resistances. It was a hypothesis of this investigation that at some scale the ion transport may exhibit an enhanced nonvolatility, as predicted for single monolayer of crown ethers (CE) complexed with Li^+ ions. In crown-ether structures, first principles calculations [32] indicated that Li^+ ions tend to be located either above or below the CE plane, resulting in two configurations of the CE–Li^+ complex. Transport through the CE's cavity requires surmounting an energy barrier, producing a double-well energy landscape. The barrier is lowered by applying an electric field perpendicular to the CE, thereby permitting ion transport. The increased electrostatic force of the ion-carrier EDL lowers the energy of the pair and makes release a higher energy process than formation thereby increasing the retention. The CE–Li^+ complex has been experimentally studied on highly ordered pyrolytic graphite (HOPG) [42] and graphene [43], but not in simple capacitor geometries which are needed to draw strong conclusions about the controlling physics.

1.3.3 Physical factors controlling the SPE thickness

Nanometric film thicknesses are achievable in PEO by changing the SPE deposition method. Rather than depositing a droplet of the polymeric solution on the substrate and simply letting it dry, which is known as dropcasting (resulting in ~1 μm thick films), the substrate is spun at thousands of revolutions per minute (rpm) to obtain films hundreds or even tens of nanometers thick. A summary of reported ultrathin (< 100 nm) PEO films is shown in Table 1.1, along with the spinning parameters used. These include the polymer's molecular weight and concentration in the chosen solvent, the substrate surface and any pretreatments applied to it, the spin protocol used, and the subsequent temperature treatment or anneal. These reports suggest that with the right spinning parameters, the PEO:$CsClO_4$ films could be tens of nm thick or even less, although it is expected that the addition of salts to the polymer solution will affect the film thickness.

TABLE 1.1

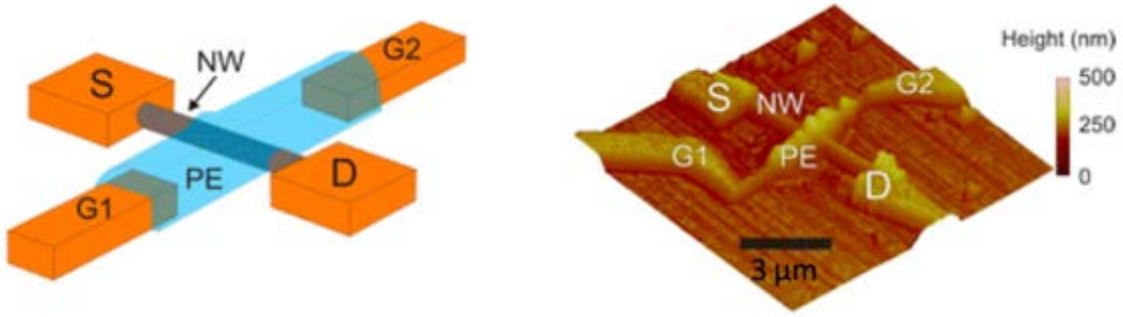
COMPARISON OF THIN AND ULTRATHIN PEG AND PEO FILM FORMATION METHODS

Mw ($\frac{\mathbf{kg}}{\mathbf{mol}}$, kDa)	**Solvent**	**[PEO]** (% wt)	**Substrate (pre-treatment)**	**Spin speed, time**	**Anneal *T*** (ºC)	t_{PEO} (nm)	**Ref.**
• 2 • 7.6	Toluene	/	Si (UV[a]–ozone)	/	• 30 • 44	50–100	[44]
• 4 • 6	ACE[a]	0.4	Si (UV[a] 145 min)	4,000 rpm 30 s	49	~7.5	[45]
100	CF[a]	0.1–5.0	Oxidized Si (Ar–plasma)	3,300 rpm, 60 s	47 –61	10–15	[41]
272	ACE[a]	0.65–3.00	• Si • 110 nm Au / Si	/	48	40–1,000	[46]
600	Water	0.1	Si	• 1,000 rpm, 60 s • 3,000 rpm, 60 s • 5,000 rpm, 60 s	/	• 3.8 • 2.1 • 1.4	[47]

[a] Abbreviations: Acetonitrile (I), Chloroform (CF), deionized water (DI), Dichloromethane (DCM), Tetrahydrofuran (THF), ultraviolet (UV)

1.4 Patterning and ion containment

PEO can be used as a negative photoresist and patterned using electron beam lithography (EBL) (both without ions [33] and with $LiClO_4$ ions [48], Fig. 1.6) and can also be compatible with optical lithography [49]. While EBL patterning of PEO:$LiClO_4$ did result in electron–induced polymer cross–linking, which reduces the ion mobility and can neutralize ions, the lower ion mobility still produced functional nanowire transistors [48].



(a) (b)

Fig. 1.6**:** Patterned SPEs: (a) schematic and (b) atomic force microscopy (AFM) graph of PEO:$LiClO_4$ that was patterned by electron-beam lithography over a nanowire transistor with source, drain, and side gates (G1, G2). Figures from Carrad [48].

The patterned SPE can be encapsulated to permit performing subsequent lithography steps on the wafer, as well as to enhance the EDL device's repeatability and reduce device-to-device variability due to differences in ion loss. The present work explores using a nanometer scale oxide layer for ion encapsulation based on SiO_2, although other materials (e.g. Al_2O_3) may be selected in future work for optimized containment and device performance.

This work addresses the important topic of adding functionality to nanoelectronic devices by using an organic, nanoscale polymer film with mobile ions over nanostructures such as individual, semiconducting CNTs. The exploration of interfaces of polymer/solid state systems at the decananometer scale is basic to their use in electronics and paves the way for practical incorporation of ion-electron functionality into devices. The intent of this investigation has been to develop a quantitative and experimentally validated understanding of ionic transport to gauge the utility of ions in deep learning training, neuromorphic devices, and reconfigurable switching.

1.5 Outline

This thesis details simulations, as well as physical and electrical characterization and analysis of PEO and PEO:$CsClO_4$ thin films in capacitor structures. Chapter 2 presents Multiphysics simulations of the ion dynamics in capacitors with nanometric PEO:$CsClO_4$ films after applying a constant voltage bias. The electric field across the PEO film and the resulting ionic distribution are observed after constant-voltage turn-on, as well as the net ionic charge and capacitance at the electrode interfaces during EDL charging, which is seen to occur within the microsecond timescale. The simulated current density through the capacitor is shown to have the initial peak and subsequent decay observed in experiments. The effects of thinning the PEO film is shown in the time evolution of the current and EDL capacitance.

In Chapter 3, record-thin films of PEO:$CsClO_4$ are demonstrated on Si and CNTs-on-quartz. We show that PEO:$CsClO_4$ can be spin coated at thicknesses compatible with VLSI (very large scale integration) electronics, as thin as 8 nm. Transmission electron

microscopy (TEM) and electron energy loss spectroscopy (EELS) images show that the film surrounds nanostructures such as CNTs without interlayers, as desired for EDL formation, which is a functionality that can be exploited for memory and neuromorphic devices. Cesium is imaged for the first time in the PEO film, where it is confined by an SiO_2 encapsulating layer deposited by e-beam evaporation, thereby enabling subsequent lithography steps. This suggests it is possible to develop an appropriate PEO:$CsClO_4$ deposition process to achieve stronger ion doping of CNTs.

Chapter 4 presents the electrical characterization of pure-PEO thin films of various thicknesses in metal polymer semiconductor capacitors. These are characterized in terms of resulting thickness and electrical behavior, including impedance vs. frequency and capacitance, conductance vs. voltage measurements.

In Chapter 5, the COMSOL Multiphysics model is used to study the ion dynamics in response to various applied voltage steps and triangular waveforms. This is compared to the current density and polarization charge density measured in fabricated metal polymer metal capacitors. The later are shown to have an impedance vs. frequency behavior similar to that of metal polymer semiconductor capacitors in Chapter 4. The work is summarized and wrapped up in Chapter 6.

CHAPTER 2:

STATIC AND DYNAMIC SIMULATIONS OF ION TRANSPORT IN CAPACITORS WITH AN ULTRATHIN POLYMER DIELECTRIC

2.1 Overview

This chapter presents static and dynamic simulations of a 1–D PEO:$CsClO_4$ capacitor implemented in COMSOL Multiphysics [50]. In these simulations, the electrodiffusion of ions in the PEO film is solved using the Poisson-Nernst-Planck equations, modified to account for the finite ion size, using finite element analysis, to simulate the transient and steady-state ionic response to an applied bias. These simulations are used to observe the time evolution of the ionic transport in PEO over the course of nanoseconds to a milliseconds. This is then used to guide interpretation of measurements of fabricated PEO:$CsClO_4$ capacitors presented in the following chapters.

2.2 Physical principles and model implementation

An ultrathin PEO:$CsClO_4$ capacitor was simulated in COMSOL Multiphysics using the coefficient form partial differential equation solver and the AC/DC module, more specifically its electrostatics and electrical-circuit interfaces. The ionic transport in the PEO film was modeled using the Nernst-Planck equations as modified by Kilic, Bazant, and Ajdari [51] to account for the finite ion size, which limits the maximum amount of ions that can be accumulated at the interface:

$$\frac{\partial c_{\pm}}{\partial t} = D\nabla^2 c_{\pm} + \frac{D}{V_{th}} z_{\pm} \nabla \cdot (c_{\pm} \nabla V) + D\nabla \cdot \left(\frac{c_{\pm} \nabla (c_{+} + c_{-})}{c_{MAX} - c_{+} - c_{-}} \right), \qquad (2.1)$$

where c is the molar ion concentration, the + and – subscripts indicate cations and anions, respectively, D is the ionic diffusion coefficient, ∇ is the gradient, $\nabla = \partial/\partial x$, x is the position along the film thickness, $V_{th} = k_B T/q$ is the thermal voltage, k_B is Boltzmann's constant, T is temperature in K, q is the fundamental electron charge, z is the ion valence (+1 for Cs^+, –1 for ClO_4^-), V is the electric potential, c_{MAX} is the maximum molar ion concentration equal to $1/N_A a^3$ [51], N_A is Avogadro's number, and a is the effective ion size, including any solvation shell around the ion. The behavior captured by these theoretical equations will be compared with experimental results in later chapters, in order to see if they reflect the main features of the measurements of fabricated PEO and PEO:$CsClO_4$ capacitors.

The third term in Eq. (2.1) captures the effects of the finite ion size on the EDL charging dynamics. These so-called steric effects become pronounced in surfaces with high charge density, such as at an electrode with a large applied bias, i.e $V >> V_{th}$. In such densely packed surfaces, the finite ion size must be taken into account, as it limits the ion concentration to a maximum of c_{MAX}. The effective cation diameter, a = 0.4 nm, used here, sits between the value for completely-hydrated Cs^+, 438 pm [52] and the diameter of non-hydrated Cs^+, 362 pm [53]. The Cs^+ cation could be partially hydrated by water absorbed into the PEO. The diffusion coefficient of Cs^+ was taken to be 10^{-11} cm^2/s, higher than that of Li^+, 10^{-12} cm^2/s [39], since larger cations like Cs^+ have higher ionic conductivity[3] [54] and thus, higher diffusivity than Li^+. Simulations were run

[3] Larger cations have lower charge density, which weakens the interactions with the sections of the polymer with negative charge. This results in a looser polymer matrix that is more flexible and has more empty spaces through which cations can travel [54].

for ionic diffusivities from 10^{-13} cm^2/s to 10^{-10} cm^2/s and the diffusion coefficient chosen for subsequent simulations was 10^{-11} cm^2/s, as that simulation best matched the measured current response to a triangular voltage pulse, as described in Chapter 5. To observe first-order effects, a and D were assumed to be the same for cations and anions.

Given the symmetries in the capacitor system, the COMSOL model had a 1–D geometry across the PEO:$CsClO_4$ film, as shown in Fig. 2.1, with thickness of 10 nm and a maximum mesh element size of 0.01 nm. Given this 1–D geometry, the simulation does not model fringing fields. However, COMSOL's electrostatics interface does consider a certain capacitor cross-sectional area A. This was taken to be the area a 20-μm disc, which is one of the sizes of the fabricated capacitors studied in later chapters. The resulting simulated current was divided by this area to obtain the current density, J.

The PEO film is modeled using a bulk static permittivity of PEO, $\varepsilon_0\varepsilon_{PEO}$, where $\varepsilon_{PEO} = 1.5$, in accordance with findings shown in later chapters. Since real ions are not point charges but have finite size, there is a limit to how close they can come to the PEO/electrode interface. To capture this, so-called Stern layers were defined at the interfaces, as shown in Fig. 2.1, with the thickness of the ionic radius, $a/2$. To simulate the case of blocking electrodes for both ions and electrons, charge transport was not permitted through the Stern layers, which also had the permittivity of vacuum. The only current transport mechanism across the EDL is by electric displacement current. As the ionic charge density changes on one side of the interface, this causes image charge density changes on the electrode, giving rise to current. Fig. 2.1 also shows that ions can still accumulate deeper into the film beyond the Stern layer, in what's known as the

diffuse layer, with a decaying charge concentration until eventually, the charge-neutral bulk of the electrolyte is reached.

With zero applied bias in this symmetric system with no built-in electric field, the ions are evenly distributed across the film, having a molar concentration of c_0 = 361.8 moles/m^3 ($n_0 = 2.2 \times 10^{20}$ ions/cm^3) for both cations and anions (with initial concentrations, $c_{+0} = c_{-0} = c_0$; $n_{+0} = n_{-0} = n_0$). This is the same value used in the fabricated PEO:$CsClO_4$ capacitors studied in later chapters.

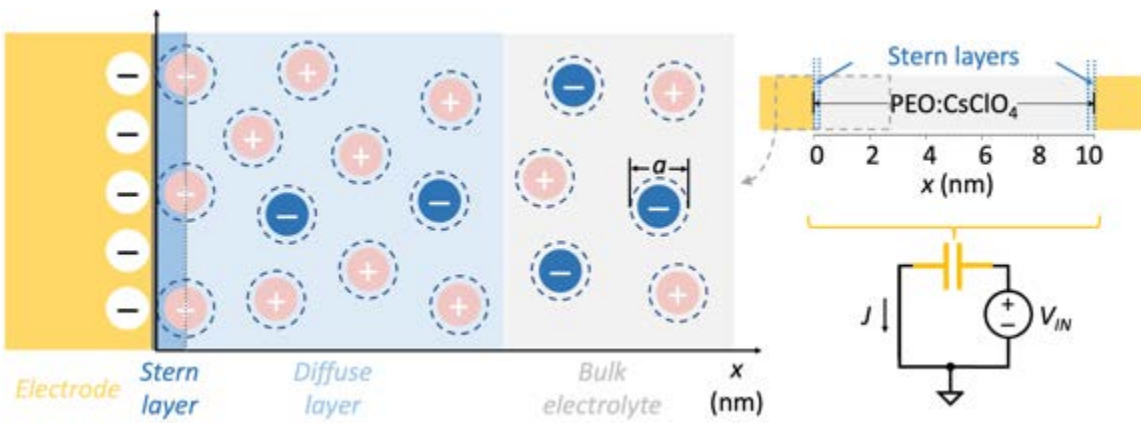


Fig. 2.1 Schematic diagram of the model of a biased capacitor with a 10-nm thick PEO film with dissolved mobile cations (pink) and anions (blue). The zoom-in into the electric double layer at one electrode shows the Stern and diffuse layers in dark and light blue, respectively, and metal electrons in white. The Stern layer has the thickness of the effective ionic radius, $t_{Stern} = a/2$ = 0.2 nm.

The electric potential in the system is governed by Poisson's equation with ρ representing the volumetric charge density,

$$-\nabla \cdot (\varepsilon \nabla V) = \rho = q(c_+ - c_-) \,. \tag{2.2}$$

The electrodes were assumed to be perfect conductors, so that the potential is applied exactly from one electrode surface to the other. As shown in Fig. 2.1, the left electrode was grounded, while a constant positive voltage, V_{IN}, was applied to the right electrode.

The stationary study applied a constant voltage (V_{IN} in the range from 0 to 1 V with a voltage step of 0.2 V) to give the final ion concentrations, electric field magnitude, and electrostatic potential distributions for a given bias. Transient studies applied a step voltage from zero to V_{IN} = 1 V at t = 0 and sampled time linearly in 300 ns intervals up to 1 ms, to observe the dynamic ionic response. Current was only obtained in transient studies, since in the stationary system, there is not electric displacement current and J = 0. The current density could be calculated directly as the displacement current across the Stern layer, divided by the capacitor cross-section. The list of simulation parameters is shown in Table 2.1.

TABLE 2.1

COMSOL MULTIPHYSICS MODEL PARAMETERS

Parameter	**Symbol**	**Value**
Area of electrode	A	3.14×10^{-6} cm^2
Avogadro's number	N_A	6.02×10^{23} /mol
Boltzmann constant	k_B	8.62×10^{-5} eV/K
Dielectric constant of PEO	ε_{PEO}	1.5
Diffusivity of cations, anions	D_+, D_-	10^{-11} cm^2/s
Effective ion size	a	0.4 nm
Elemental charge	q	1.60×10^{-19} C
Initial molar concentration of cations, anions	c_{+0}, c_{-0}	361.8 mol/m^3
Initial volumetric concentration of cations, anions	n_{+0}, n_{-0}	2.18×10^{20} 1/cm^3
Max. molar concentration of cations, anions	c_{+MAX}, c_{-MAX}	$\frac{1}{N_A a^3}$ =25,946 mol/m^3
Max. volumetric concentration of cations, anions	n_{+MAX}, n_{-MAX}	1.56×10^{22} 1/cm^3
Permittivity of vacuum, Stern layer	ε_0	8.85×10^{-14} F/cm
Temperature	T	300 K
Thermal voltage at 300 K	V_{th}	25.9 mV
Thickness of PEO:$CsClO_4$ film	t_{PEO}	5, 10, 15, 20 nm
Thickness of Stern layer	t_{Stern}	$a/2$ = 0.2 nm
Valence of cation, anion	$z_\pm$	±1
Voltage bias	V_{IN}	1 V

2.3 Static simulations of metal / PEO:$CsClO_4$ / metal capacitors

The ionic concentration profiles across the thickness of the PEO film in the steady state for a 1 V bias are shown in Fig. 2.2. The cation, n_+, anion, n_-, and net, $n_{NET} = n_+ - n_-$, ion concentration profiles are shown in red, blue, and green lines, respectively. The gray line marks the initial ion concentration n_0, before the bias is applied. After turning on the bias, the electric field across the film causes ions to drift to the electrode interfaces, thereby reducing the ion concentration in the bulk, as the inset of Fig. 2.2 shows. For a given voltage polarity at an electrode (e.g. negative), ions of opposite polarity (cations) are attracted and accumulate at the interface, while ions of the same polarity (anions) are

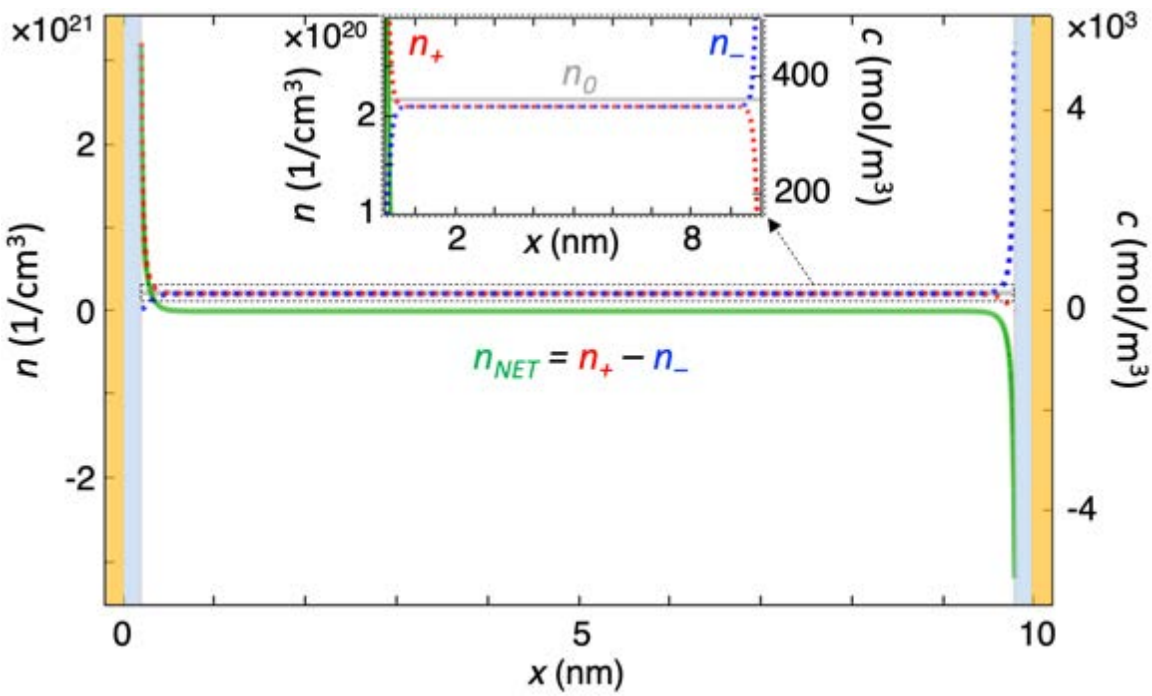


Fig. 2.2 Simulated ionic concentration profile in the steady state for an applied bias of 1V. The left and right y-axes indicate the volumetric and molar concentration, respectively, of cations (dotted red line), anions (dotted blue line), as well as the initial (solid gray line) and the net (solid green line) ion concentration. The location of the Stern layers and the electrodes are indicated by blue and yellow boxes, respectively. The inset is a zoom-in into the boxed region.

repelled and their concentration drops in the electrode vicinity. The resulting cation and anion concentration profiles are mirror images of each other with respect to a vertical line at the PEO midpoint (x = 5 nm). Thus, going forward only the cation profiles will be shown for clarity, knowing that the anion profile is axially symmetric with respect to the PEO midpoint.

Shown in Fig. 2.3 are the (a) electric field magnitudes and (b) cation concentration profiles vs. position in the steady state after applying a constant voltage between 0 – 1 V. Since in the steady state, the ionic charge at the EDLs fully compensates the charge at the electrodes, the applied voltage drops across the EDLs, while the bulk remains at an equipotential. With increasing bias, the electrode surface becomes more densely packed with ions of opposite polarity and the EDL extends deeper into the PEO film, as the left inset of Fig. 2.3(b) shows. Meanwhile, in the vicinity of the electrode of the same polarity, the ions are further repelled with increasing bias, as the right inset shows, increasing the width of the ionic species' depletion region.

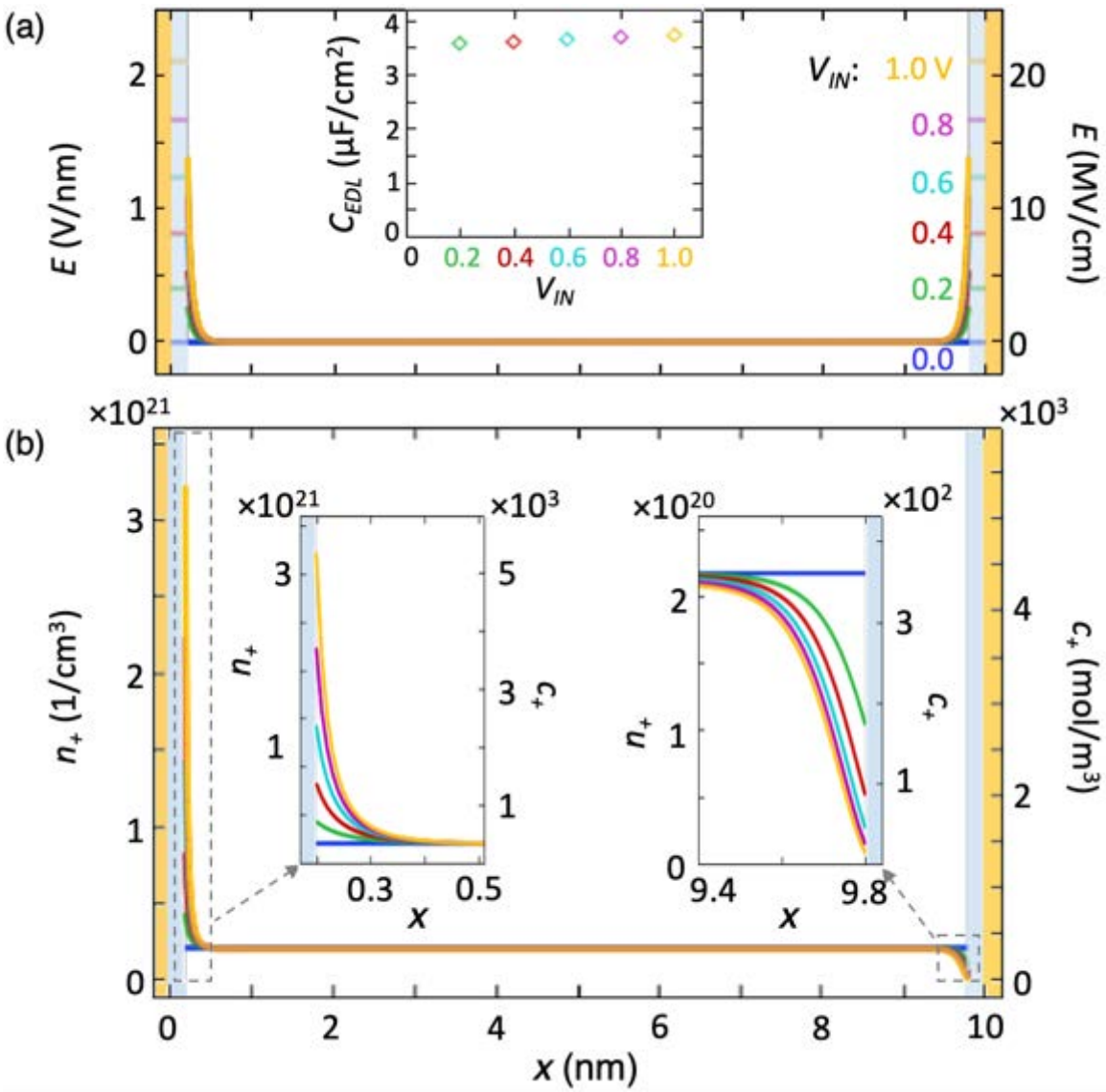


Fig. 2.3 Steady-state (a) electric field and (b) cation concentration profile across the film as a function of biases ranging from 0 to 1 V. The Stern layers and electrode contacts are indicated in light blue and yellow, respectively. The left and right y-axes in (a) indicate the electric field in V/nm and MV/cm, respectively. The inset in (a) is the EDL capacitance density vs. applied bias. The left and right y-axes in (b) show the volumetric and molar ionic concentration, respectively. The insets in (b) are zoom-ins into the ionic concentration at the electrode vicinities.

The inset in Fig. 2.3(a) shows the steady-state EDL capacitance for various applied voltages, calculated as $C_{EDL} = Q_{EDL}/0.5V_{IN}$, where Q_{EDL} is the integral of the net ion concentration, $n_{NET} = n_{+} - n_{-}$, from the electrode to the PEO midpoint, in order to account for all the net charge corresponding to that EDL, even if far from the electrode interface. For reference, the expected capacitance density for a geometrical capacitor with a relative dielectric constant ε_{PEO} =1.5 and a plate spacing of 0.4 nm (a/2 = 0.2 nm Stern layer with ε_{Stern} =1, plus 0.2 nm Diffuse layer = 0.4 nm with ε_{PEO} = 1.5; this is the depth at which the cation concentration is approximately equal to the bulk concentration, as the inset of Fig. 2.3(a) shows) is 3.3 μF/cm^2 for a 20 μm diameter area, which is consistent with the simulation. The inset shows that with greater applied bias, there is a slight increase in the final EDL capacitance, which is consistent with the higher electric field extending deeper into the PEO film and resulting in greater ionic accumulation, as seen in the left inset of Fig. 2.3(b).

2.4 Simulated transient response of metal / PEO:$CsClO_4$ / metal capacitors

The time evolution of the cation concentration profile and the electric field along the PEO thickness is shown in solid lines in Fig. 2.4(a) and (b), respectively. The net ion concentration at one electrode is marked in circles in the left inset of (a). Given that as time evolves, there is an order magnitude difference in concentration of cations and anions at this electrode interface, the net ion concentration, $n_{NET} = n_{+} - n_{-}$, almost equals the concentration of the accumulated ion. As explained in the prior section, the cation profile is a mirror image of the anion profile, as Fig. 2.2 shows, since both types of ions are taken to have the same properties other than their opposite polarity.

Again, once the electric field is applied, the cations drift toward the negative electrode, where they accumulate over time. The ion concentration saturates as time progresses, as the zoom-in in the left inset of Fig. 2.4(a) shows. The depletion of cations at the positive electrode also slows down over time.

Additionally, Fig. 2.4(b) shows that as the EDLs charge up over time, more of the applied bias drops across the EDLs, while the electric field in the bulk decreases. By 150 μs it has dropped by an order of magnitude. This decreasing rate in EDL charging happens because the ion accumulation (depletion) also increases (decreases) the concentration gradient, which opposes any further accumulation (depletion). However, if the applied bias and thus, electric field in the bulk was increased, cations would continue to drift toward the negative electrode and away from the positive electrode, until a new balance with the concentration gradient is reached. That would allow n_+ at the interface to get closer to the maximum n_{MAX} set by the steric limit and, for even higher bias, it would thicken the EDLs as seen in Fig. 2.3(a).

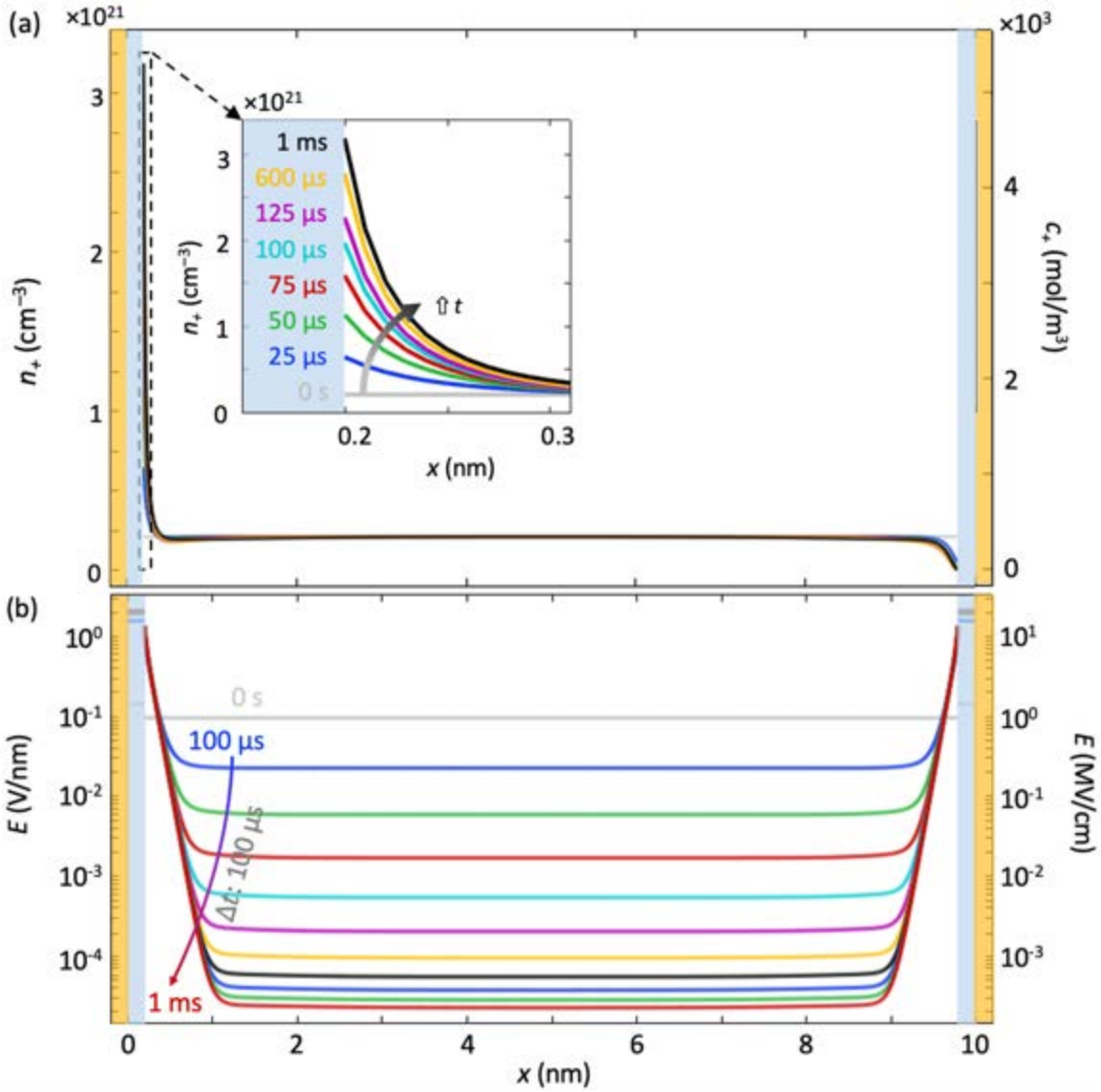


Fig. 2.4 Multiphysics simulation. (a) Ion concentration and (b) electric field vs. position along the depth of the PEO film at various times after applying a 1 V bias. The left and right y-axes in (a) indicate the volumetric and molar ion concentration, respectively. The insets in (a) are zoom-ins into each electrode vicinity. The cation density in shown in solid lines, while the net ion density is indicated by circles in the left inset. The left and right y-axes in (b) each show the electric field in V/nm and MV/cm. The blue and yellow boxes indicate the location of the Stern layers and metal contacts, respectively.

To better visualize how the EDLs charge up, Fig. 2.5 shows (a) the ionic concentration at the interfaces and (b) the EDL charge and capacitance density over time. Fig. 2.5(a) shows how, starting from the initial concentration n_0, the ionic concentration at the electrode of opposite (dashed lines) and same (dotted lines) polarity changes non-linearly over time. Ions repelled by the electrode of the same polarity drift away from it, lowering their concentration at the interface to ~ 7×10^{18} cm^{-3} in 250 μs, as the inset in (a) shows, after which it increases only slightly over time due to the increased concentration gradient, eventually reaching ~ 8×10^{18} cm^{-3} after 1 ms. This reflects the already-discussed time evolution of the concentration profile at the electrode of the same polarity seen in the right inset of Fig. 2.4(a).

The inset in Fig. 2.5(a) shows that the ionic accumulation at one electrode is only symmetric with the depletion at the other for around 200 ns. Afterwards, the ionic accumulation continues to increase linearly while the ionic depletion at the other electrode settles on a value orders of magnitude lower. This is because while the cation concentration at the positive electrode can only vary between n_0 and 0, the change in n_+ can be much greater at the negative electrode, where it is capped at n_{MAX} ~ 1.56×10^{22} 1/cm^3 by the steric limit set by the finite ion size. Thus, cations can accumulate faster at the negative electrode than they deplete the positive-electrode vicinity in the first tens of microseconds.

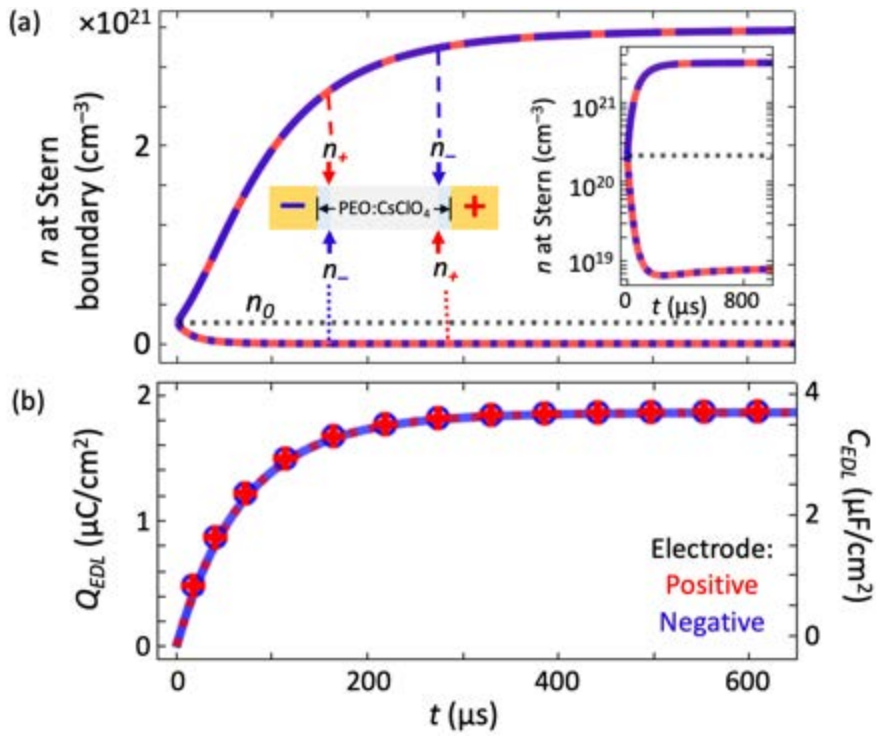


Fig. 2.5 Time evolution of the ionic concentration and EDL charge and capacitance density in response to an applied bias of V_{IN} = 1 V. (a) Concentration of cations, n_+, and anions, n_-, at the left and right edges of the PEO (x = 0.2 and 9.8 nm, respectively). The time dependence of the accumulated (dashed) and depleted (dotted) peak concentrations are shown. The black dotted line indicates the initial equal ion concentration of cations and anions. The inset is a semilogarithmic plot from 0 to 1 ms. (b) Charge (dotted lines; left y-axis) and capacitance (markers; right y-axis) density of the EDL at the positive (red) and negative (blue) electrodes.

The combined effect of ion accumulation at the electrode of the opposite polarity and depletion from the electrode of the same polarity leads to a net charge density at the EDLs, as the left y-axis in Fig. 2.5(b) shows for both positive (red dotted line) and negative (blue dotted line) electrodes. Again, this net charge of one of the EDLs, Q_{EDL}, was obtained by integrating the net ionic concentration, $n_{NET} = n_+ - n_-$, from x = 0.2 to 0.5 nm. The right y-axis of Fig. 2.5(b) shows the EDL capacitance, indicated by markers.

The EDL capacitance is shown again on the left y-axis of Fig. 2.6(a), this time using a logarithmic time scale. The right y-axis shows the percentage of the steady-state C_{EDL} for a 1 V applied bias, marked in yellow in the inset of Fig. 2.3(a). The EDL capacitance reaches 3.7 μF/cm^2 after 1 ms, which already is 99.7% of the steady-state C_{EDL}. The capacitor goes from 10% to 90% charged in ~168 μs.

The 3.7 μF/cm^2 EDL capacitance is slightly less than the capacitance density of a parallel-plate capacitor with the permittivity of vacuum and thickness d equal to the 0.2 nm of the Stern layer, $d = t_{Stern}$, so that $C_{Stern}/A = \varepsilon_0/t_{Stern}$ = 4.4 μF/cm^2. This is consistent with the net ion concentration at 1 ms, shown in the inset of Fig. 2.6(a), which indicates that the EDL extends into the PEO film beyond the Stern layer. Thus, there is a second capacitor, consisting of a more diffuse ionic layer and the permittivity of PEO, in series with C_{Stern}, thereby reducing the total EDL capacitance to 3.7 μF/cm^2.

The time evolution of the electric field, E, is shown in Fig. 2.6(b), again using a log time scale, for three locations indicated by arrows in the inset: the Stern boundaries (x = 0.2 and 9.8 nm) and at the midpoint, x = 0.5 nm. As seen in the electric-field profile in Fig. 2.4(b), while the electric field at the Stern boundaries increases and saturates as the EDLs charge, less of the applied bias drops across the bulk, thereby slowing further ion drift to continue charging the EDLs. As the left inset of Fig. 2.4(b) shows, after a few tens of microseconds of applied bias, the electric field in the bulk drops by several orders of magnitude, essentially halting the EDL charging in this timescale.

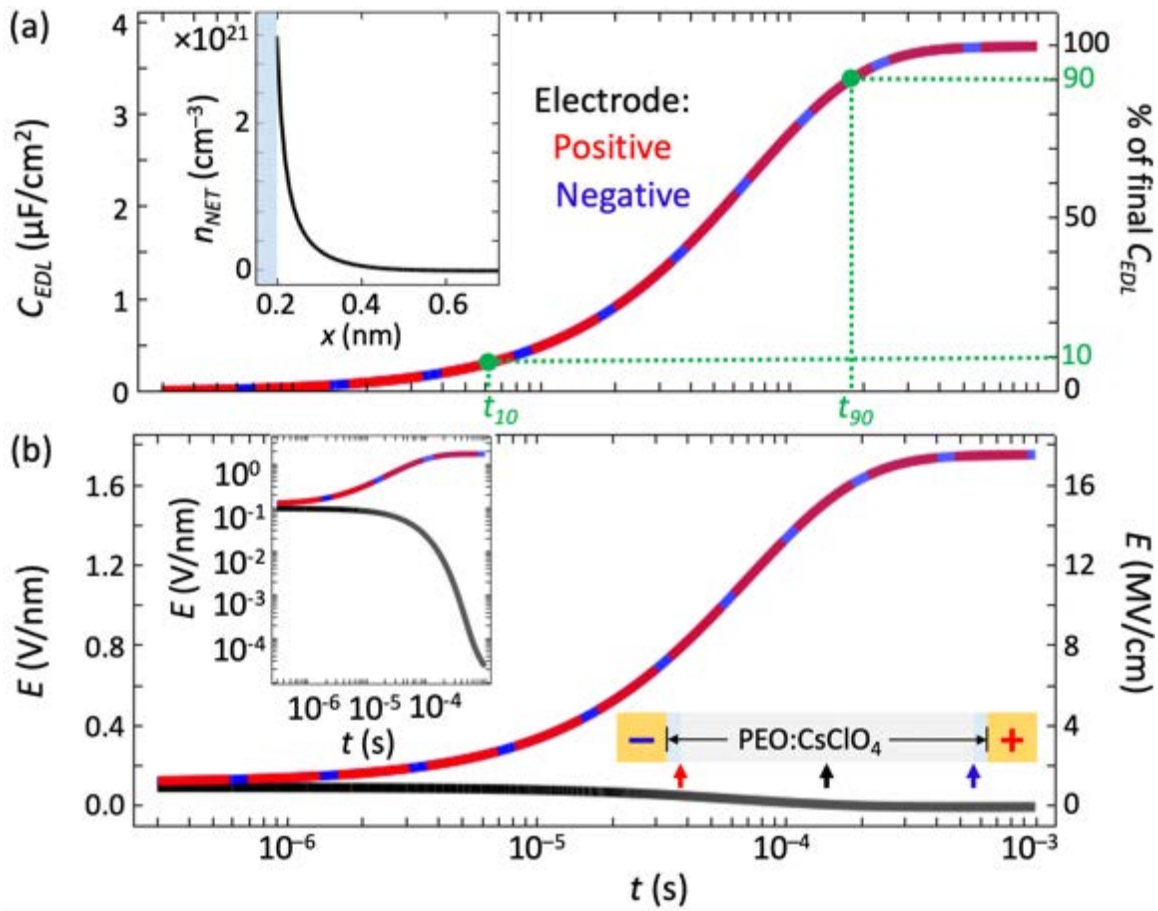


Fig. 2.6 Simulated time evolution of the EDL capacitance density and electric field at various depths of the PEO film after a bias of V_{IN} = 1 V is applied across the PEO:$CsClO_4$ film. (a) Charging of the EDL capacitance at the positive (red) and negative (blue) electrodes over time. The right y-axis shows the percentage of the steady-state C_{EDL}. The 10%–90% charge time is marked in green dotted lines. The inset in (a) shows the net ion concentration profile near the positive electrode at 1 ms. (b) Electric field vs. time at the locations marked by arrows in the right inset: mid-bulk (black), x = 0.2 nm (red), and x = 9.8 nm (blue).The left inset in (b) shows a log-log plot of *E*.

The prior results show that the significant changes in ion concentration, electric field, surface charge density, and EDL capacitance all happen within the microsecond timescale. This is also where most of the current decay takes place. This can be seen in the *J-t* plots in Fig. 2.7, which show the current density (indicated with a solid line) circulating through the circuit in the inset after a 1 V bias is applied. As observed

experimentally [38, 55], the current density exhibits an initial peak, here of ~25 mA/cm^2, followed by a decay of more than 3 orders of magnitude spanning ~3 time decades.

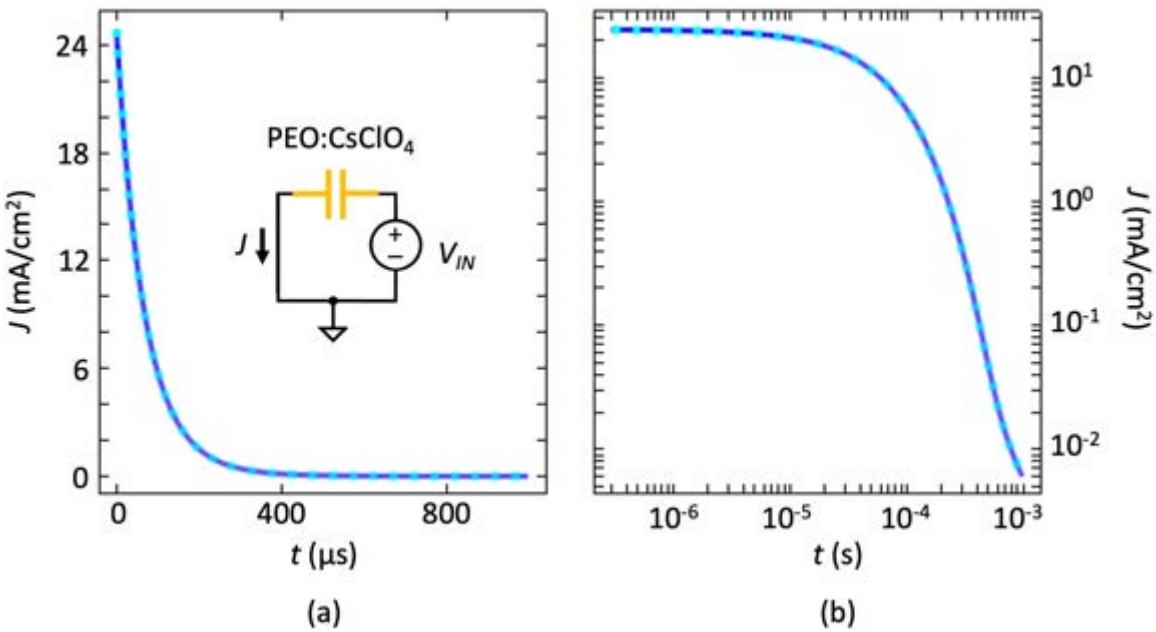


Fig. 2.7: Current density flowing through the circuit in the inset vs. time after applying a bias of V_{IN} = 1 V, shown in an (a) linear and (b) logarithmic scale. The simulated current and the displacement current at the Stern layer are indicated with solid and dotted lines, respectively.

Given current continuity, the current density can be calculated as the electric displacement current at the Stern layer, due to a change in the electric field across the Stern layer, E_{Stern}, over time: $J = \frac{\varepsilon_0 d(E_{Stern})}{dt}$. This is indicated with markers in Fig. 2.7, showing that this calculation matches the external circuit's current density directly outputted by COMSOL.

The effect of thinning the PEO film in the ion dynamics is examined next. Fig. 2.8 shows the time progression of the EDL capacitance and electric field in PEO films of

thicknesses between 5 and 20 nm. The insets in Fig. 2.8(a) and (b) show the net ion concentration profile vs. position and the 10% to 90% charge time of the EDL capacitance vs. PEO thickness, respectively. Fig. 2.8(a) shows that all films eventually achieve the same final C_{EDL} because, as seen in Fig. 2.8(b), all films reach the same steady-state electric field at the Stern layer and thus, the same net ion concentration profile, indicated by a dashed gray line in the inset of Fig. 2.8(a). However, thinner films reach the steady state hundreds of microseconds faster, inset of Fig. 2.8(b), because they experience a higher electric field cross the film from the onset, leading to faster ion drift, which is proportional to E, and thus, greater ion accumulation and higher C_{EDL} for a given time in the transient response.

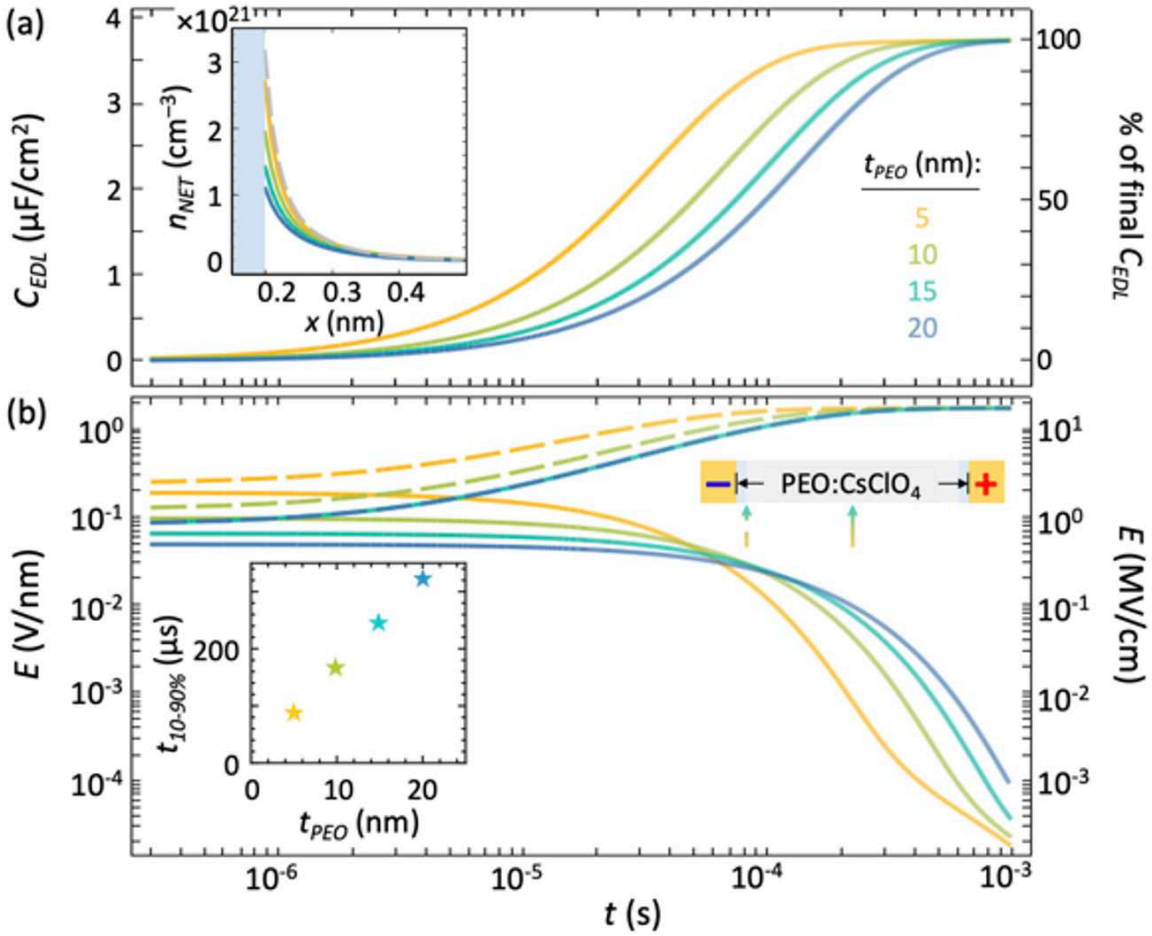


Fig. 2.8 Simulated time progression of the EDL charging and the electric field at various depths of the PEO film after a 1 V bias is applied, for four PEO film thicknesses. (a) EDL capacitance density (left y-axis) and percent of the steady-state C_{EDL} (right y-axis) achieved at a given time. The inset shows the net ionic concentration vs. position near one electrode at 100 μs (colored lines) and 1 ms (gray dashed line). (b) Time evolution of the electric field in mid-PEO (solid lines) and at the edge of the Stern layer with the rest of the PEO film (dashed lines), as indicated by the schematic diagram. The inset in (b) shows the 10% to 90% charge time vs. PEO thickness.

The time evolution of the current density for various PEO:$CsClO_4$ thicknesses is shown in Fig. 2.9 using (a) linear and (b) logarithmic scales. The current peak increases for thinner films, given that the electric field at x = 0.2 nm is higher, which in turn increases the displacement current in this layer. The current decay is also more pronounced, with the 5 nm film having almost an order of magnitude less current at t = 1 ms than the 20 nm film.

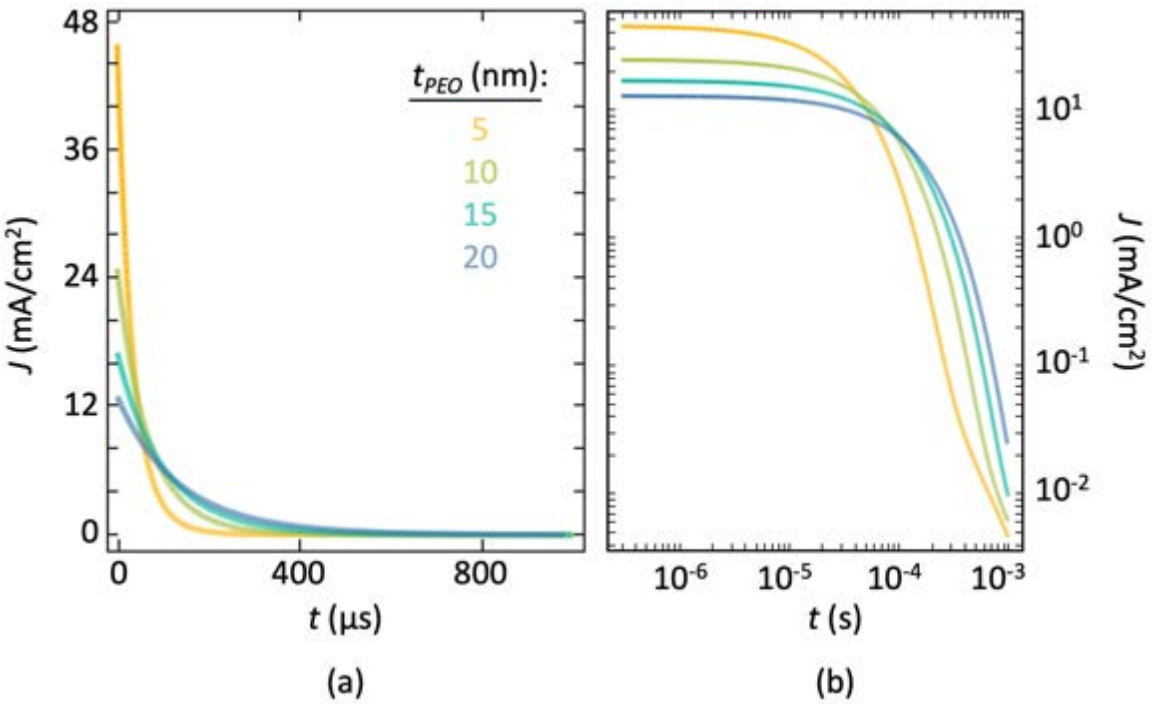


Fig. 2.9 Simulated current density vs. time after applying a 1-V bias to various thicknesses of PEO:$CsClO_4$ film, shown in (a) linear and (b) logarithmic scales.

2.5 Conclusion

The transient study shows that, for the 5 to 20 nm film thicknesses explored, most of the steady-state ionic response has been reached after 1 ms of a 1 V applied bias. However, the EDL capacitance is 90% charged much sooner, after only ~176 μs for the 10-nm PEO film. After that time, the decrease in the electric field in the bulk slows down any further ionic drift toward the EDLs, essentially halting it by ~500 μs for the 10 nm film. The time progression towards the steady state happens nonlinearly, with the peak electric field at the Stern layers and the net charge accumulation at the electrodes growing at an increasing rate after ~1 μs, after which they continue to rise linearly for tens of microseconds before saturating and resulting in a steady-state EDL capacitance of around 3.7 $\mu F/cm^2$. The displacement current density exhibits an initial peak and subsequent decay, with larger peaks and faster decays seen in thinner films, corresponding to the higher electric field and producing faster ionic drift. While films of various thicknesses achieve the same EDL capacitance, thinner films reach their steady-state charge faster, with a 5 nm film reaching a 90% charged state ~250 μs faster than the 20-nm film. If the applied voltage is limited, thinner PEO:$CsClO_4$ films offer the advantage of faster charging rates due to the higher electric field.

CHAPTER 3:

NANOSCALE SOLID POLYMER ELECTROLYTE FOR MEMORY AND COMPUTING

3.1 Overview

Having observed the theoretical ion dynamics describing EDL charging in ideal capacitors with decananometer-thick PEO:$CsClO_4$, we now turn to fabricated systems in which PEO:$CsClO_4$ has been spin-coated onto various substrates, some of which have nanometric features such as CNTs. Dropcasting processes for depositing PEO on CNTs have not been as effective or reproducible as on 2D crystals. It has often been assumed that PEO either does not coat CNTs effectively or that an interfacial layer forms, which acts to set the ions back from the semiconductor, thereby reducing the geometrical capacitance and induced carrier density. High-resolution imaging can expose unexpected gaps, residues, or contaminants at the PEO/CNT interface. This chapter reports on the imaging of CNTs embedded in a PEO polymer matrix, both by high-resolution TEM (HRTEM) and scanning TEM (STEM) combined with EELS imaging. The latter also permitted imaging the distribution of Cs in the polymer matrix.

In this study, record thin PEO:$CsClO_4$ films are demonstrated on Si and CNTs-on-quartz for potential applications in transistors and neuromorphic computing. Spin coated films as thin as 7.8 nm, commensurate with VLSI electronics, are shown to surround CNTs without interlayers. EELS mapping reveals the uniformity of Cs in PEO at the decananometer scale. Evaporated SiO_2 on PEO is demonstrated as a capping layer for further lithography.

3.2 Introduction

Ion-containing polymer dielectrics are being explored in electron devices at the decanometer scale for junction formation and reconfiguration, dynamic memory, and neuromorphic functions. As detailed in Table 1.1, spin-coated films of PEO without an added salt have been achieved as thin as 40 nm by Dalnoki–Veress [46], 14 nm by Schönherr and Frank [41], and 13 nm by Seung [41]. In contrast, studies of PEO with a salt are mostly of micrometer-thick films. Scaling down the polymeric film's thickness can alter its physical behavior with respect to the bulk properties, including its conductivity, morphology, and degree of crystallization [40, 41], which can affect how it coats nanometric structures. Moreover, the addition of a salt is known to affect the film structure of PEO [56].

Here, PEO:$CsClO_4$ films are achieved in the range of thicknesses of 7 to 11 nm, a scale relevant to nanoscale device applications, obtained on SOI and CNT-on-quartz substrates. This chapter reveals the physical attributes of a fabrication process that has shown remarkably ideal capacitance-voltage behavior [57, 58]. The films are characterized in cross–sectional images by TEM and EELS, as summarized in Fig. 3.1, to reveal the coating of structures with nanometer features. Through EELS analysis, the polymer's amorphous carbon character is distinguished from the sp^2–hybridized carbon of the CNT. With SiO_2 evaporated over the PEO, Cs is observed to be contained within PEO, which can serve as a capping layer for further lithography. EELS mapping reveals the unbiased accumulation of Cs at the PEO/SiO_2 interface due to the built-in electric field. In the coating of 2-nm-diameter CNTs, EELS mapping shows that PEO:$CsClO_4$

closely surrounds the CNT wall, with no indication of interlayers, as desired for electric double layer formation used in transistors and neuromorphic applications.

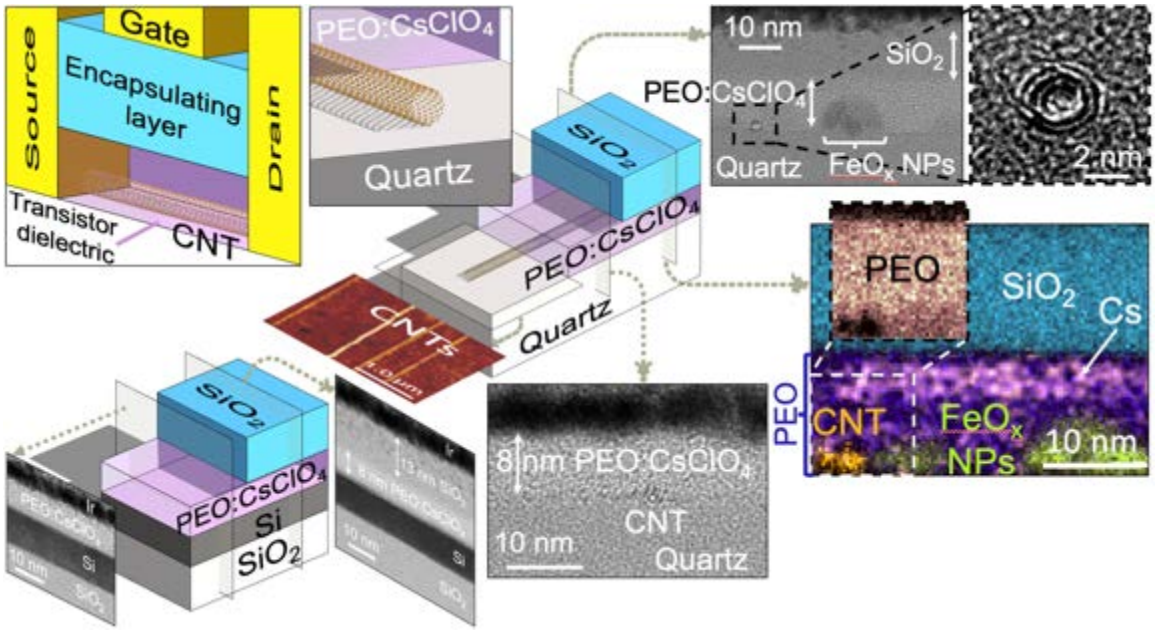


Fig. 3.1 Schematic summarizing the characterized device structures and measured TEM and EELS cross-sections discussed in this chapter.

3.3 Experimental section

Two sample sets were prepared on two different substrates, one a commercial SOI wafer and the other being CNTs-on-quartz. Fig. 3.2 shows the CNT-on-quartz starting substrate (from Greg Pitner, Stanford University), consisting of aligned CNTs with a density of ~2 CNTs/μm. The wafers were cleaned using conventional surface preparation steps before spin coating PEO:$CsClO_4$.

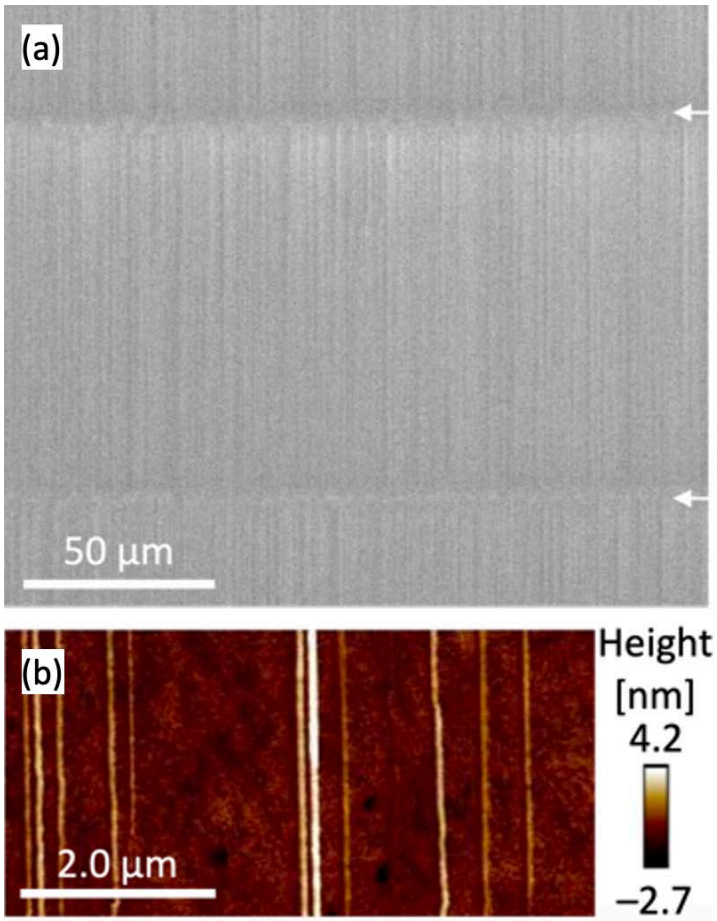


Fig. 3.2 Plan-view images of CNTs on quartz: (a) scanning electron microscope and (b) AFM images. The CNTs were grown between Fe catalyst lines (white arrows) and have a density of ~2 CNTs/µm.

$CsClO_4$ (Sigma Aldrich, 99.995% purity) was dissolved in PEO (molecular weight, 110,000 g/mol, Polymer Standards Service PSS-peo110k) as reported [19], at room temperature in an Ar glovebox (99.999% Ar, H_2O <0.1 ppm, O_2 <0.1 ppm). The PEO:$CsClO_4$ solution was spin coated at 8,000 rpm, using a previously detailed process [58], on: a) 1.3×1.3 cm^2 SOI (12 nm Si / 20 nm SiO_2 / (100) Si), RCA–cleaned[4] and HF–dipped immediately before spin coating and b) similarly-sized quartz wafers with aligned CNTs, solvent-cleaned in hot acetone and isopropyl alcohol for 5 minutes each, rinsed in DI water for 30 s, and dried with N_2. Substrates were then hot-plate baked at 50 °C for 10 minutes in Ar to evaporate the remaining solvent. For each substrate, after spin coating of PEO:$CsClO_4$, one wafer was capped with ~13 nm of e-beam evaporated 99.99% SiO_2 (base pressure 4×10^{-7} Torr; O_2 pressure 3.5×10^{-4} Torr, deposition rate 0.5 Å/s) while the other wafer was left uncapped.

Cross-sections of each wafer were prepared for TEM and EELS spectral imaging using focused ion beam milling (FEI Helios G4 Ux DualBeam) after depositing a protective Ir/Pt cap to preserve the structure. CNTs-on-quartz wafers were cut perpendicular to the nanotube axis. TEM images were taken in an FEI Titan 80-300 kV in bright–field mode; scanning electron microscope images were taken in an FEI Magellan 400; and atomic force microscope images were taken in a Bruker Dimension Icon system in an Ar Glovebox.

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4 The RCA clean consists of a 10 minute dip in the following baths: Piranha (3 : 1 H_2SO_4 : H_2O_2), RCA 1 (40-50 : 1 : 1 DI : NH_4OH : H_2O_2), and RCA 2 (40-50 : 1 : 1 DI : HCl : H_2O_2), with a DI rinse in between baths.

The EELS spectra were acquired using a JEOL F200 STEM (200 keV, 0.1 nm beam spot size) equipped with a Gatan quantum image filter and spectrometer with a direct-detection electron-counting camera (K2 Summit, energy resolution 0.5 eV). The EELS STEM dataset was collected using a beam current on the order of 20 pA, with a 3 – 4 Å probe size, and an exposure time per spectrum of 15 and 1 ms for CNT and SOI scans, respectively. No signs of electron-beam damage were observed. Each capped specimen was first imaged under ADF STEM mode to select the desired scan region.

3.4 Results

Titan TEM cross-sections of (a) uncapped and (b) capped PEO:$CsClO_4$/SOI are shown in Fig. 3.3. The wafers were imaged with HRTEM in bright–field mode. The spin coating of PEO:$CsClO_4$ on SOI resulted in an ~8 nm film. The deposition of the ~13 nm SiO_2 layer did not alter the PEO thickness. This may be due to the way PEO crystallizes in films that are only a few nanometers thick: the polymer chains fold into a serpentine composed of several ~10-nm long segments, each oriented perpendicular to the substrate's surface, which is known as a flat-on orientation [59, 60]. The top few nanometers of the SiO_2 film appear to show an interpenetration of the Ir cap. The lower surface of the SiO_2 at the PEO interface is relatively smoother than the upper surface. Considering 12 equidistant points along a 312 nm lateral line under the capped PEO (imaged at 145,000×), the average thickness is 7.8 ± 0.6 nm. This thickness is to our knowledge the thinnest spun film of high molecular weight PEO:$CsClO_4$ reported to date.

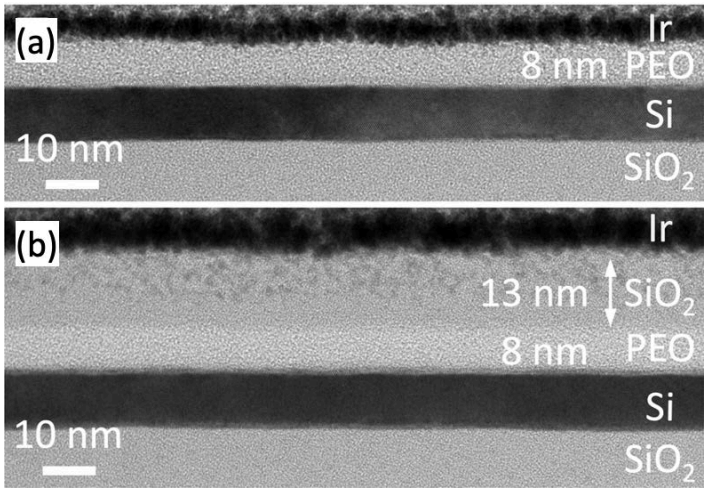

Fig. 3.3 High-resolution TEM images of PEO:$CsClO_4$ on SOI: (a) uncapped PEO and (b) SiO_2-capped PEO. Ir is deposited to protect the wafers during focused ion beam milling.

A Titan TEM cross-section of PEO:$CsClO_4$ on the CNT-on-quartz substrate is shown in Fig. 3.4(a). The cross-section contains two CNTs embedded in an approximately 8-nm-thick PEO film. Fig. 3.4(b) shows a CNT in capped PEO:$CsClO_4$, 11 nm thick, with a zoom-in of the CNT shown in Fig. 3.4(c–d). The nanotube has multiple walls. Several iron oxide nanoparticles (NPs) from the seeding/growth process can also be seen in Fig. 3.4(b–c), on the quartz surface.

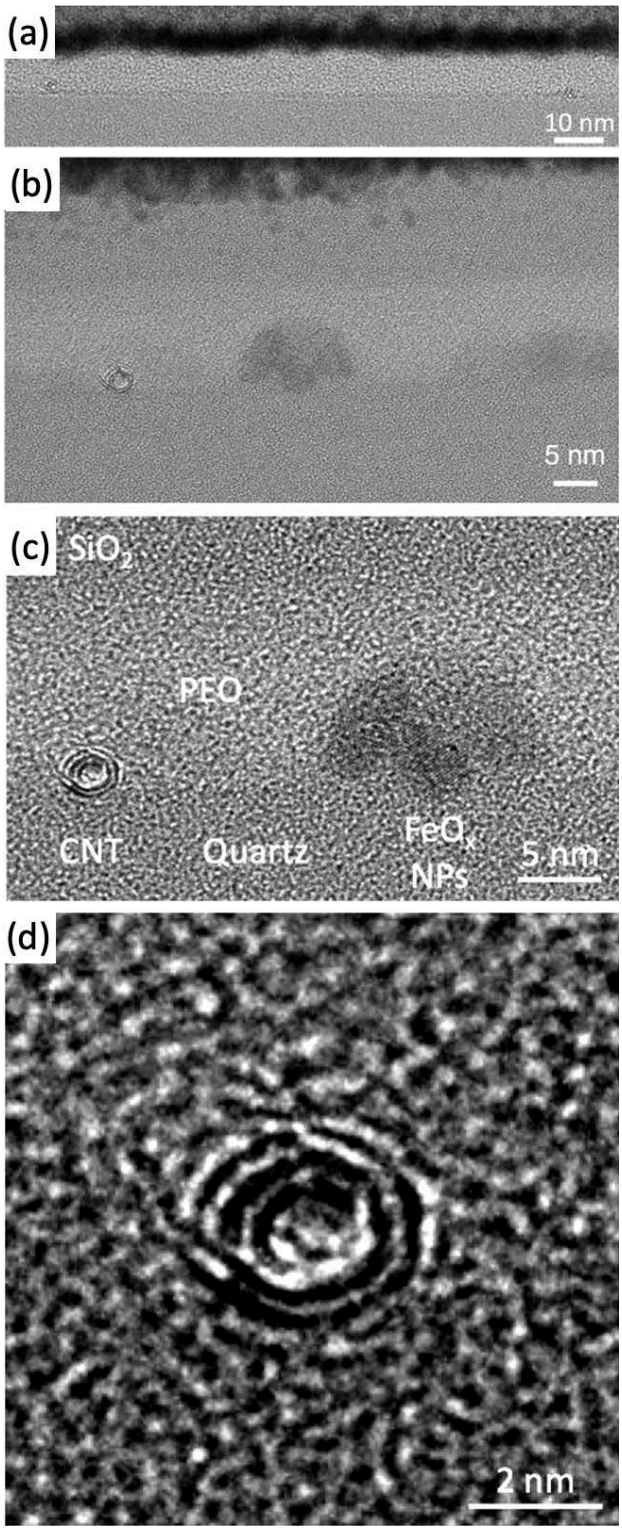

Fig. 3.4 High-resolution TEM images of PEO:$CsClO_4$ on CNTs-on-quartz. (a) CNTs coated with PEO. (b) CNT and iron oxide NPs coated with PEO and capped with SiO_2. (c–d) Increasing zoom–in into the CNT.

EELS analysis was carried out in a JEOL F200 STEM, starting by selecting the scan region in annular dark field (ADF) STEM mode, as shown in Fig. 3.5(a). From a microscopy perspective, the challenges lie in the nature of the specimen. CNTs embedded in a polymer matrix of COH atoms are not visible using ADF STEM because the total atomic weight is similar, making contrast too low to distinguish the two different C phases. Carbon-based materials are particularly beam sensitive and for this reason beam current is kept low (<20 pA). In the CNT wall, carbon is in a double-bonded sp^2 configuration. This configuration is revealed in the EELS spectrum, shown in red in Figure 4b, where the strong and pronounced π* peak is apparent. The K2 detector [61] is capable of counting single electrons, thus removing instrumentation and photoconversion errors arising in scintillator-based detection schemes. With this detector, we were able to locate the sp^2 C rich phase typical of a CNT while avoiding beam damage of the specimen.

In the SiO_2-capped PEO on CNT-on-quartz wafer, analysis of the EELS spectra from the PEO area between the quartz substrate and the SiO_2 cap reveals a C K–edge with features corresponding to amorphous carbon, shown in blue in Fig. 3.5(b). There, the C K–edge exhibits a weaker π* peak relative to the CNT π* peak (Fig. 3.5(b), red). This is because in PEO, C atoms are in a mixture of sp^2 and sp^3 phases, with a lower percentage of C atoms in a sp^2 configuration vs. a CNT, thereby resulting in a weaker π* peak. Notably, the π* peak in the spectra extracted from the polymer layer appears to be split, indicating the presence of some degree of C-O bonding, as expected from the chemical structure of PEO.

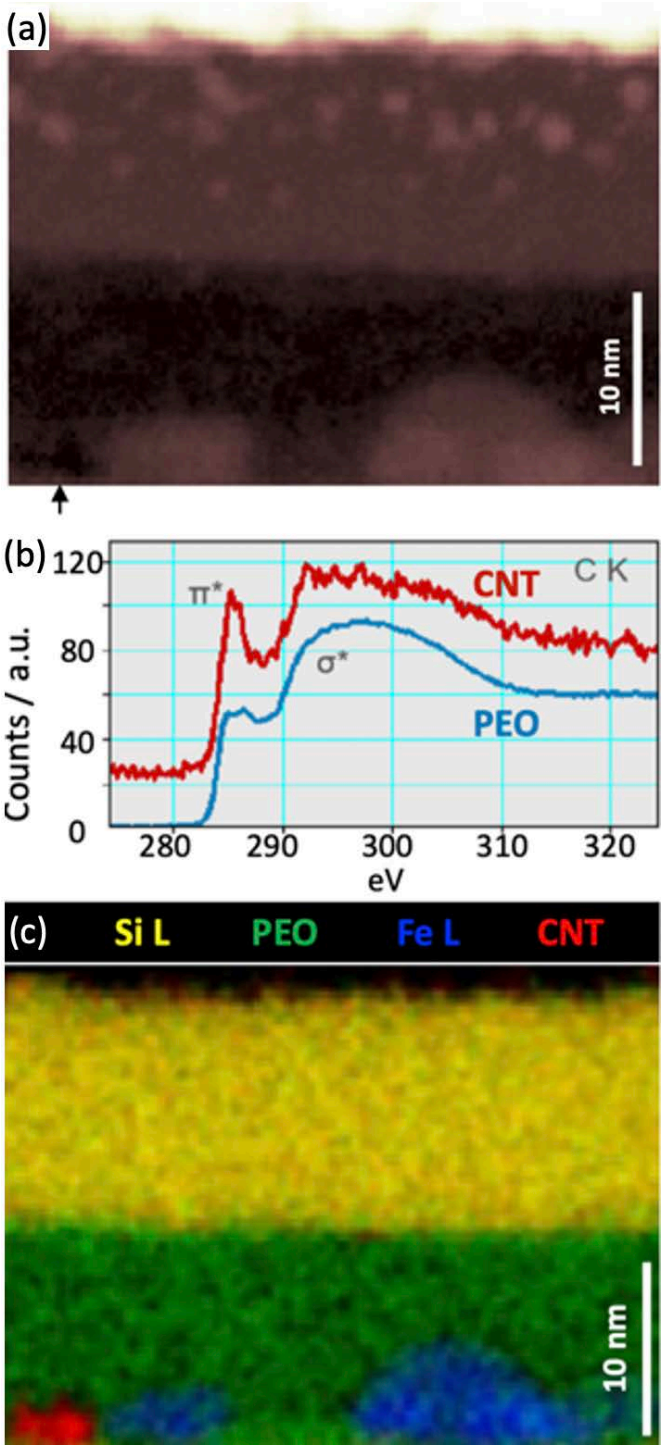

Fig. 3.5 (a) ADF STEM survey image of the scan region. An arrow marks the location of a CNT detected using EELS chemical mapping. (b) EELS spectra of two carbon allotropes: amorphous carbon from the PEO layer (blue) and sp^2-hybridized carbon from a CNT (red), with a pronounced π* peak. The curves were normalized to the same σ* maximum and vertically displaced for visibility. (c) EELS colorized elemental and chemical map distinguishing Si, Fe, amorphous C (PEO), and sp^2-hybridized C (CNT).

The two carbon allotropes were chemically mapped out, Fig. 3.5(c), using their distinct C K–edge features, as previously utilized by Su [62]. Fig. 3.5(c) also shows the elemental maps of Si and Fe. The spectra from the cap region shows a Si L edge with the typical fine structure of SiO_2, while the NP region contained an Fe L edge (not shown) which together with the NP shape, size, and focused-ion-beam cut along the Fe catalyst line confirms that these are iron oxide NPs used in the CNT growth process [28]. This map shows no substantial interfacial layers or gaps at the CNT/PEO interface. PEO can be seen to fully surround the nanostructures.

The EELS spectra from the PEO layer also exhibited the Cs M4,5 features, Fig. 3.6(a), thereby enabling the detection of the ~0.19 atomic percent of Cs in the polymer film. The Cs M4,5 spectrum was superimposed and normalized to the same maximum as a standard Cs M4,5 spectrum extracted from the atlas reference library in Gatan DigitalMicrograph. The close match with the reference spectrum of Cs confirms the presence of Cs.

The detected Cs M4,5 features allowed imaging the Cs distribution in PEO for the first time, Fig. 3.6(b), showing that Cs is confined to the PEO matrix. There is a notable increase in the intensity of the Cs signal near the SiO_2/PEO, which likely indicates the accumulation of Cs^+ ions due to the built-in electric field of the heterostructure. Iron oxide NPs are also visible in the lower portion of the PEO layer. Cesium was not detected in the SiO_2 layer, suggesting an effective encapsulation. An arrow in Fig. 3.6(b) marks the scan region where the CNT was detected. Here, a faint dark circle indicating the CNT can be seen with Cs in proximity and in the interior. It is known that Cs can be inserted into CNTs, reported by Senga [63] using STEM with EELS.

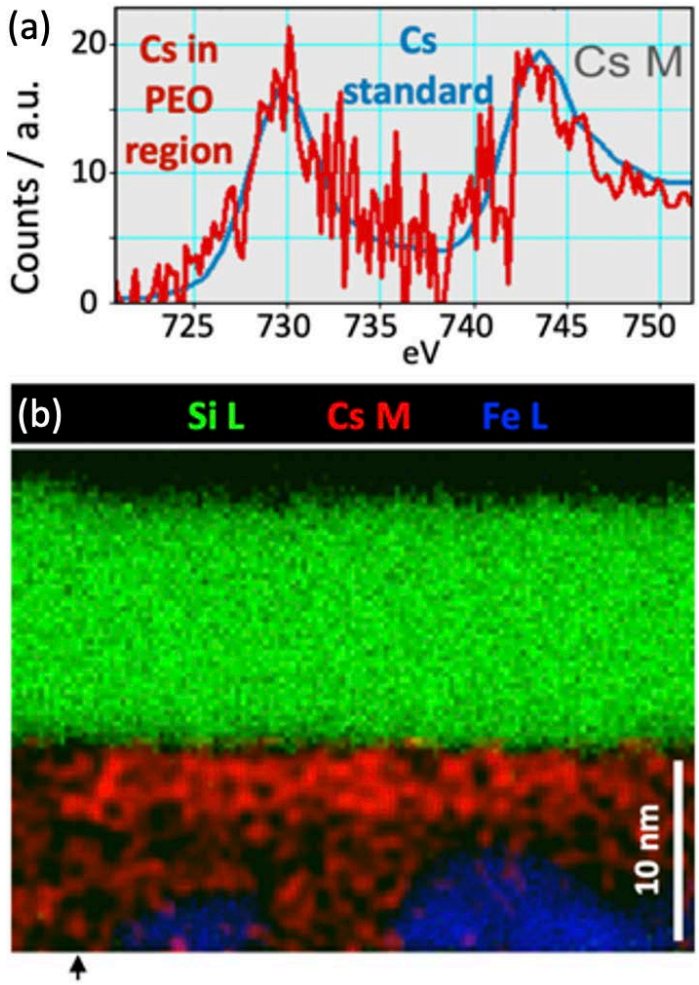

Fig. 3.6 (a) EELS spectra of Cs extracted from the PEO region (red) vs. a Cs standard (blue). (b) EELS colorized elemental map distinguishing Si, Cs, and Fe. An arrow marks the CNT location where Cs is apparently observed inside and outside of the CNT.

The anion ClO_4^- was not imaged in these experiments. While the Cs M4,5 edge in PEO's COH matrix is pronounced and easy to identify, the same amount of Cl from the ClO_4^- anion is not readily observed. This is because of the shape of the Cl L-edge at 200 eV is not easily resolved. In a typical EELS spectrum, the peak to background ratio increases with energy loss, which suggests using the Cl K at 2.8 keV; however, in our measurements, the Cl intensity is too low at the beam currents needed to stay below the damage threshold.

3.5 Discussion

The semiconductor/PEO:$CsClO_4$ interface is shown here to be flat at the nanometer scale, with the Cs^+ ion content relatively homogeneously distributed. The capacitance-voltage characteristics of Pd/Ti/PEO:$CsClO_4$/Si metal oxide semiconductor capacitors, formed using this same spin process, have recently been shown to have electrical properties in good agreement with the physical dimensions and with low leakage [58]; this is also discussed in the next chapter. The Si/PEO:$CsClO_4$ interface is polarizable with Cs^+ cations or ClO_4^- anions, and can achieve surface charge densities similar to ferroelectric materials, e.g. hafnium zirconate [64]. Unlike ferroelectrics, which switch abruptly about a coercive field, the Si/PEO:$CsClO_4$ and metal/PEO:$CsClO_4$ interfaces polarize continuously with applied electric field. Thus, many different levels of EDL strength can be achieved at these interfaces.

3.6 Conclusions

The physical characteristics of PEO:$CsClO_4$ were measured at the nanometer scales of interest for VLSI. We have shown that spin-coated films can be achieved with thickness of 7.8 nm, thinner than prior reports. TEM images show that the coating is homogeneous and the coating of nanostructures is effective even on 2-nm-diameter CNTs, without visible interlayers, as desired for electric double layer formation. We have been able to image Cs in PEO by EELS, also not previously reported, and show that it is well confined in the polymer and distributed within the PEO film. The Cs also appears to be substantially confined by an evaporated SiO_2 cap, which has been added for the purposes of encapsulation and to enable subsequent lithography. No physical

impediments are indicated for applications of PEO:$CsClO_4$ at the decananometer scale. This solid polymer electrolyte can be used to form electric double layers at polymer/semiconductor interfaces, which is a functionality that can be exploited for memory and nontraditional computing.

CHAPTER 4:

IMPEDANCE-FREQUENCY CHARACTERIZATION OF ULTRATHIN POLYETHYLENE OXIDE CAPACITORS

4.1 Overview

Having observed the physical characteristics of spin-coated PEO:$CsClO_4$ with and without an SiO_2 encapsulation layer, we now turn to characterize the electrical properties of these ultrathin films. The impedance-frequency and capacitance-voltage characteristics of metal/PEO/Si MIS capacitors at thicknesses relevant to transistor technology are measured with and without $CsClO_4$. Basic understanding of the impedance frequency and voltage characteristics of this MIS system is established in spin-coated films in the thickness range from 6 to 19 nm, as determined from capacitance measurements and transmission electron microscopy. Estimates of the dielectric constant, energy band diagram, charge trap density, and conductivity in ultrathin PEO are obtained. Simple equivalent circuits based on resistive and capacitive elements that reflect the physical system are used to model the measured impedance frequency trends and compare films with and without $CsClO_4$ in the polymer matrix. This study reveals the electrical properties of PEO near the limits of thickness scaling, toward memory and neuromorphic device applications.

4.2 Introduction

In the early days of MOSFET development, ions such as Na and K were extensively characterized to understand their source and eliminate them from SiO_2 gate

oxides [65]. Mobile ions in MOSFET oxides introduce hysteresis in the threshold voltage, which is an effect generally to be minimized. However, with recent interest in analog memory for weight storage in neural networks and synapse formation in neuromorphic computing, the hysteretic properties of oxides are inspiring applications [66] [67].

PEO containing an alkali perchlorate has been widely used to electrolytically gate thin film and two-dimensional semiconductors [1, 4, 6, 34, 68]. It is common for the thicknesses in these studies to be in the range of 0.2 – 1 μm, well beyond the thickness scales of VLSI electronics. In this paper, we investigate the electrical properties of spin-coated PEO in the thickness range of 6 – 19 nm. We fabricate MIS capacitors and perform impedance spectroscopy to provide data in a form common to the characterization of solid-state oxides. By comparing PEO with and without the ionic salt $CsClO_4$, we can understand the effect of the salt on the capacitor's electrical properties and show that the solid polymer PEO in ultrathin MIS capacitors has low leakage and remarkably ideal impedance-frequency behavior. This is then compared with PEO MIS capacitors containing the salt $CsClO_4$, which shows that the effects of the ionic content in these ultrathin films are remarkably consistent with prior reports on much thicker films.

4.3 Experimental section

PEO was prepared by spin coating films with and without $CsClO_4$. Conventional Si surface preparation steps were used prior to spin coating, including an RCA–clean and buffered HF–dip. This was followed immediately by transfer into an Ar MBraun glovebox for spin coating, to maintain the O_2 content below 0.1 ppm and thus minimize

exposure of the PEO to water vapor and O_2. The PEO was obtained from Polymer Standards Service (PSS-peo110k). Solutions of PEO with and without $CsClO_4$ were prepared using methods previously described [19]. The $CsClO_4$ is a product of Sigma Aldrich with purity 99.995%, and the mole fraction used was 0.013. The spin coating was applied to 3.5 × 3.5 cm^2 Si (100) substrates with a resistivity of 0.01 – 0.02 Ω-cm, and for two carrier types: *n*–type, Sb, and *p*–type, B. PEO without $CsClO_4$ was spun on *n*–Si wafers at 2, 4, 6, 8, or 10 krpm. PEO either with or without $CsClO_4$ was spin–coated on *p*–Si wafers at 2, 4, 6, or 8 krpm. Each wafer was spun for 30 s, followed by a hot–plate bake at 50 °C for 10 minutes in the Ar glovebox to evaporate the solvent. Top-electrodes were formed by electron-beam evaporation through a shadow mask; the deposition consisted of a 1 nm Ti adhesion layer followed by 180 nm Pd top electrode. Capacitor diameters of 20, 45, and 63 μm were used to provide normalized area steps of 1×, 5×, and 10×. When not under test in an N_2 ambient, the capacitors were stored in the Ar glovebox to minimize water absorption.

Electrical measurements were made in a Cascade Summit 11000 probe station at room temperature in the dark and in flowing N_2. A Keithley 4200A parameter analyzer was used to measure impedance Z, parallel capacitance, C_P, and conductance, G_P, vs. the top gate electrode voltage, V_G and frequency, f. For Z, C_P, and G_P vs. f measurements, the gate voltage was applied with a superimposed sinusoid of 30 mV rms. The time over which frequency sweeps (1 kHz to 2 MHz) were taken was 284 s; this is relevant to the electrode polarization/charging state. For C, G–V measurements, V_G was swept from most negative towards positive values in steps of 0.1 V and at 10 mV/s unless otherwise noted. A 10 s hold was applied at the first measurement voltage before the start of data

acquisition.

TEM measurements of a Pd/Ti/PEO/*n*-Si capacitor were made in an FEI Titan 80-300 to establish the physical thickness of spin-coated PEO. Focused-ion-beam milling (FEI Helios G4 Ux DualBeam) was used to prepare the TEM specimens, after an in-situ deposition of a protective Ir/Pt cap. The average PEO thickness of the 8-krpm-coated wafer was determined over a lateral length of 932 nm (82 points) to obtain the physical thickness of ~7.4 nm. Accumulation capacitance measurements were then calibrated to this thickness using a dielectric constant of 1.5. For the remainder of the sample set, capacitance measurements were used to determine the thickness with the same dielectric constant.

4.4 Results and discussion

Shown in Fig. 4.1(a) is the TEM cross-section of a PEO film spun at 8 krpm, showing a thickness of 7.4 ± 1.4 nm. The PEO/Si interface is notably sharp, with most of the thickness variation arising from the upper PEO/metal interface. The measured frequency dependence of the impedance magnitude and phase are shown in Fig. 4.1(b–c) for five different PEO thicknesses. The impedance is well described by a simple capacitance, decreasing inversely with frequency, with a phase of approximately –90°. This ideal capacitance behavior is observed over more than 2 orders of magnitude. The measurement in Fig. 4.1 was made for an accumulation bias of 2 V; however, this ideal capacitive behavior is maintained for all bias conditions spanning the full range of voltages used in the *C*–*V* measurements. The impedance was also found to scale linearly with capacitor area, as expected.

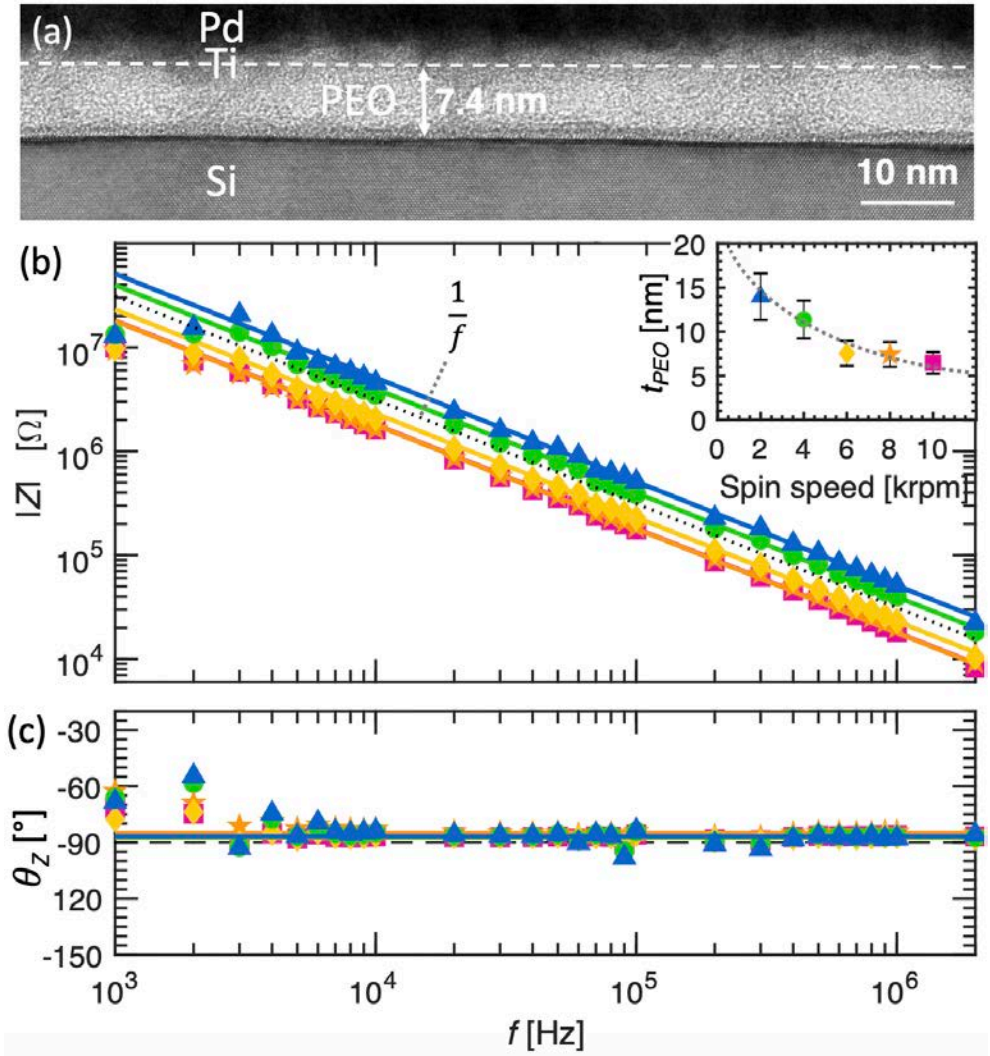

Fig. 4.1 (a) TEM image of a Pd/Ti/PEO/*n*–Si capacitor using PEO spun at 8 krpm, resulting in an ~7.4 nm film. (b) Frequency dependence of the impedance magnitude and (c) phase of 63 μm diameter MIS capacitors of different PEO thicknesses, biased in accumulation at V_G = 2 V. The dotted black line shows the excellent agreement of the measurements (markers) to an ideal capacitor's $|Z|$ with thickness t_{PEO} of 8 nm. Colored solid lines represent model fits to the measurements using a parallel-*RC* equivalent circuit. The inset shows PEO thickness vs. spin speed extracted from the accumulation capacitances with ε_{PEO} = 1.5.

Using the measured physical thickness of 7.4 nm, the capacitor area, and the measured accumulation capacitance at 1 MHz, a relative dielectric constant, ε_{PEO} = 1.5, was obtained. This value is somewhat lower than reported by Nasir *et al.* [69], ε_{PEO} ~2.3, and measured on thick PEO films (600,000 g/mol; thickness, ~250–400 μm) between mm-diameter stainless steel electrodes. Using 1.5 for the dielectric constant, measured thicknesses vs. spin speed were computed from accumulation capacitance measurements and plotted in the inset of Fig. 4.1(b), with error bars given from geometrical uncertainties.

Given the ideal MIS *Z–f* dependence, we can accurately account for the frequency dependence by a parallel capacitance, C_P, and conductance, G_P. From the conductance, the conductivity, $\sigma = G_P t_{PEO}/A$, can be obtained, where A is the area. The resulting semi–logarithmic C_P–f and log–log σ–f plots are shown in Fig. 4.2(a) and (b). As expected for a geometrical capacitor, the measured capacitances are substantially independent of frequency, with a slight increase observed below 3 kHz which will be discussed later. The capacitance density with electrode areas measured by optical microscopy increases inversely with film thickness, again as expected.

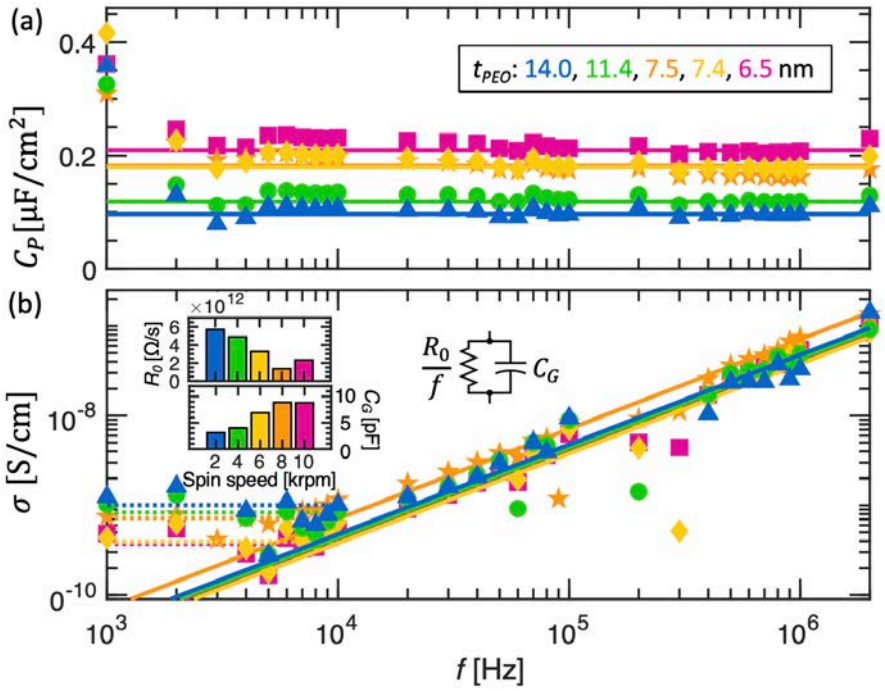

Fig. 4.2 Frequency dependence of the parallel (a) capacitance and (b) conductivity of 63 μm MIS capacitors with different PEO thicknesses biased in accumulation at V_G = 2 V. Dotted lines mark a region of dc conductivity. Solid lines represent model fits to the measurements (markers) from 5k – 2 MHz, using the equivalent circuit in the inset of (b).

The log–log σ–f plot in Fig. 4.2(b) shows a plateau at low frequencies, indicated by dotted lines. This frequency-independent dc conductivity, σ_{dc}, has been previously observed [70] in thicker PEO films. The plateau is followed by a region in which the conductivity increases directly in proportion to frequency spanning more than 2 decades. Such a frequency dependence of the conductivity is a property of many heterogeneous systems such as noncrystalline materials, including PEO [71, 72]. In parallel conductance measurements when the impedance phase is close to –90°, the measured real part of the complex impedance is much smaller than the imaginary part. The conductance of the ultrathin PEO capacitors exhibits a variability which is associated with the low signal level of the real impedance component. This is true here and in measurements to follow.

The simple capacitor behavior of $|Z|$, θ_Z, and C_P, along with the linear frequency dependence of σ for $f \geq \sim 5$ kHz can be modeled by a parallel RC, where C is a geometric MIS capacitance and R is a resistive element that has a linear frequency dependence, with the equivalent circuit shown in the inset in Fig. 4.2(b). The solid lines in Fig. 4.1 and 2 show how closely this model represents the measured behavior (shown in markers) of Pd/Ti/PEO/*n*–Si MIS capacitors.

The measured *C–V* characteristics vs. PEO thickness are shown in Fig. 4.3 and compared with simulated characteristics of an ideal MIS capacitor. The simulated *C–V* characteristic, Fig. 4.3(a), is obtained using the heterostructure Poisson solver BandProf [73]. For the purposes of the simulation, a plausible band diagram is proposed using a PEO band gap from optical absorption measurements of 4.5 eV [74]. The *n*–Si substrate has a doping of $N_D = 1\times10^{18}$ cm^{-3} and our measured value of $\varepsilon_{PEO} = 1.5$ is used. The metal/PEO barrier is placed near midgap, 2.2 eV, and a PEO/Si conduction band offset, ΔE_C, of 1.2 eV leads to a flatband voltage of approximately 1 V. This band diagram is consistent with the *C–V* measurements.

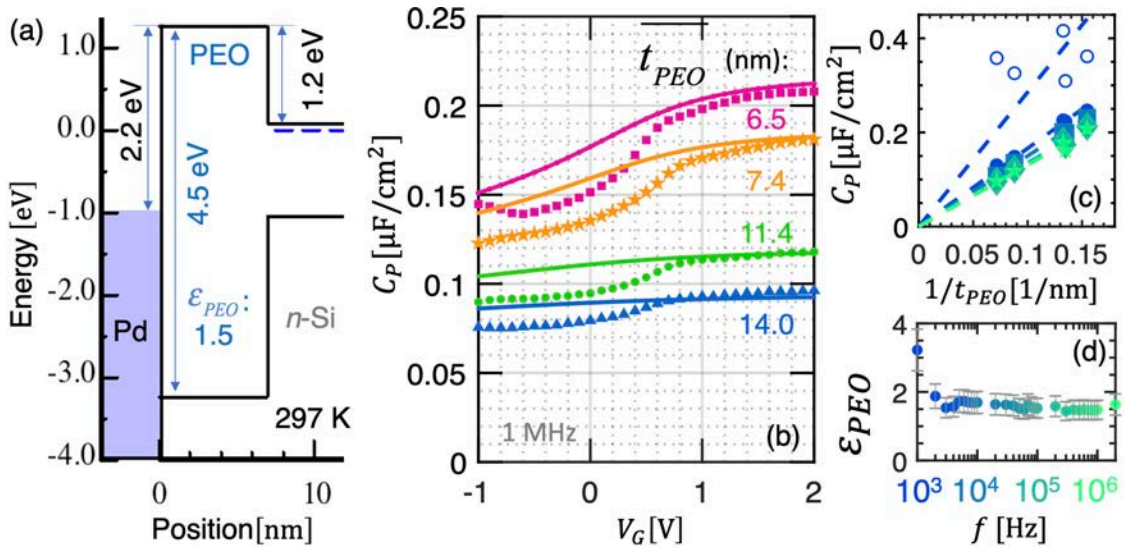

Fig. 4.3 (a) Energy band diagram of a Pd/PEO/*n*–Si capacitor biased at flatband and simulated using the heterojunction Poisson-solver BandProf [73]. (b) Capacitance density vs. voltage in Pd/Ti/PEO/*n*–Si MIS capacitors vs. thickness. Markers indicate measurements made at 1 MHz while biasing from depletion at –1 V towards accumulation at 2 V. The solid lines are the simulations. (c) Accumulation capacitance density (at 2 V) vs. inverse PEO thickness, extracted from TEM and *C*–*V* measurements at 1 kHz (open circles) and 2 k, 10 k, 100 k, and 1 MHz (filled colored circles). Dashed lines show the linear fit, $C = (\varepsilon_0\varepsilon_{PEO})/t_{PEO}$, used to extract ε_{PEO}. (d) Dielectric constant of PEO vs. frequency.

The simulated characteristics generally agree with the accumulation capacitance and minimum capacitance, but the transition to the minimum capacitance happens over a lower voltage span than the simulation predicts. This may arise from residual background ion conductivity in the films. PEO is also known to absorb moisture, which raises its ionic conductivity [75]. Ionic polarization of the PEO surfaces can be expected to alter the capacitance transitions.

The accumulation capacitance density is plotted vs. inverse PEO thickness in Fig. 4.3(c). The linear relation and low frequency dispersion suggest a nearly ideal capacitive behavior across the various PEO thicknesses. The linear fit (dashed lines) of the measurements (markers) was used to extract the dielectric constant of PEO, which as Fig.

4.3(d) shows, has a weak dependence on frequency across most of the frequency range, with ε_{PEO} of 1.9 at 2 kHz and 1.5 at 1 MHz.

The detailed dependence of the capacitance and conductance characteristics vs. slew rate of the gate voltage (using double sweeps) is shown in Fig. 4.4 for MIS capacitors spun at 4 krpm (t_{PEO} ~11.4 nm). The white noise reduction factor in the Keithley 4200A, i.e. filter factor, was varied from 1 to 100, and used to increment the measurement slew rate between 580 and 10 mV/s. For the PEO MIS capacitor on *n*–Si, the flatband voltage is approximately 1 V, and as bias increases electrons accumulate on the Si surface. The hysteresis observed in the capacitance as the voltage is ramped from –1 to 2 V and back corresponds to a bias which ranges from depletion to accumulation, Fig. 4.4(a). Hysteresis in the characteristics in the voltage range above zero can be associated with charge trapping at or near the PEO/*n*–Si interface and reaching a maximum near the flatband voltage, 1 V.

From the voltage shift in the double sweep measurement at fixed capacitance, the density of charge trapped at the PEO/*n*–Si interface can be estimated. In this portion of the *C*–*V* characteristic, the bias ranges from just below flatband to accumulation, so that electron traps in this region are likely located energetically near the conduction band edge. The charge responsible for the hysteresis ΔV_G at a particular C is $\Delta Q = C\Delta V_G$, and from ΔQ the density of mobile charge can be estimated as $N_T = \Delta Q/qA$, where q is the electron charge. This charge density, N_T, is plotted vs. bias and slew rate in the lower right portion of Fig. 4.4(a). Contributions to this hysteresis likely come from electronic traps, but mobile ions in the PEO cannot be ruled out. If the main contribution is electronic, the trap states are located near the Si conduction band edge. For the lowest

slew rate, 10 mV/s, the peak in the mobile charge density occurs at voltages corresponding to accumulation biases. These traps are likely at the Si surface or in the surface border region of the PEO. The slew rate dependence can be explained if the traps have a higher capture rate than emission rate. High slew rates produce the greatest magnitude of accumulated fixed charge. The slower sweep rates allow the traps to fill and empty along with the bias, so that the voltage differences in the double sweep measurement are reduced. The highest accumulated charge is found to be $2.6 \times 10^{11}/\text{cm}^2$.

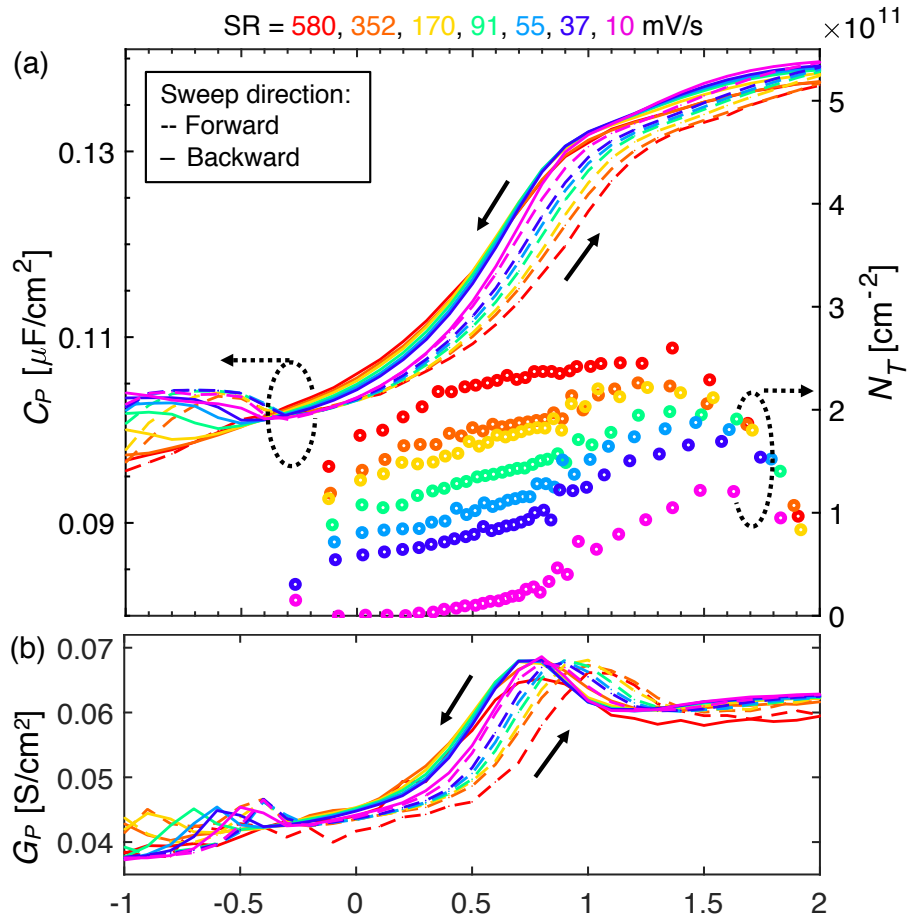

Fig. 4.4 Measured double-sweep slew–rate dependence of a Pd/Ti/PEO/*n*–Si MIS capacitor spun at 4 krpm (t_{PEO} ~11.4 nm) with a diameter of 63 μm. (a) Parallel capacitance, C_P, and density of trapped charge, N_T, vs. voltage, and (b) parallel conductance, G_P, vs. voltage. Forward and backward sweeps are indicated in dashed and solid lines, respectively.

Considering the *G–V* measurement of Fig. 4.4(b), two conductance peaks are observed, and the slower slew rates shift the conductance peaks toward smaller gate voltages. The conductance peaks measured at 10 mV/s are centered around –0.5 and 0.8 V. The upper peak at around 0.8 eV corresponds to a bias near accumulation bias and is likely due to state filling near the conduction band edge of Si. The peak at around –0.5 V is still in the upper half of the Si band gap, as band diagram simulations indicate the valence band is not reached until a voltage of nearly –4 V. The energetic position of the conductance peak near the conduction band edge may suggest the presence of shallow donor traps.

The impedance–frequency characteristics of PEO capacitors with and without $CsClO_4$ are compared in Fig. 4.5, here using *p*–Si substrates. Open and filled markers indicate the measurements of PEO and PEO:$CsClO_4$ capacitors, respectively, biased in accumulation. As was observed in the *n*–Si substrates, the capacitors without $CsClO_4$ exhibit an essentially ideal characteristic, with inverse frequency dependence and –90° phase shift. With the added salt, the impedance magnitude decreases due to the increase in ionic conductivity. In contrast to prior published studies [69, 72] on thick PEO capacitors, the measurements here show an impedance which is more capacitive than conductive. Where the phase reaches 45º, the real and imaginary parts of the impedance become equal. This again is a consequence of the reduced impedance of the PEO:$CsClO_4$ due to the ionic conductivity of the film.

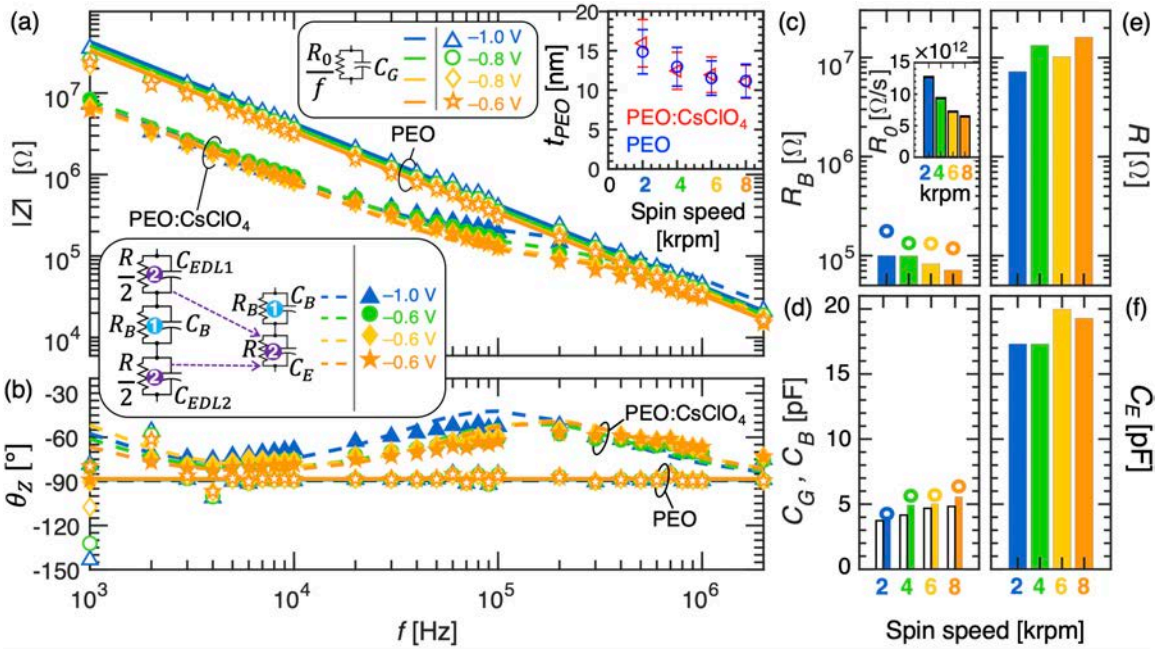

Fig. 4.5 Impedance-frequency dependence comparing Pd/Ti/PEO:$CsClO_4$/*p*–Si and Pd/Ti/PEO/*p*–Si MIS capacitors. (a) Impedance magnitude, $|Z|$, and (b) phase, θ_Z, vs. frequency. The measurements of PEO and PEO:$CsClO_4$ capacitors are indicated with open and filled markers, respectively. The capacitors were biased in the range –0.6 to –1 V corresponding to accumulation biases. Solid and dashed lines represent *RC* model fits to the PEO and PEO:$CsClO_4$ capacitor data, respectively, using the equivalent circuits shown in the insets of (a) and parameters given in (c-f), with the geometrical capacitances computed from the physical geometry with $\boldsymbol{\varepsilon}_{PEO} = 1.5$. The boxed inset in (a) shows the electrical thickness vs. spin speed of PEO without (blue •) and with (red ◀) $CsClO_4$. (c) Bulk resistance R_B; inset shows the R_0 parameter of the frequency-dependent resistance. (d) Geometric capacitance C_G and bulk capacitance C_B for PEO (white bars) and PEO:$CsClO_4$ (colored bars). (e) Resistance R and (f) capacitance $C_E = C_{EDL1}C_{EDL2}/(C_{EDL1}+C_{EDL2})$ at the electrodes. Circles in (c) mark the expected R_B extrapolated from thick PEO:$CsClO_4$ (t_{PEO} ~1 μm) discussed in [76]. Circles in (d) indicate the C_B expected from the same bulk thickness used in the extrapolation of R_B. The left and right axes have the same resistance and capacitance scales.

The PEO and PEO:$CsClO_4$ capacitor data is modeled using the simple equivalent circuits shown in the insets of Fig. 4.5(a) and parameters given in (c-f). The resulting model fits are shown in Fig. 4.5(a-b) in solid and dashed lines for films without and with $CsClO_4$, respectively. Here our aim is to see to what extent the simplest lumped element model can capture the responses which relate to ion transport and the electrode polarization. For PEO capacitors without $CsClO_4$ on *n* and *p*–Si, the essential physics is captured by a parallel *RC* circuit, where the capacitive element is the geometric capacitance and the resistive element is a frequency–dependent resistor, R_0/f.

The PEO:$CsClO_4$ capacitors can be modeled by an equivalent circuit with three *RC* loops in series (inset of Fig. 4.5(a)). One loop, consisting of capacitance C_B in parallel with resistance R_B, represents the charge transport in the bulk of the PEO film [77]. The second and third *RC* loops represent the polarization at the metal and Si electrodes with the capacitor, C_{EDL}, representing an EDL capacitance. This capacitance is shunted by a conductance that represents the charge transfer between the PEO film and the electrodes due to ionic and / or electronic processes. This resistance *R* has previously been referred to as a charge transfer resistance at the solid electrolyte's interface with partially blocking electrodes, and it produces a plateau in the modeled conductivity at low frequencies [77]. The measurements reported here are for biases sufficiently low that the measurements are reversible and repeatable.

The expected bulk resistance, R_B, and capacitance, C_B, of PEO:$CsClO_4$ capacitors are marked by circles in Fig. 4.5(c) and (d), respectively. The anticipated bulk capacitance and resistance were calculated as $C_B = \varepsilon_0 \varepsilon_{PEO} A / t_{Bulk}$ and $R_B = \rho t_{Bulk} / A$, considering $\varepsilon_{PEO} = 1.5$, the resistivity of ~1 μm thick PEO:$CsClO_4$, $\rho \sim 5.67 \times 10^6$ Ω-cm

[76], and the thickness of the bulk, $t_{Bulk} = t_{PEO} - 2t_{EDL}$. The EDL thickness t_{EDL} is estimated from the average EDL capacitance at the PEO/electrode interface, $C_{EDL} = \varepsilon_0 \varepsilon_{PEO} A / t_{EDL}$, obtained from the circuit parameter $C_E = C_{EDL}/2$. The expected R_B and C_B are within the same order of magnitude as the values obtained from the circuit model fits of PEO:$CsClO_4$. For both PEO and PEO:$CsClO_4$ capacitors, R_B drops and the C_B increases with decreasing film thickness as can be expected. Capacitors with $CsClO_4$ have a higher C_B, since the added presence of the EDL capacitors at the electrode / PEO interfaces reduces the bulk thickness compared to PEO films without $CsClO_4$.

The EDL capacitance density estimated from the model fit, $2C_E/A$, which assumes the EDLs at each electrode are equally strong, is ~1.1 μF/cm^2 and may be considered small for an EDL capacitance; 3.7 μF/cm^2 can be expected from the COMSOL Multiphysics simulations in Chapter 2, while prior measurements in this solid polymer electrolyte yielded 4 μF/cm^2 [14]. The lower C_{EDL} in these ultrathin PEO:$CsClO_4$ capacitors is likely due to the roughness of the Pd/Ti/PEO top electrode, see Fig. 4.1(a), in contrast with the flatter PEO/Si bottom electrode. The resulting difference in the space-charge separation at the top and bottom electrodes can lead to different EDL capacitances at each electrode, C_{EDL1} and C_{EDL2}. These two capacitances in series form the capacitor C_E in the inset of Fig. 4.5(a). If at the flatter PEO/Si electrode C_{EDL1} is 3.6 μF/cm^2, while at the rougher Pd/Ti/PEO electrode C_{EDL2} is lower, say 0.7 μF/cm^2, the total capacitance density C_E would be ~0.6 μF/cm^2 and the EDL capacitance, assuming both EDLs where equal, would be ~1.2 μF/cm^2. Thus, the lower-than-expected C_{EDL} may arise from non-uniformities in the top-electrode.

Again, the *Z–f* data of PEO and PEO:$CsClO_4$ capacitors is used to calculate the parallel capacitance density, C_P, from which the effective dielectric constant, ε_r, can be extracted, Fig. 4.6. Measurements are indicated with markers, while the *RC* models are indicated with solid and dotted lines in Fig. 4.6(a) for PEO and PEO:$CsClO_4$, respectively. As with the *n*–Si devices, the capacitance and dielectric constant of PEO without $CsClO_4$ on *p*–Si are constant across more than two decades. The C_P and ε_r of devices with $CsClO_4$ are the same as in PEO devices without $CsClO_4$ at high frequencies. However, at frequencies below ~600 kHz, C_P and ε_r increase with decreasing frequency, as the two-*RC* model also shows, reaching a maximum at 1 kHz of C_P ~0.6 μF/cm^2 and ε_r ~8.0 for PEO:$CsClO_4$ vs. ~0.2 μF/cm^2 and 1.9 for PEO without $CsClO_4$.

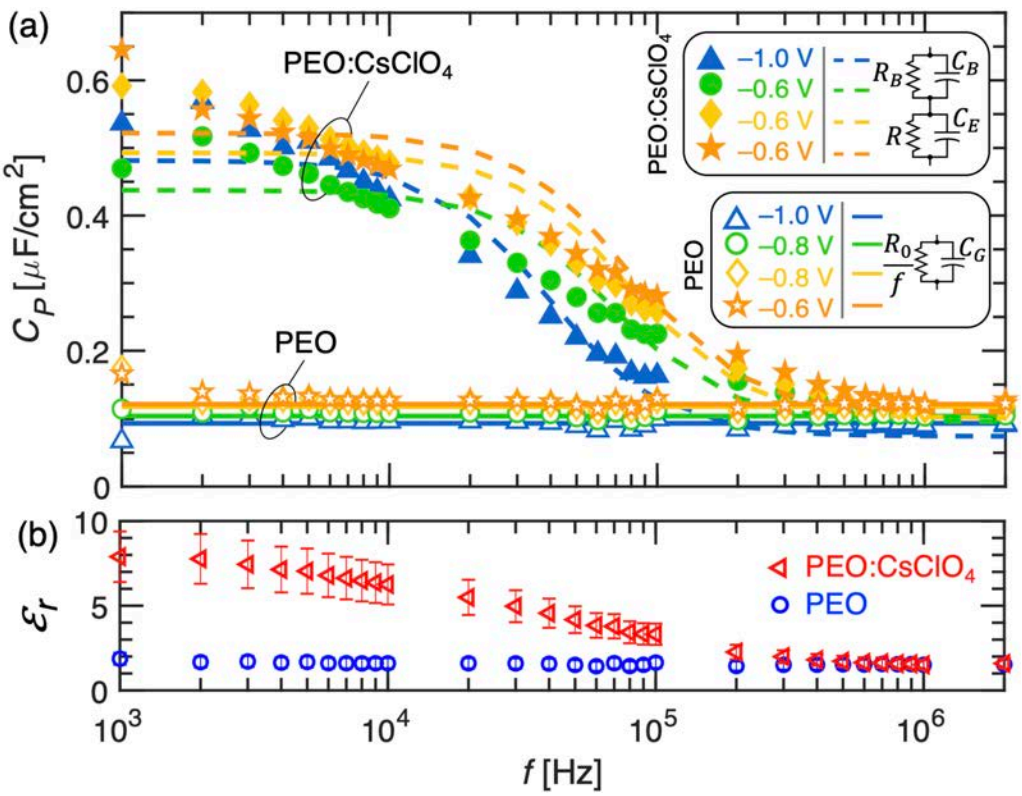

Fig. 4.6 Measured frequency dependence comparing Pd/Ti/PEO:$CsClO_4$/p–Si and Pd/Ti/PEO/p–Si MIS capacitors: (a) parallel capacitance, C_P, and (b) dielectric constant, $\boldsymbol{\varepsilon}_r$, of 63 μm MIS capacitors of various PEO thicknesses biased between –0.6 and –1 V. $\boldsymbol{\varepsilon}_r$ was extracted from a linear fit between the parallel capacitance density and inverse thickness. For reference, in (a) solid and dashed lines indicate the one- and two-RC loop models, for PEO and PEO:$CsClO_4$, respectively as shown in the insets, with parameters plotted in Fig. 4.5.

The frequency dependence of the conductivity of PEO and PEO:$CsClO_4$ capacitors on *p*–Si wafers is shown in Fig. 4.7, where measurements and circuit model fits are indicated in colored markers and solid or dashed lines, respectively. PEO devices without $CsClO_4$ have a conductivity roughly increasing linearly with frequency above 10 kHz. There are some variations in σ due to the closeness of θ_Z to the ideal –90°, as seen in Fig. 4.5(b); that is, the measured real component of the impedance, used to calculate σ, is very small, leading to some variability in the calculation of the real part of the

impedance. The linear σ–f trend measured in PEO without $CsClO_4$, shown in open markers, is reproduced by the one-*RC* equivalent circuit, indicated by solid lines, due to the presence of a frequency dependent resistor, R_0/f.

The measured conductivity of PEO:$CsClO_4$ capacitors, shown in solid markers, is between roughly 1 to 2 orders of magnitude higher than in PEO without $CsClO_4$. The frequency exponent n in the σ–f^n relation changes value at around 100 kHz, below which it is relatively linear and above which σ goes roughly as the square-root of f, as shown in black dashed and dotted lines in Fig. 4.7. These n values are within the limits of 0 and 1 reported in the literature for polymers, with various fractional values representing different ion conduction processes [1].

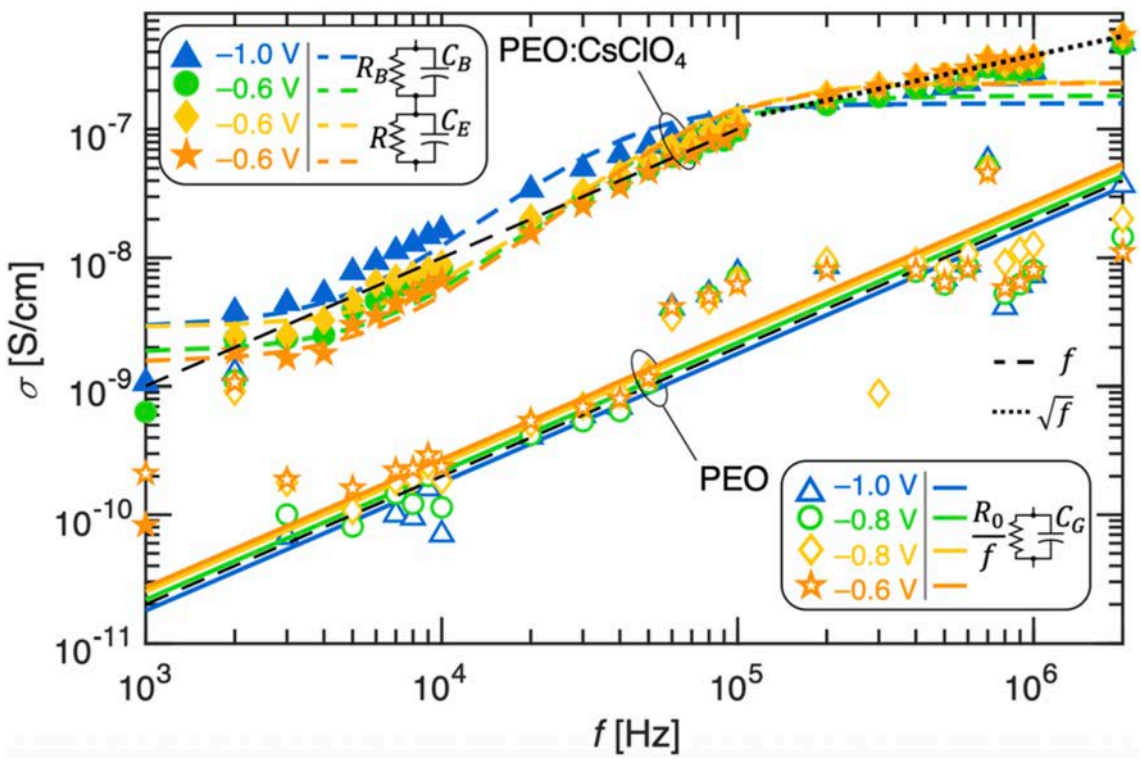

Fig. 4.7 Measured frequency dependence comparing Pd/Ti/PEO:$CsClO_4$/*p*–Si and Pd/Ti/PEO/*p*–Si MIS capacitors: conductivity, σ, of 63 μm MIS capacitors of various PEO thicknesses biased between –0.6 and –1 V. For reference, the one- and two-*RC* loop model, shown in the insets with parameters plotted in Fig. 4.5, are indicated in colored solid and dashed lines for PEO and PEO:$CsClO_4$, respectively. Dashed and dotted black lines indicate a linear and square–root σ–f relation.

The two-*RC* model for PEO:$CsClO_4$ captures the approximate frequency in which n changes values. Its bulk resistor, R_B, is orders of magnitude lower than the frequency-dependent resistor, R_0/f, describing the bulk of PEO without $CsClO_4$. This again shows that the addition of $CsClO_4$ increases the conductivity of the PEO bulk. In these two separate conductivity ranges for PEO and PEO:$CsClO_4$ there may be different ion conduction mechanisms involved, leading to different σ–f^n relations, as can be expected from the additional presence of Cs^+ and ClO_4^- ions, rather than only PEO's background ions, such as OH^- and H^+.

The increase in dielectric constant, Fig. 4.3(d) and Fig. 4.6(b), and the decrease in σ, Fig. 4.2(b) and Fig. 4.7, at low frequencies observed in PEO and to a greater degree in PEO:$CsClO_4$ capacitors has been reported in bulk PEO and other ion-conducting materials, and it is largely attributed to incipient electrode charge polarization effects that strengthen at even lower frequencies [70, 78]. At high frequencies, the conductivity is governed by ion drift in the bulk [77] of the PEO film. With increasing frequency, the conductivity increases approximately linearly and the dielectric constant tends to level off. The low-frequency σ and dielectric constant spectra are related to the accumulation of ions at the PEO/electrode interface, producing space-charge layers across which most of the electric field is dropped, while the PEO bulk experiences a much lower electric field. This causes the dielectric constant to increase and σ to drop with decreasing frequency, at least until reaching a σ plateau due to the partially, rather than fully, blocking nature of the electrodes [77].

4.5 Conclusion

The impedance frequency properties of PEO and PEO:$CsClO_4$ have been characterized at thicknesses from 6 to 19 nm, thinner than prior reports. The properties of PEO without $CsClO_4$ are well described by an oxide that has a band gap of approximately 4.5 eV, metal-PEO barrier of 2.2 eV, and PEO/Si band offset of 1.2 eV. From the *C–V* hysteresis of PEO capacitors without $CsClO_4$ and assuming its main contributions are electronic, the trap density is estimated to exceed approximately $2.6\times10^{11}/cm^2$. The extracted static dielectric constant of PEO without $CsClO_4$ in ultrathin films is ~1.6. Adding $CsClO_4$ increases the parallel capacitance and dielectric constant for frequencies

below 500 kHz, due to the polarization of ions at the interface of PEO with the electrodes. Adding $CsClO_4$ also increases the conductivity of the films across the full frequency range. Both PEO and PEO:$CsClO_4$ capacitors had a roughly linear frequency dependence, with the latter transitioning to a square-root conductivity-frequency dependence at ~100 kHz.

Simple equivalent circuit models capture the overall impedance vs. frequency trends. For PEO without $CsClO_4$, a single *RC* loop represents the ion transport in the bulk of the film, with the resistor having a simple inverse-frequency dependence. When $CsClO_4$ is present, the charge transfer resistance and an electrode polarization capacitance is sufficient to explain the measured response. The addition of $CsClO_4$ reduces the bulk resistance by orders of magnitude compared to PEO without $CsClO_4$. Ultrathin PEO films at the decananometer scale are shown here to be insulating and to exhibit impedance-frequency behavior similar to thicker films even at the micron scale. No impediments are found to using PEO:$CsClO_4$ at scales commensurate with VLSI technology for deep learning and neuromorphic applications.

CHAPTER 5:

DYNAMIC RESPONSE OF MIM CAPACITORS WITH DROPCASTED AND SPIN-COATED PEO AND PEO:$CSCLO_4$

5.1 Introduction

In this chapter, the Multiphysics capacitor model introduced in Chapter 2 is used to simulate the ionic response of PEO:$CsClO_4$ to a voltage step and to a train of triangular voltage pulses. This is then compared with measurements of MIM capacitors, where the insulator is ultrathin PEO:$CsClO_4$. The measurement are shown to have a response in reasonable agreement with the simulations at biases in which the electronic currents (leakage and trap-filling) are negligible. The fabricated devices were further analyzed by TEM and contrasted with impedance-frequency measurements to enable comparison with our prior studies and the work of others.

5.2 Simulated triangular-bias response

A Multiphysics capacitor model with PEO thickness of 10 nm and parameters listed in Table 2.1 was used to simulate the dynamic response of PEO:$CsClO_4$ to a ±1 V triangular pulse train of various slew rates, for comparison with experiments. A sufficiently low slew rates (e.g. 4 kV/s) the EDLs charge and discharge in response to the applied electric field. High slew rates (e.g. 4 MV/s) lead to short times for EDL charging and significant displacement currents. In the Multiphysics model only the ionic and displacement currents are computed. No electronic current transport mechanism is included in the simulation.

Shown in Fig. 5.1 is the current density J (left y-axis) produced by an input voltage V_{IN} (right y-axis) with a decreasing slew rate, from 4 MV/s in (a) to 4 kV/s in (d). The current scales by three orders of magnitude across these plots. In the 4 MV/s – 400 kV/s range, Figs. 5.2(a-b), the displacement current is much larger than the ionic current and the current magnitude changes in direct proportion to the slew rate. The capacitance density, estimated from $C = J/(dV/dt)$, is approximately 0.13 μF/cm^2 in Fig. 5.2(a); this corresponds to a dielectric with relative permittivity of 1.5 and thickness of 10 nm, as expected from the geometry. As the slew rate decreases to 40 and 4 kV/s, Fig. 5.2(c-d), the displacement current becomes small relative to the ion current. As the displacement current diminishes, the ionic current component is revealed.

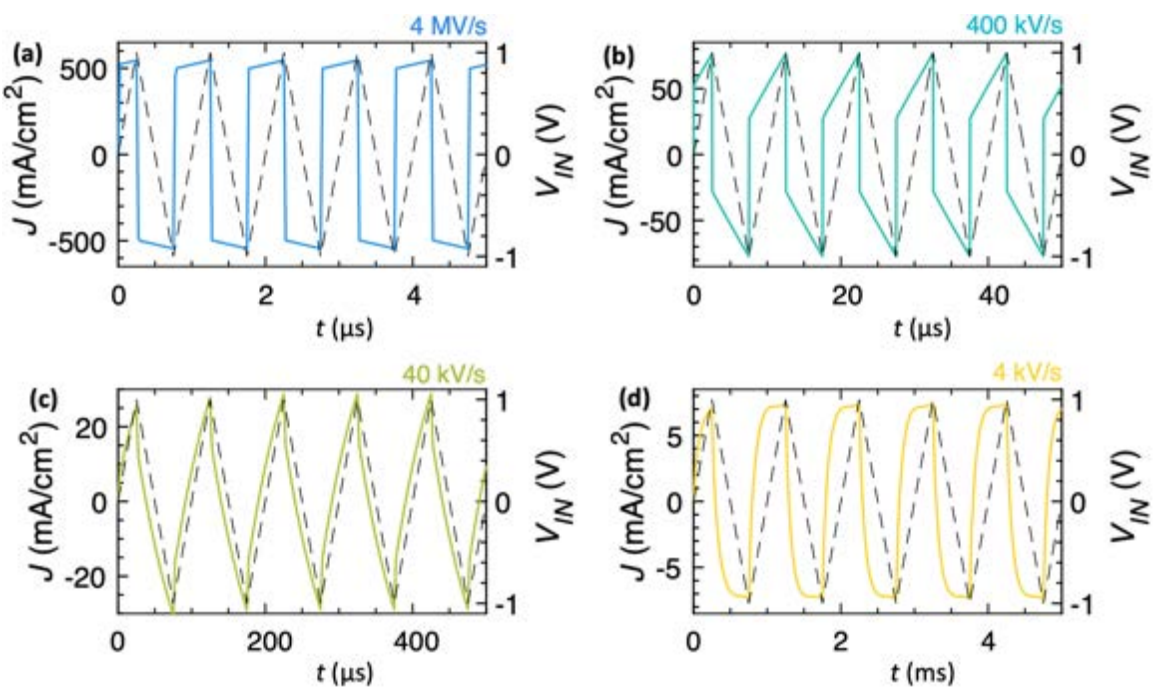

Fig. 5.1 Current density J (left y-axis) and input voltage V_{IN} (right y-axis) vs. time t for 5 cycles of a triangular-waveform bias with various slew rates: (a) 4 MV/s, (b) 400 kV/s, (c) 40 kV/s, and (d) 4 kV/s.

To quantify the amount of charge accumulated at the EDL with each slew rate, the simulated current density was integrated over time. Plotted in Fig. 5.2 are the last 4 cycles of (a) the current density and (b) the polarization charge density vs. input voltage. Fig. 5.2(a) shows the 78× decrease in peak current, from ~546 mA/cm^2 at 4 MV/s down to ~7 mA/cm^2 at 4 kV/s. As the slew rate decreased, the polarization charge increased, Fig. 5.2(b), since it extends the amount of time under a given voltage polarity for ions to drift toward the EDLs to charge them.

The location of the polarization-charge peak is dependent on sweep rate. At the higher slew rates, where the displacement-current component dominates, the apparent polarization is maximum at the peak voltage. This represents the charge density due to the geometrical capacitance (as the ions do not move quickly enough to polarize the surface). In contrast, when the displacement current becomes comparable to the polarization current, the absolute maximum polarization charge density occurs after the peak voltage has been reached and the slew rate has changed sign. This delay, seen in the inset of Fig. 5.2(b), occurs because of the relatively slow ionic response under an electric field that retains the same direction and thus continues to support ionic flow toward the EDLs, thereby producing a maximum polarity at lower than maximum input bias.

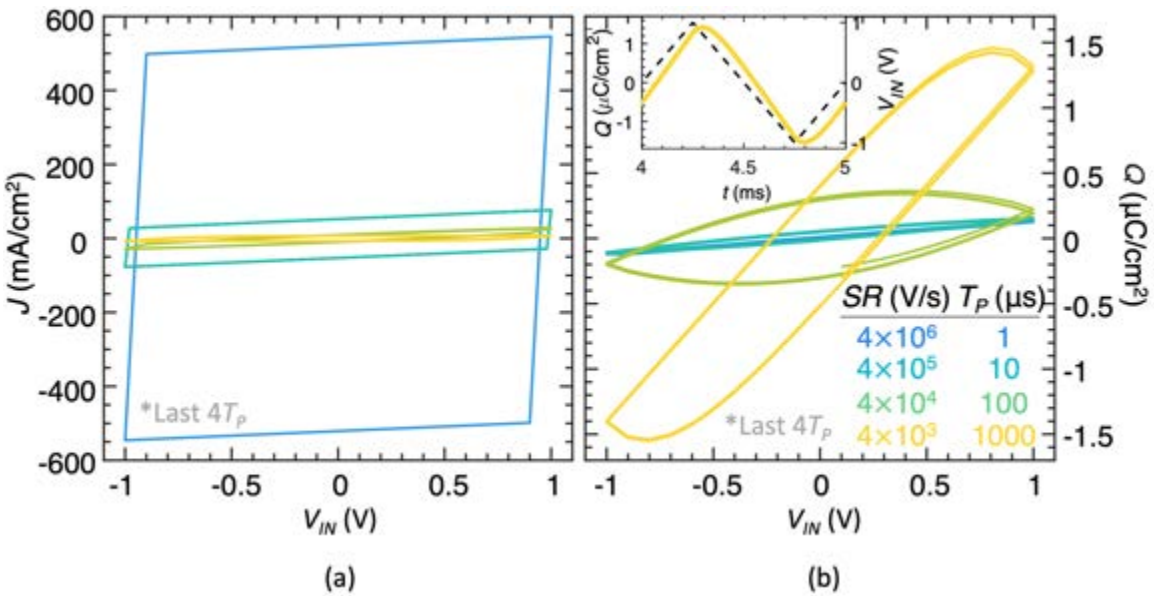

Fig. 5.2 Current (a) and polarization charge density (b) vs. input voltage for a triangular waveform reaching a maximum of 1 V at various slew rates. The polarization loops cycle in the counterclockwise direction. The inset in (b) shows the polarization (solid line) and input voltage (dashed line) during the last cycle of the 4 kV/s triangular wave.

5.3 Experiments to validate modeling

To assess whether the Multiphysics model captures the dynamic behavior of experimental capacitors with nm-thick PEO, MIMs with spin coated PEO and PEO:$CsClO_4$ were fabricated for subsequent electrical characterization. In the Notre Dame Nanofabrication Facility, 2 × 2 cm^2 *p*–type Si (100) wafers with a resistivity of 0.01 – 0.02 Ω-cm were MOS-cleaned and HF-dipped (50:1 DI:HF, 5 s), followed by an electron-beam evaporation of the bottom electrode. The later consisted of two noble metals, 135 nm Au, followed by 50 nm Pt, chosen in order to minimize the likelihood of electrochemical reactions between the metal and the electrolyte. Finally, a ~2 nm Ti layer was evaporated as an adhesion layer for PEO. This is meant to help increase the interaction of PEO with the substrate, which is known to result in a lower crystallization

rate, as well as in a type of polymer-chain folding known as flat-on lamellae [79], resulting in more continuous films compared to the edge-on lamellae [80] that occur when there is little to no interaction with the substrate [81].

Inside an Ar glovebox (99.999% Ar, H_2O <0.1 ppm, O_2 <0.1 ppm), PEO and PEO:$CsClO_4$ solutions were prepared, as detailed in Chapter 3 and 4, and spin coated on the bottom electrodes at either 1 or 8 krpm. The wafers were then baked at 50 °C for 10 minutes to evaporate the solvent. Finally, top electrodes were formed by electron-beam evaporation through a shadow mask of the same metals in the bottom electrode but in inverted order: ~1 nm Ti, followed by 8 nm Pt and 125 nm Au. A schematic of the MIM stack is shown in Fig. 5.3(a). The top electrodes where 20, 45, and 63 μm in the spin-coated wafers in order to have capacitor area steps of 1×, 5×, and 10×. When not under test, the wafers were stored in the Ar glovebox to minimize moisture absorption.

TEM cross-sections of a 20 μm MIM with PEO:$CsClO_4$ spin coated at 8 krpm are shown in Fig. 5.3(a-b). The top electrode had an irregular profile, which together with the roughness of the top electrode resulted in a PEO film with greater thickness variations than that seen in previous chapters, Fig. 3.3, Fig. 3.4(a), and Fig. 4.1(a), in which smoother bottom substrates where used. Despite this greater thickness variation, the electrical characterization shows that these MIM capacitors are well behaved, with many similarities with their previously-studied MIS counterparts (chapter 4).

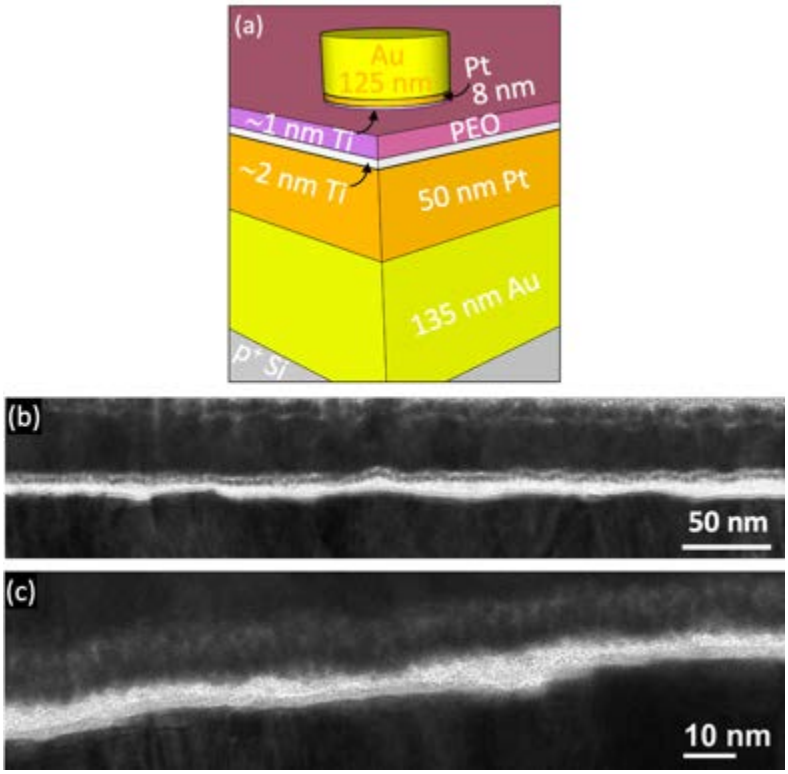

Fig. 5.3 MIM (Au/Pt/Ti/PEO/Ti/Pt/Au/*p*-Si) capacitor with ultrathin PEO:$CsClO_4$. (a) Stack schematic. (b) HRTEM image of the cross-section of a 20-μm diameter capacitor with PEO:$CsClO_4$ spin-coated at 8 krpm.

5.3.1 Dynamic response of MIMs to triangular voltage pulses

The behavior of the Multiphysics model for a 10 nm PEO:$CsClO_4$ capacitor is compared next with experimental MIMs with PEO and PEO:$CsClO_4$ spin-coated at 1 krpm. Fig. 5.4(a) shows the simulated and measured current density in solid blue and dotted green lines, respectively, in response to a ±0.7 V, 10 kV/s pulse train, indicated by a dashed black line. The resulting polarization charge is shown in Fig. 5.4(b). A low maximum applied voltage (±1 V on MIMs with 1 krpm PEO) was chosen in order to stay well away from voltages that could induce electrochemical reactions at the electrodes.

In the absence of Cs^+ and ClO_4^- ions (dark-green, dotted line), the total current density is expected to be near the displacement current density, given by the product of the geometric capacitance density and the slew rate, which for a capacitor with the permittivity of PEO, 10-nm thickness and 20 μm in diameter is ~1.3 mA/cm^2. The measured current density for the PEO MIM was approximately 2× higher, ~3 mA/cm^2, which is in reasonable agreement with expectation, given the uncertainties in layer thickness, area, and ion diffusivities. As for PEO:$CsClO_4$, the simulated current density had a maximum of ~12 mA/cm^2, while the experimental peak current was approximately 2× higher, ~ 22 mA/cm^2.

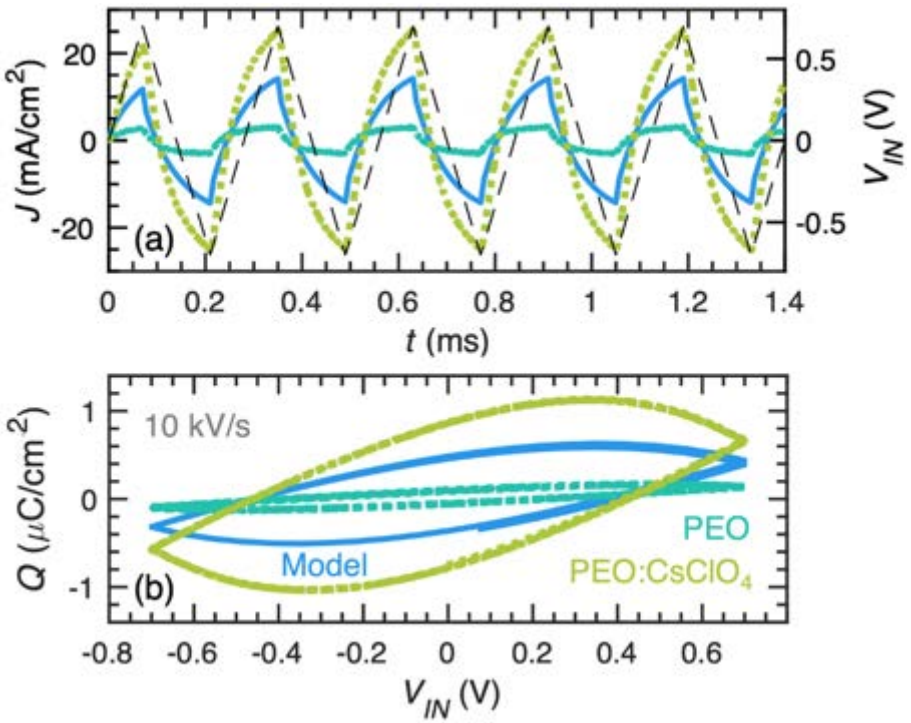

Fig. 5.4 Comparison of the (a) current density and (b) polarization charge density of a PEO:$CsClO_4$ capacitor modeled in COMSOL Multiphysics (solid blue line) vs. experimental (dotted green line) 20-μm capacitors with PEO (dark green line) and PEO:$CsClO_4$ (light green line) spin-coated at 1 krpm and biased with ±0.7 V, 10 kV/s triangular pulses (dashed black line).

The polarization charge density of the last 4 cycles is shown in Fig. 5.4(b). The PEO-only capacitor (dark green) had a maximum polarization charge density of $Q \sim 0.16\ \mu C/cm^2$. This non-zero polarization despite lacking $CsClO_4$ reflects the presence of a residual background ion density in PEO, some of which could be H^+ and OH^- from any absorbed air moisture. The PEO:$CsClO_4$ capacitor (light green) had a higher maximum polarization charge density of ~1.1 $\mu C/cm^2$, which is close to the ~0.6 $\mu C/cm^2$ observed in the COMSOL model (blue). This polarization increase with respect to pure-PEO capacitors reflects the additional presence of the large number of Cs^+ and ClO_4^- ions contributing to charge the EDLs. Overall, the Multiphysics simulations capture the transport and transient response of the measured films.

The impact of the slew rate on the polarization charge accumulated at the electrodes is examined next and compared with the trends seen in the Multiphysics model. Fig. 5.5 shows the (a) current density and (b) polarization charge density vs. input voltage of an MIM capacitor with 1-krpm PEO:$CsClO_4$, as indicated by the schematic in (b). The applied bias was 5 cycles of a ±1 V triangular pulse train with slew rate varied from 800 V/s to 100 kV/s. Again, a decreasing slew rate resulted in a lower current density and a larger polarization charge density, as expected, reaching up to ~6.4 $\mu C/cm^2$ at 800 V/s. The maximum charge accumulated with a 5 kV/s slew rate is in the same order of magnitude as the value yielded by the simulated triangular waveform with a 4 kV/s slew rate, Fig. 5.2, again showing the agreement between the Multiphysics model and the experiments.

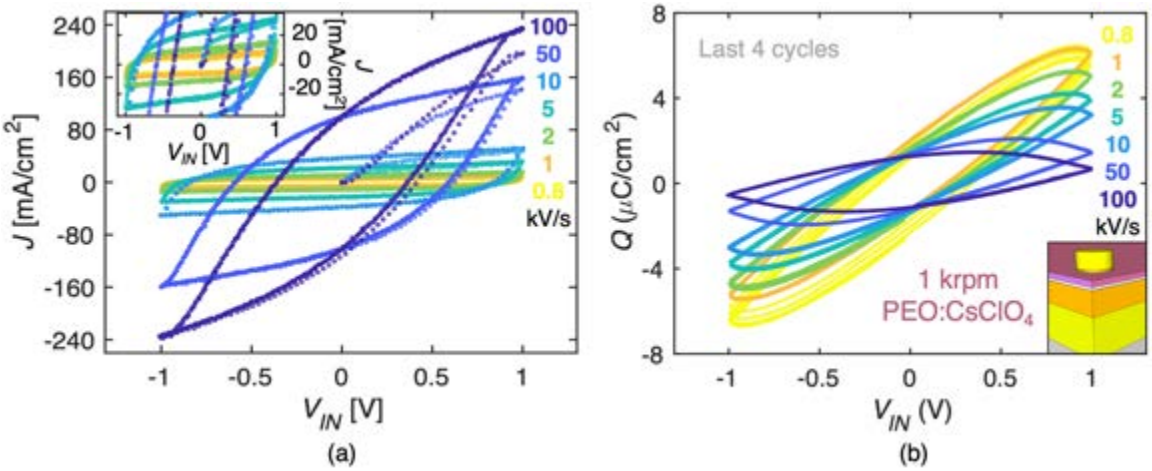

Fig. 5.5 Dependence of the measured (a) current density and (b) polarization charge on the input-voltage sweep rate in an experimental Au/Pt/Ti/PEO:$CsClO_4$ /Ti/Pt/Au/*p*-Si capacitor with 1-krpm PEO:$CsClO_4$. The inset in (a) is a zoom-in across the y-axis.

5.3.2 Dynamic response to a large applied electric field

Having previously restricted the magnitude of the applied voltage to minimize leakage current, next we show the effects of leakage current as biases are increased. Leakage current is not included in the Multiphysics model we have been using. Fig. 5.6(a) shows the current density (left y-axis; colored solid lines) in response to 5 cycles of a ±1 V, 750 V/s triangular waveform (right-axis; dashed black lines) applied to an MIM with 8-krpm PEO:$CsClO_4$. Different colors mark three consecutive repetitions of this 5-cycle test. Unlike the symmetric current density loops observed previously (e.g. the response of the 1-krpm MIM to a ±1 V, 800 V/s bias, Fig. 5.5), here the same ±1 V is applied across the thinner 8-krpm MIM result in a higher electric field, large enough to produce an asymmetric current. The current density vs. voltage loops in Fig. 5.6(b) show the marked increase in current above around +0.6 V. Within this range, a leakage component is added to the total current, which could be due to electronic transport across

the PEO film and/or charge trapping. When the current density is integrated over time across each of the 5 cycles, Fig. 5.6(c), the resulting polarization charge density no longer forms overlapping loops as in Fig. 5.5(b), but instead increases with every additional period in an upward spiral. Nonetheless, the current-density overlap of the three repetitions highlights the repeatability of the measurements, despite the higher electric field, suggesting it is not large enough to cause an electrochemical reaction that would irreversibly modify the device behavior.

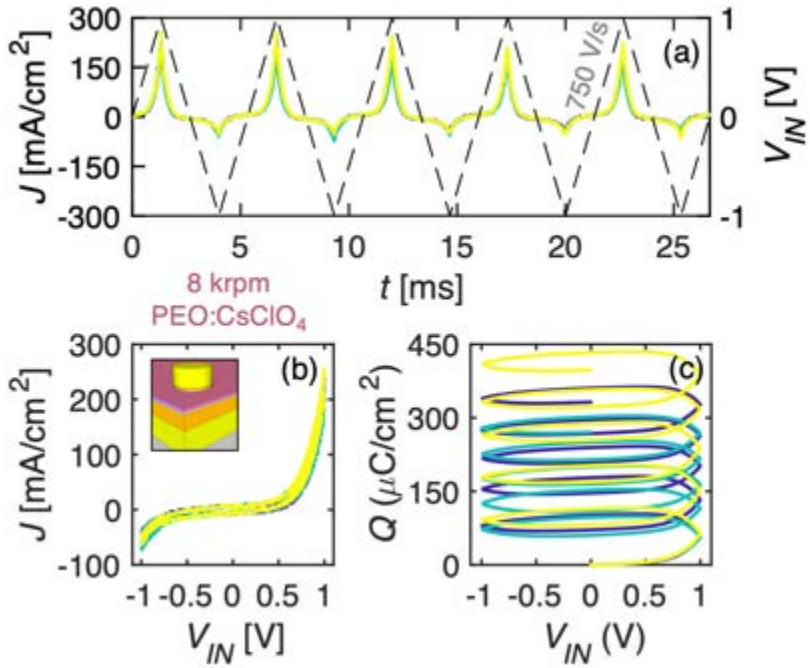

Fig. 5.6 Repeatability of the time evolution of the (a) current density (left y-axis; colored solid lines) of a Au/Pt/Ti/PEO:$CsClO_4$ /Ti/Pt/Au/*p*-Si capacitor with 8-krpm PEO:$CsClO_4$, in response to 5 cycles of a ±1 V, 750 V/s triangular pulse train (right y-axis; dashed black line). The colors indicate three subsequent repetitions. (b) Current density and (c) polarization charge density vs. input voltage for the three repetitions.

This current asymmetry is less pronounced at higher slew rates, as the *J-V* loops in Fig. 5.7(a) show, and is almost absent at 100 kV/s (yellow). This results in a *Q-V* loop, Fig. 5.7(b), that overlaps with itself across cycles, as shown in the zoom-in in the inset of Fig. 5.7(b). As the slew rate decreases, the asymmetry becomes more accentuated, likely because the mechanism behind it has sufficient and greater time to transport electronic charge and/or accumulate charge in the film. Since there is a slightly larger positive than negative current, the maximum polarization charge density is positive and increases with each cycle.

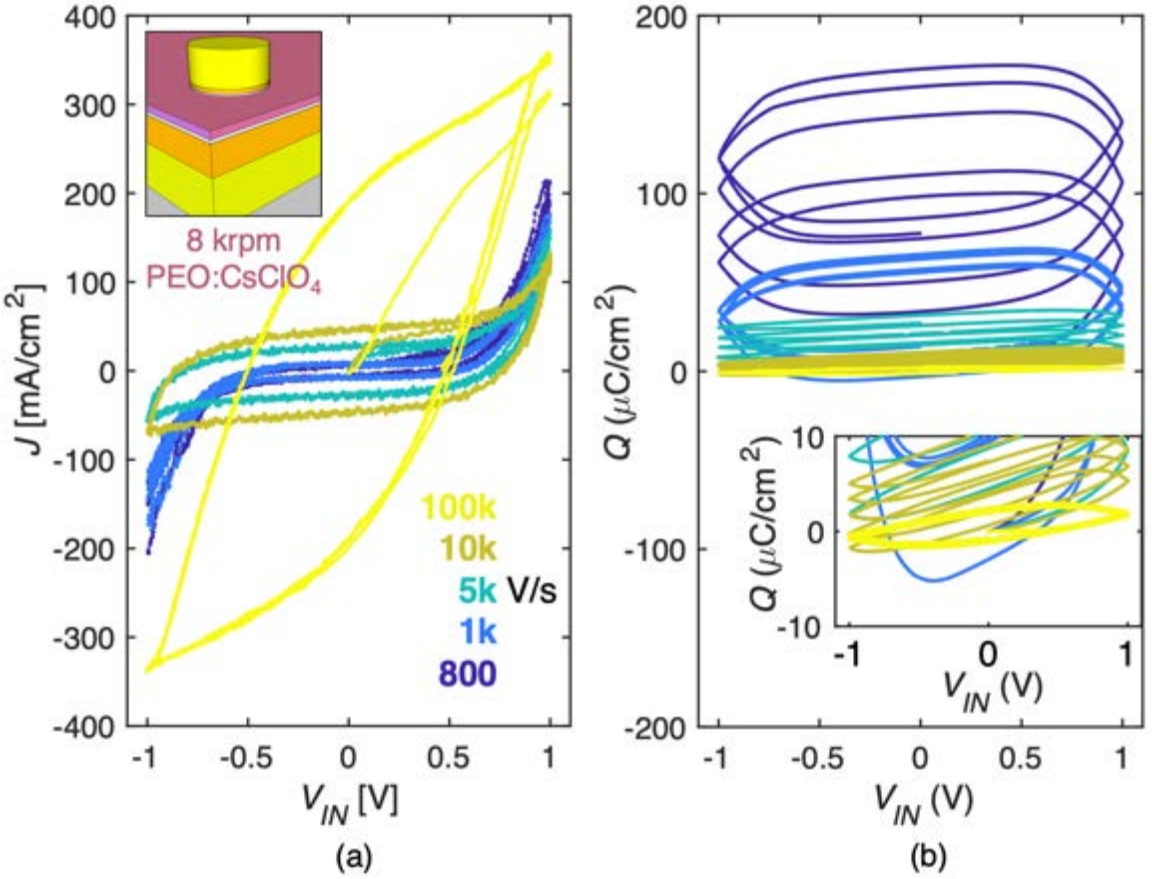

Fig. 5.7 (a) Current density and (b) polarization charge density vs. input voltage of an Au/Pt/Ti/PEO:$CsClO_4$ /Ti/Pt/Au/*p*-Si capacitor with 8-krpm PEO:$CsClO_4$, shown schematically in the inset of (a), in response to 5 cycles of a ±1 V triangular pulse train with slew rate between 800 and 100k V/s.

5.3.3 Dynamic response of MIMs to a voltage step

The step response of simulated and experimental 1-krpm PEO:$CsClO_4$ MIMs is observed next. Fig. 5.8(a-c) show the current-density and polarization-charge response to a voltage step of increasing magnitude, from 0.1 to 0.4 V, reached at a rate of 1 kV/s. The current density is seen to increase in magnitude during both the ramp up and the ramp down to zero. The measured currents and polarization charges (dotted lines) are within the same order of magnitude as the ones predicted by the Multiphysics simulations (solid lines). However, during the ramp, the simulated current density saturates but the measured current density continues to increase, which could suggest some current leakage through the PEO film. As soon as the voltage becomes constant, the current begins to decay. The polarization charge density increased with higher voltages, as expected. However, in the simulations the polarization charge saturated at a maximum value around 1 ms after reaching the plateau of the voltage step, while the measured polarization charge continued to increase throughout the plateau.

The dependence of the current and polarization-charge response on a 0.4-V step's slew rate, which was varied between 1, 2, and 4 kV/s, is shown in Fig. 5.8(c-e) for both simulated (solid lines) and measured (dotted) capacitors. The current density increased with slew rate, as expected from the larger displacement current component, which is proportional to dV/dt. Given that this step series had the same voltage amplitude, the polarization charge density reached approximately the same value after around 500 μs in the simulations and ~800 μs in the measurements. However, the simulated value eventually saturated, while the measured charge density continued to increase during the step plateau. In addition, the maximum polarization charge was achieved faster using the

higher slew rate, corresponding to the greater amount of time spent at the maximum voltage. The results in Fig. 5.8 also suggest there is no non-volatility in these ultrathin capacitive structures, given that the charge and discharge times are the same.

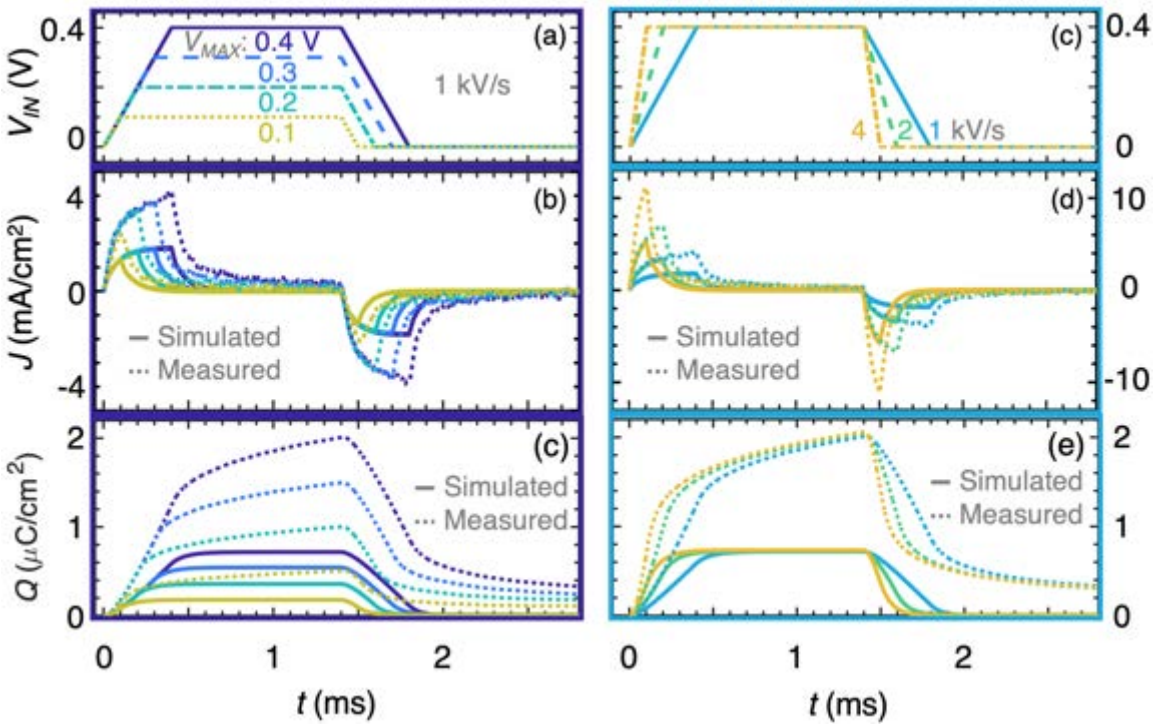

Fig. 5.8 Current-density and polarization-charge response of a simulated (t_{PEO} = 10 nm, ε_{PEO} = 1.5, 25 μs time step) and experimental (1 krpm) Au/Pt/Ti/ PEO:$CsClO_4$ /Ti/Pt/Au/*p*-Si capacitor to a voltage pulse of varying amplitude (a-c) or slew rate (c-e). The applied voltage step, current density, and polarization charge can be seen in the top, middle, and bottom panels, respectively. The simulated and measured current density and polarization charge are indicated in solid and dotted lines, respectively.

5.4 Frequency dependence of the impedance of MIM capacitors

The frequency dependence of the impedance of spin-coated MIM capacitors of various areas and thicknesses is examined next. Fig. 5.9 indicates with markers the *Z-f* of three sizes of MIMs with 8 krpm PEO (a-b) and PEO:$CsClO_4$ (c-d). The three capacitor areas, defined using a shadow mask with 20, 45, and 63 μm discs, resulted in slightly

larger top electrodes, on average 36, 57, and 71 μm in diameter, respectively, according to optical-microscopy measurements from a previous fabrication. The colored lines in (a) and (c) indicate the impedance magnitude of an ideal capacitor with the dielectric constant of PEO, ε_{PEO} = 1.5, thickness of 4, 6, or 8 nm, and diameter of 36, 57, or 71 μm. The *Z-f* of PEO MIMs in Fig. 5.9(a-b) reflects a capacitive behavior. The impedance magnitude decreases with frequency at almost the rate of an ideal capacitor, while the impedance phase remains around –90°. The impedance magnitude decreases with area, as expected from its inverse relation to the area of a parallel-plate capacitor. The three capacitors have an impedance magnitude matching that of an ideal capacitor between 4 and 8 nm thick PEO, suggesting their effective thickness variation is somewhere within this range.

The *Z-f* of PEO:$CsClO_4$ MIMs, Fig. 5.9(c-d), departs from this ideality, with a decreasing $|Z|$ at lower frequencies and a minimum impedance phase at around 200 kHz. This behavior is expected, given that the EDL with Cs^+ and ClO_4^- has a higher charge density for a given voltage, i.e. a larger capacitance, especially at lower frequencies, in which ions have enough time to drift and charge the EDLs, thereby resulting in a lower impedance than in PEO without added ions.

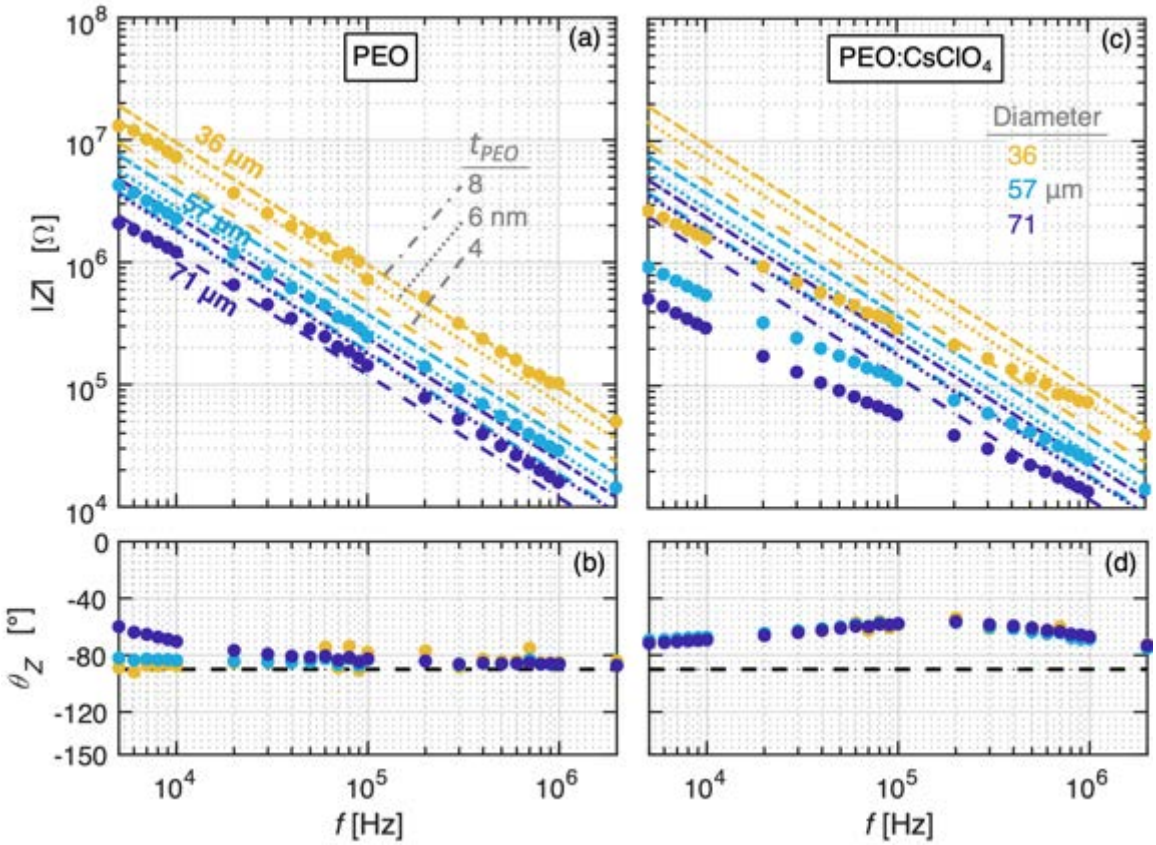

Fig. 5.9 Frequency dependence of the impedance magnitude (top panels) and phase (bottom panels) of MIM capacitors with 8 krpm PEO (a-b) and PEO:$CsClO_4$ (c-d) with top electrodes 36, 57, and 71 µm in diameter biased at V_{IN} = 0 V. Markers indicate measurements while coloroed lines in (a) and (c) show the |*Z*| of an ideal capacitor with ε_{PEO} = 1.5, 4, 6, and 8 nm PEO thickness, and diameter of 36, 57, and 71 µm.

Shown in Fig. 5.10 is the frequency dependance of the impedance of 20 µm MIM capacitors with PEO, Fig. 5.10(a-b), and PEO:$CsClO_4$, Fig. 5.10(c-d) spin-coated at 1 and 8 krpm. Different markers indicate distinct capacitors. Colored reference lines mark the impedance magnitude of an ideal capacitor with ε_{PEO} = 1.5, diameter of 36 µm, and thicknesses from 5 to 45 nm. As Fig. 5.10(a-b) show, the PEO MIMs had in general a behavior following the trends of an ideal PEO capacitor, with |*Z*| decreasing with higher spin-speed, as expected, and an impedance phase of around –90°.

Again, the *Z-f* of PEO:$CsClO_4$ MIMs, Fig. 5.10(c-d), depart from this ideality, with the effect in the impedance magnitude being more pronounced in the thicker, 1 krpm films. This may be the result of the lower resistance across the shorter bulk of the thinner film, leading to an impedance more dominated by the capacitive, rather than resistive, component.

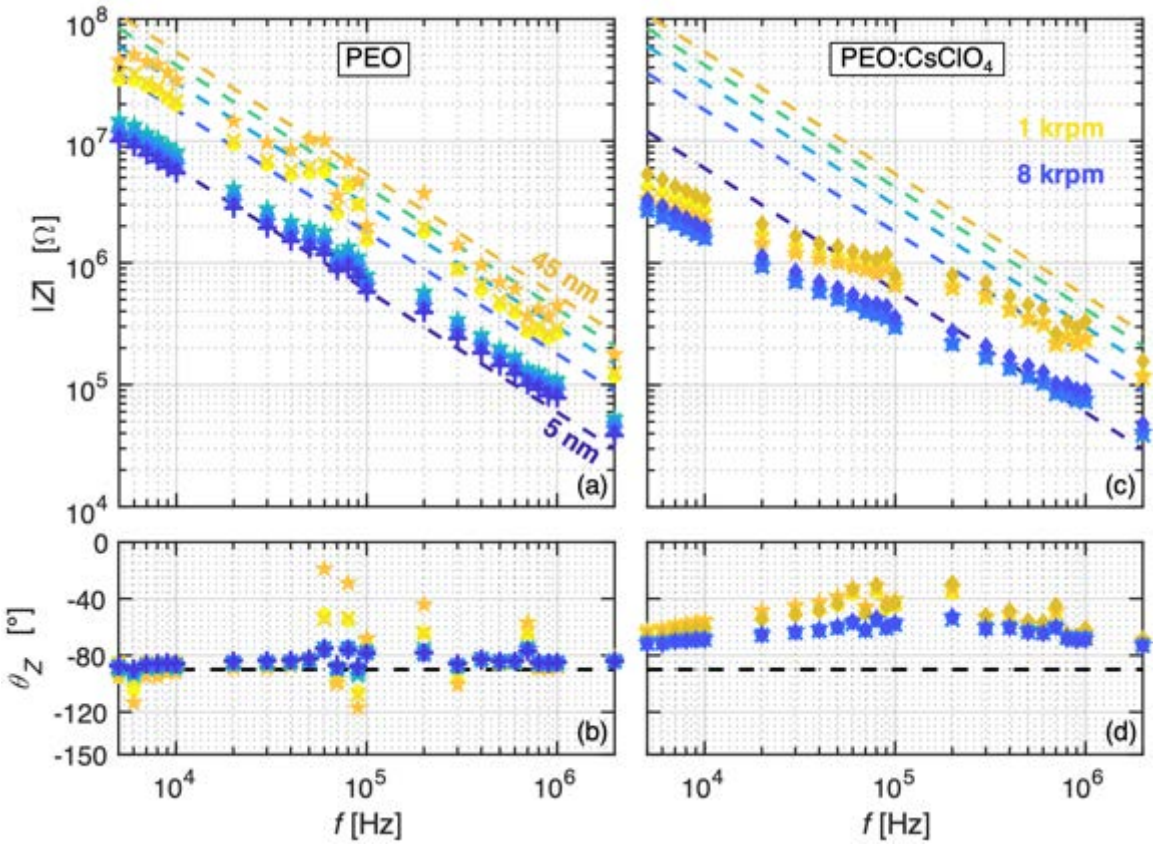

Fig. 5.10 Frequency dependence of the impedance magnitude (top panels) and phase (bottom panels) of 20-μm MIM capacitors with PEO (a-b) and PEO:$CsClO_4$ (c-d) biased at V_{IN} = 0 V. The polymer solutions were spin-coated at either 1 or 8 krpm, as indicated by yellow, green, and blue markers, respectively. For a given spin speed, different markers indicate distinct capacitors. For reference, dashed colored lines in (a) and (c) mark the ideal |Z| for $_{PEO}$ = 1.5, 36 μm diameter, and t_{PEO}: 5, 15, 25, 35, and 45 nm.

These measurements match the trends observed in MIS capacitors in the previous chapter, Fig. 4.5(a-b). One difference is that MIMs without added ions appear to have a lower electrical thickness than their MIS counterparts spin coated at the same speed. For example, 8-krpm MIMs without ions have an impedance close to an ideal PEO capacitor of only ~5 nm, rather than the ~11 nm of MIS capacitors with PEO spin coated at 8 krpm, likely as a result of a lower electrical thickness, Fig. 5.1(d), than their more uniform MIS counterparts, Fig. 4.1(a).

5.5 Dynamic behavior of thick MIMs

The response to a triangular bias was also measured in MIMs with thicker, dropcasted PEO:$CsClO_4$, as reported in [76], in order to observe the charge density achieved by various voltage amplitudes or slew rates. Fig. 5.11 shows the experimental current density and polarization charge density in response to a bias consisting of 5 cycles of a triangular waveform of amplitude between ± 0.4 and 2.8 V, Fig. 5.11(a-b), or slew rate between 0.8 and 100 kV/s, Fig. 5.11(c-d). Because a dropcasted film is much thicker (~1 μm) than a spin-coated one, the resulting electric field at 2.8 V is two orders of magnitude lower than the ~ 1 MV/cm a 10-nm film would experience. Thus, the current density, Fig. 5.11(a), is symmetric and does not exhibit a sudden increase near the voltage peaks like the spin-coated films do when under a 1-V bias, Fig. 5.6(a-b) and Fig. 5.7(a), as expected given the much lower electric field.

At 0.8 kV/s, higher voltage amplitudes resulted in a larger maximum polarization charge density, Fig. 5.11(b), as expected from the higher electric fields driving the ions to charge the EDLs. A higher voltage amplitude also increased the voltage at which the

maximum polarization charge was registered, which continues to increase even after a change in sign in the slope of the triangular waveform, due to the slower ionic drift compared to the bias. Increasing the slew rate decreased the maximum charge polarization, Fig. 5.11(d), as expected and measured in the thinner MIMs, suggesting no major differences in the behavior of micron- and nanometer-thick films.

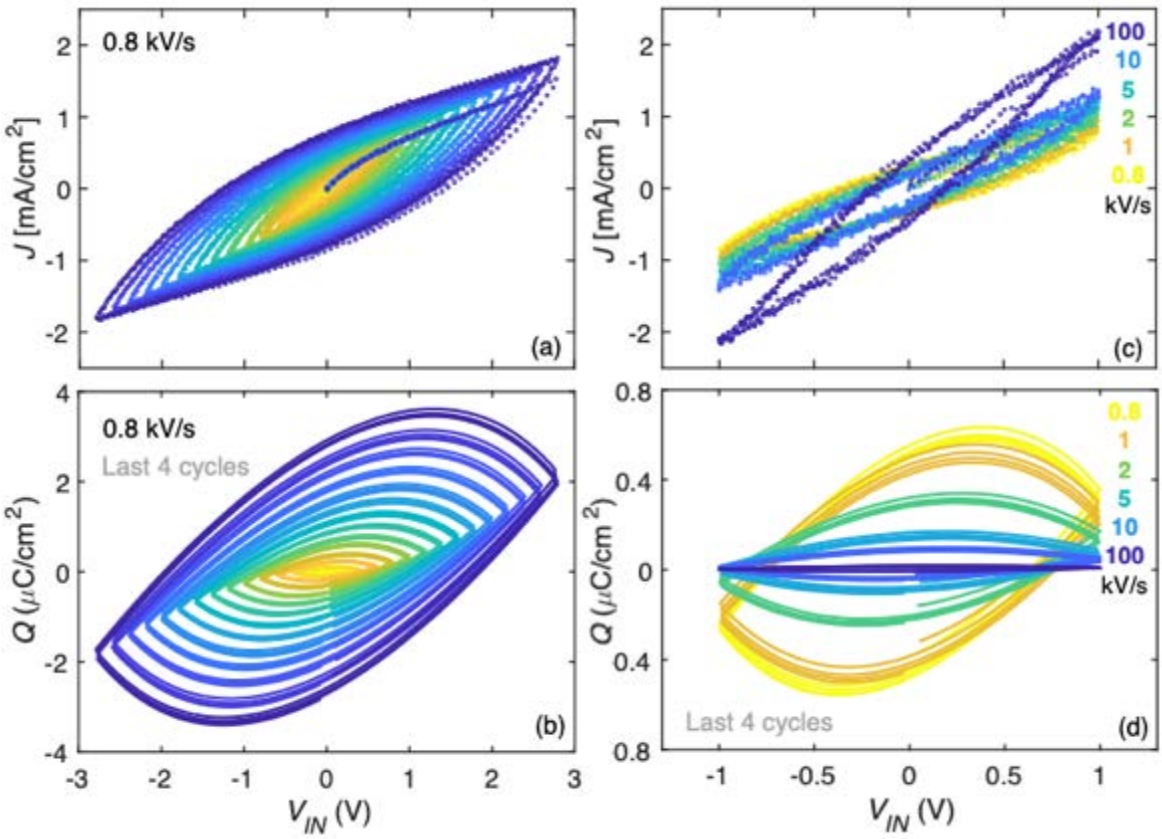

Fig. 5.11 Current density (top panels) and polarization charge (bottom panels) of experimental MIM capacitors with dropcasted (~1 μm) PEO:$CsClO_4$ under 5 cycles of a triangular bias of different amplitudes (a-b) or slew rates (c-d).

5.6 Conclusions

The comparison of the experimental and simulated triangle and step responses at 500 Hz speeds, using voltages well below the electrochemical limit of V/nm, shows that the measured transient response of ultrathin PEO:$CsClO_4$ MIMs is fairly well represented by the Multiphysics simulations of the ionic response. However, under a larger electric field, the 8-krpm MIMs were driven further from equilibrium, revealing current asymmetries that may be due to electronic transport and/or charge trapping within the film. Further studies could reveal the electric fields needed to observe electronic transitions where perhaps new interface phenomena are revealed. In all PEO:$CsClO_4$ MIMs observed, higher bias frequencies decreased the amount of charge available per cycle to strengthen the EDL. Higher voltages and shorter pulse times could be explored in future work to see whether there are fast reversible and nonvolatile interactions at the electrode surfaces that could be used for memory and neuromorphic computing.

CHAPTER 6:

CONCLUSIONS AND FUTURE WORK

Motivated by an interest in increasing the charging speed of the EDL to a range relevant to electronics, this dissertation has studied a solid polymer electrolyte consisting of the organic dielectric PEO and a dissolved salt, $CsClO_4$, as it behaves when confined in one dimension. Decananometer-thick films of PEO and PEO:$CsClO_4$ in MIS and MIM capacitor structures were physically characterized with TEM and EELS, in order to understand how the film coats nanometric structures such as individual CNTs for potential integration with CNT logic. These ultrathin films were also electrically characterized and simulated in COMSOL Multiphysics to better understand their static and dynamic response to an applied electric field. It is known that confinement can potentially alter a polymer's bulk properties, including its degree of crystallization and therefore, its conductivity [40]. PEO's crystallinity decreases at thicknesses below ~200 nm [41]. This higher percentage of amorphous regions in which ions can move may increase the speed of the ion response compared to the bulk. In addition, thinning the SPE increases the electric field produced by a fixed input voltage, or conversely, it lowers the voltage necessary to achieve a desired electric field. While PEG and PEO have been spin coated down to ~10 nm, to the best of our knowledge, PEO with an added salt such as $CsClO_4$ had previously only been drop casted; it is known that $LiClO_4$, for instance, alters the structure, mobility, and conductivity of PEO-based SPEs in various degrees depending on the salt concentration [56].

This dissertation has shown that PEO and PEO:$CsClO_4$ can form continuous nanometer-thick films after spin coating their polymer solutions onto various surfaces, including semiconductors, such as Si and CNTs-on-quartz, Ti, and noble metals such as Pd and Pt. It is known that the degree of interaction of the polymer chains with functional groups on a particular surface can alter how the polymer chains orient themselves as the film crystallizes [79]. The wrong orientation could result in discontinuous films after crystallization. However, the physical and electrical characterization in this work show that the films are continuous across at least several micrometers, resulting in a nearly ideal capacitive behavior of PEO, with electrode polarization effects emerging in PEO:$CsClO_4$ films with decreasing frequency.

TEM and EELS imaging have also shown that spin coating is a deposition method that can produce PEO:$CsClO_4$ films that, despite being only a few nanometers thick, can still completely coat nanometric structures on the substrate surface, such as individual CNTs, without any visible gaps or interlayers between the polymer and the nanostructure, as desired for EDL formation at the SPE/CNT interface. These PEO:$CsClO_4$ films can be encapsulated by e-beam evaporated SiO_2, retaining the Cs^+ within the polymer matrix as shown with EELS imaging for the first time, as well as coated with Ti, Pd, and Pt, resulting in structures with record-thin films of ~6 and 7 nm for PEO and PEO:$CsClO_4$, respectively, as shown in the TEM cross-sections and electrical thicknesses in Chapters 3 and 4. The deposition of a top layer of SiO_2 or a metal did not significatively change the polymer film thickness with respect to an uncapped PEO:$CsClO_4$ film. This is likely because in PEO films that are a few nanometers thick, the polymer chains crystallize in a

flat-on orientation, meaning they fold into a serpentine with segments perpendicular to the surface, each ~10 nm long [59, 60].

Chapter 2 & 5 presented Multiphysics simulations of nanometric PEO:$CsClO_4$ to observe the steady-state and transient ion response to a constant or time-varying voltage bias. The charging of the EDL was seen to occur in the microsecond timescale, with the EDLs of a 10-nm film reaching 90% of their steady-state capacitance density of 3.7 $\mu F/cm^2$ after ~176 μs. While decreasing the film thickness did not affect the steady-state EDL capacitance, it did increase the speed at which it was reached, with the 5 nm film acquiring 90% of its final EDL charge ~250 μs faster than the 20 nm film, as expected for the higher electric field in it driving ions to the electrode interfaces. Thus, when voltage-limited for power reasons, nanometric, spin-coated films offer an advantage with respect to micrometric, dropcasted films because the same applied voltage produces a higher electric field, which allows for faster EDL charging.

The ion concentration used experimentally and considered in these simulations was too high to result in the EDLs at opposite electrodes overlapping and interacting with each other. To observe any potential non-linearities introduced by this interaction, the film thickness would likely need to be a few nanometers lower than 5 nm, given that the Debye length is approximately 0.7 nm. However, at that point the electrode roughness may be of comparable magnitude. Alternatively, the ion concentration could be reduced to increase the Debye length in the electrolyte; the study of any resulting nonlinearities could be the subject of future work.

The ultrathin PEO and PEO:$CsClO_4$ MIS and MIM capacitors were electrically characterized in Chapters 4 and 5, respectively. Both exhibited the same frequency

dependence of the impedance. While previous studies of thick PEO capacitors [69, 72] reported an impedance more resistive than capacitive, this work showed that MIS and MIM capacitors with nanometric PEO have an insulating, nearly ideal capacitive behavior. Ultrathin PEO ~ 6-15 nm thick was found to have a static dielectric constant of ~1.6, which is constant across ~ 3 orders of magnitude, a band gap of ~4.5 eV, and a trap density of at least ~$2.6\times10^{11}/cm^2$. The additional presence of $CsClO_4$ increases the film conductivity by 1–2 orders of magnitude, depending on the frequency. There is no indication of a significant increase in conductivity specifically due to the polymer confinement.

At high frequencies (> ~ 600 kHz), the impedance, static dielectric constant, and parallel capacitance were the same for PEO with and without ions. But below 600 kHz, electrode polarization effects became increasingly noticeable with decreasing frequency, as reported for bulk PEO and other ionic conductors [70, 78]: the dielectric constant of PEO:$CsClO_4$ increased, reaching ~ 8.0 at 1 kHz, which is 5× the value for PEO without ions; the conductivity decreased in PEO with and without ions, until reaching a plateau due to partially- but not fully-blocking nature of the electrodes, which sets a lower limit to the conductivity. Finally, for PEO:$CsClO_4$ capacitors, the linear conductivity-frequency region transitioned into a square-root dependence above ~ 100 kHz, suggesting a change in the ion conduction mechanism dominating in this frequency region [1].

This work has also proposed simple equivalent circuit models that capture the general trends of the impedance vs. frequency behavior of experimental MIS capacitors. PEO capacitors can be modeled with a single *RC* loop, where the resistance decreases with frequency. The ion transport in ultrathin PEO:$CsClO_4$ capacitors can be captured

with two *RC* loops in series: one has constant *RC* components representing ion transport in the bulk, while a second *RC* loop contains the charge transfer resistance of the partially blocking electrodes, as well as the electrode polarization capacitance. The bulk resistance for the ultrathin PEO:$CsClO_4$ capacitors, ~7–10×10^4 Ω, is around 1–5 orders of magnitude smaller than the frequency-dependent bulk resistance of PEO capacitors without an added salt, R_0/f, which varies with frequency and PEO thickness between ~10^6–10^{10} Ω. This is in agreement with the higher conductivity measured in ultrathin PEO:$CsClO_4$ capacitors.

The EDL capacitance density of ultrathin PEO:$CsClO_4$ in MIS structures was ~1.1 μF/cm^2, as estimated using the two-*RC* model and assuming the EDLs at the top and bottom electrodes are equally strong. This is below the 3.7 μF/cm^2 expected from the COMSOL Multiphysics simulations in Chapter 2, as well as the 4 μF/cm^2 yielded by prior measurements [14]. This lower-than-expected EDL capacitance density may be due to non-uniformities in the MIS structure's metal top electrode vs. the flatter Si bottom electrode. This would result in different EDL strengths at each interface, with the rougher top electrode having a lower EDL capacitance.

The Multiphysics simulations of current density in response to triangular train pulses at 500 Hz speeds agree with experimental observations in ultrathin PEO:$CsClO_4$ MIMs, as long as the applied bias is low enough to avoid leakage and charge trap filling. Larger input voltages result in an asymmetric current response and polarization loops that no longer overlap but instead increase with each sweep repetition, which may be due to electron transport and/or charge trapping. Further studies may reveal whether there are even larger electric fields that result in electron transitions that produce new phenomena.

Also, the use of lower bias frequencies increased the polarization charge and thus the strength of the EDL in the MIMs, in agreement with observations of the frequency behavior of the impedance in MIS capacitors.

The current response of PEO:$CsClO_4$ MIMs to a voltage step did not differ during the step rise and fall times, suggesting the EDL charge and discharge times also did not significantly differ. The simulations and measurements in this dissertation suggest that the MIM capacitors are completely volatile and an added layer would be necessary to introduce non-volatility. Upon interaction with either cations or anions, this layer might undergo a fast, reversible, nonvolatile reaction at the electrodes, or temporary ion or charge trapping might occur. The latter is exemplified in [82], where a Au NP layer was used to trap charge between a transistor channel and an ion gel. Considering various candidate materials may be the topic of future studies aiming at using SPEs for faster memory devices. Overall, the work in this dissertation suggests that PEO:$CsClO_4$ can be confined to thicknesses commensurate with VLSI electronics and in combination with other functional layers and devices to pursue applications in analog memory, deep learning, and neuromorphic computing.

REFERENCES

[1] C. Alessandri, S. Fathipour, H. Li, I. Kwak, A. Kummel, M. Remškar, and A. C. Seabaugh, "Reconfigurable electric double layer doping in an MoS_2 nanoribbon transistor," *IEEE Transactions on Electron Devices,* vol. 64, no. 12, pp. 5217-5222, Dec. 2017.

[2] C. Alessandri, "Ferroelectric memory and architecture for deep neural network training in resistive crossbar arrays," Doctoral Dissertation, University of Notre Dame, 2019.

[3] Y. van de Burgt, E. Lubberman, E. J. Fuller, S. T. Keene, G. C. Faria, S. Agarwal, M. J. Marinella, A. A. Talin, and A. Salleo, "A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing," *Nature Materials,* vol. 16, no. 4, p. 414, Feb. 20 2017.

[4] D. K. Efetov and P. Kim, "Controlling electron-phonon interactions in graphene at ultrahigh carrier densities," *Physical Review Letters,* vol. 105, no. 25, p. 256805, 2010.

[5] F. Liu, W. Xie, S. Shi, C. D. Frisbie, and P. P. Ruden, "Coupling of channel conductance and gate-to-channel capacitance in electric double layer transistors," *Applied Physics Letters,* vol. 103, no. 19, p. 193304, 2013.

[6] K. Ueno, H. Shimotani, H. Yuan, J. Ye, M. Kawasaki, and Y. Iwasa, "Field-induced superconductivity in electric double layer transistors," *Journal of the Physical Society of Japan,* vol. 83, no. 3, p. 032001, 2014.

[7] H. Du, X. Lin, Z. Xu, and D. Chu, "Electric double-layer transistors: A review of recent progress," *Journal of Materials Science,* vol. 50, no. 17, pp. 5641-5673, 2015.

[8] B. N. Hendy, "Ionic polymers," in *Specialty Polymers*, R. W. Dyson, Ed. Boston, MA: Springer US, 1987, pp. 110-149.

[9] K. S. Ngai, S. Ramesh, K. Ramesh, and J. C. Juan, "A review of polymer electrolytes: Fundamental, approaches and applications," *Ionics,* journal article vol. 22, no. 8, pp. 1259-1279, 2016.

[10] S. B. Aziz, T. J. Woo, M. F. Z. Kadir, and H. M. Ahmed, "A conceptual review on polymer electrolytes and ion transport models," *Journal of Science: Advanced Materials and Devices,* vol. 3, no. 1, pp. 1-17, 2018.

[11] S. B. Aziz, Z. H. Z. Abidin, and M. F. Z. Kadir, "Innovative method to avoid the reduction of silver ions to silver nanoparticles ($Ag^+ \rightarrow Ag^\circ$) in silver ion conducting based polymer electrolytes," *Physica Scripta,* vol. 90, no. 3, p. 035808, 2015.

[12] Z. Bisri Satria, S. Shimizu, M. Nakano, and Y. Iwasa, "Endeavor of iontronics: From fundamentals to applications of ion-controlled electronics," *Advanced Materials,* vol. 29, no. 25, p. 1607054, 2017.

[13] H. Yuan, H. Shimotani, A. Tsukazaki, A. Ohtomo, M. Kawasaki, and Y. Iwasa, "High-density carrier accumulation in ZnO field-effect transistors gated by electric double layers of ionic liquids," *Advanced Functional Materials,* vol. 19, no. 7, pp. 1046-1053, 2009.

[14] H. Xu, S. Fathipour, E. W. Kinder, A. C. Seabaugh, and S. K. Fullerton-Shirey, "Reconfigurable ion gating of 2H-$MoTe_2$ field-effect transistors using poly(ethylene oxide)-$CsClO_4$ solid polymer electrolyte," *ACS Nano,* vol. 9, no. 5, pp. 4900-4910, May 2015.

[15] Y. J. Zhang, J. T. Ye, Y. Yomogida, T. Takenobu, and Y. Iwasa, "Formation of a stable p–n junction in a liquid-gated MoS_2 ambipolar transistor," *Nano Letters,* vol. 13, no. 7, pp. 3023-3028, 2013.

[16] S. Fathipour, P. Paletti, S. Fullerton-Shirey, and A. Seabaugh, "Demonstration of electric double layer p-i-n junction in WSe_2," in *2016 74th Annual Device Research Conference (DRC)*, 2016, pp. 1-2.

[17] S. Fathipour, H.-M. Li, M. Remškar, L. Yeh, W. Tsai, E. Chen, Y. Lin, S. K. Fullerton-Shirey, and A. Seabaugh, "Record high current density and low contact resistance in MoS_2 FETs by ion doping," in *2016 International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA)*, 2016, Hsinchu, Taiwan.

[18] S. Fathipour, P. Pandey, S. Fullerton-Shirey, and A. Seabaugh, "Electric-double-layer doping of WSe_2 field-effect transistors using polyethylene-oxide cesium perchlorate," *Journal of Applied Physics,* vol. 120, no. 23, p. 234902, Dec. 2016.

[19] P. Paletti, R. Yue, C. Hinkle, S. K. Fullerton-Shirey, and A. Seabaugh, "Two-dimensional electric-double-layer Esaki diode," *npj 2D Materials and Applications,* vol. 3, no. 1, p. 19, 2019.

[20] P. Paletti, A. Seabaugh, R. Yue, and C. Hinkle, "Electric double layer Esaki tunnel junction in a 40-nm-length, WSe_2 channel grown by molecular beam epitaxy on Al_2O_3," in *2018 48th European Solid-State Device Research Conference (ESSDERC)*, 2018, pp. 110-113.

[21] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE Journal of the Electron Devices Society,* vol. 2, no. 4, pp. 44-49, 2014.

[22] S. Aikawa, S. Kim, T. Thurakitseree, E. Einarsson, T. Inoue, S. Chiashi, K. Tsukagoshi, and S. Maruyama, "Carrier polarity engineering in carbon nanotube field-effect transistors by induced charges in polymer insulator," *Applied Physics Letters,* vol. 112, no. 1, p. 013501, 2018.

[23] C. Lu, Q. Fu, S. Huang, and J. Liu, "Polymer electrolyte-gated carbon nanotube field-effect transistor," *Nano Letters,* vol. 4, no. 4, pp. 623-627, 2004.

[24] G. P. Siddons, D. Merchin, J. H. Back, J. K. Jeong, and M. Shim, "Highly efficient gating and doping of carbon nanotubes with polymer electrolytes," *Nano Letters,* vol. 4, no. 5, pp. 927-931, 2004.

[25] T. Ozel, A. Gaur, J. A. Rogers, and M. Shim, "Polymer electrolyte gating of carbon nanotube network transistors," *Nano Letters,* vol. 5, no. 5, pp. 905-911, 2005.

[26] P. Paletti, M. Asghari Heidarlou, K. González Serrano, C. Alessandri, and A. Seabaugh, "Steep subthreshold swing originating from gate delay," in *Device Research Conference*, 2019, Ann Arbor, Michigan.

[27] A. Seabaugh, P. Paletti, A. Palit, K. González-Serrano, and P. Pandey, "Dynamics of ferroelectric and ionic memories: Physics and applications," in *2019 IEEE 13th International Conference on ASIC (ASICON)*, 2019, pp. 1-4.

[28] D. Akinwande, N. Patil, A. Lin, Y. Nishi, and H. S. P. Wong, "Surface science of catalyst dynamics for aligned carbon nanotube synthesis on a full-scale quartz wafer," *The Journal of Physical Chemistry C,* vol. 113, no. 19, pp. 8002-8008, 2009.

[29] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nature Nanotechnology,* vol. 8, p. 13, Dec. 2012.

[30] C. T. Chang, F. Zeng, X. J. Li, W. S. Dong, S. H. Lu, S. Gao, and F. Pan, "Simulation of synaptic short-term plasticity using Ba(CF3SO3)2-doped polyethylene oxide electrolyte film," *Scientific Reports,* vol. 6, no. 1, p. 18915, 2016.

[31] A. Seabaugh and S. Fullerton, "Single transistor random access memory using ion storage in two-dimensional crystals," *U. S. Pat. Number 9,899,480,* 20 Feb. 2018.

[32] W.-H. Wang, C. Gong, W. Wang, F. Kong, H. Kim, S. K. Fullerton-Shirey, A. Seabaugh, and K. Cho, "Energetics of metal ion adsorption on and diffusion through crown ethers: First principles study on two-dimensional electrolyte," *Solid State Ionics,* vol. 301, pp. 176-181, Mar. 2017.

[33] C. L. Chen, K. Kim, Q. Truong, A. Shen, Z. Li, and Y. Chen, "A spiking neuron circuit based on a carbon nanotube transistor," *Nanotechnology,* vol. 23, no. 27, p. 275202, 2012.

[34] N. S. T. Do, D. M. Schaetzl, B. Dey, A. C. Seabaugh, and S. K. Fullerton-Shirey, "Influence of Fe_2O_3 nanofiller shape on the conductivity and thermal properties of solid polymer electrolytes: Nanorods versus nanospheres," *The Journal of Physical Chemistry C,* vol. 116, no. 40, pp. 21216-21223, Oct. 2012.

[35] S. Yu and P. Chen, "Emerging memory technologies: Recent trends and prospects," *IEEE Solid-State Circuits Magazine,* vol. 8, no. 2, pp. 43-56, 2016.

[36] M.-F. Chang, "Nonvolatile circuits for memory, logic, and artificial intelligence," presented at the 2018 IEEE International Solid-State Circuits Conference-(ISSCC), 2018.

[37] H.-M. Li, K. Xu, B. Bourdon, H. Lu, Y.-C. Lin, J. A. Robinson, A. C. Seabaugh, and S. K. Fullerton-Shirey, "Electric double layer dynamics in poly(ethylene oxide) $LiClO_4$ on graphene transistors," *The Journal of Physical Chemistry C,* vol. 121, no. 31, pp. 16996-17004, 2017.

[38] K. Xu, M. M. Islam, D. Guzman, A. C. Seabaugh, A. Strachan, and S. K. Fullerton-Shirey, "Pulse dynamics of electric double layer formation on all-solid-state graphene field-effect transistors," *ACS Applied Materials & Interfaces,* vol. 10, no. 49, pp. 43166-43176, 2018.

[39] A. Woeppel, K. Xu, A. Kozhakhmetov, S. Awate, J. A. Robinson, and S. K. Fullerton-Shirey, "Single- versus dual-ion conductors for electric double layer gating: Finite element modeling and Hall-effect measurements," *ACS Applied Materials & Interfaces,* vol. 12, no. 36, pp. 40850-40858, 2020.

[40] M. K. Mundra, S. K. Donthu, V. P. Dravid, and J. M. Torkelson, "Effect of spatial confinement on the glass-transition temperature of patterned polymer nanostructures," *Nano Letters,* vol. 7, no. 3, pp. 713-718, 2007.

[41] H. Schönherr and C. W. Frank, "Ultrathin films of poly(ethylene oxides) on oxidized silicon. 1. Spectroscopic characterization of film structure and crystallization kinetics," *Macromolecules,* vol. 36, no. 4, pp. 1188-1198, 2003.

[42] H. Lu, I. Kwak, J. H. Park, K. O'Neill, T. Furuyama, N. Kobayashi, A. Seabaugh, A. Kummel, and S. K. Fullerton-Shirey, "Solution-cast monolayers of cobalt crown ether phthalocyanine on highly ordered pyrolytic graphite," *The Journal of Physical Chemistry C,* vol. 119, no. 38, pp. 21992-22000, Sept. 24 2015.

[43] K. Xu, H. Lu, E. W. Kinder, A. Seabaugh, and S. K. Fullerton-Shirey, "Monolayer solid-state electrolyte for electric double layer gating of graphene field-effect transistors," *ACS Nano,* vol. 11, no. 6, pp. 5453-5464, Jun. 2017.

[44] G. Reiter and J.-U. Sommer, "Crystallization of adsorbed polymer monolayers," *Physical Review Letters,* vol. 80, no. 17, pp. 3771-3774, 1998.

[45] B. Wang, S. Tang, Y. Wang, C. Shen, R. Reiter, G. Reiter, J. Chen, and B. Zhang, "Systematic control of self-seeding crystallization patterns of poly(ethylene oxide) in thin films," *Macromolecules,* vol. 51, no. 5, pp. 1626-1635, 2018.

[46] K. Dalnoki-Veress, J. A. Forrest, M. V. Massa, A. Pratt, and A. Williams, "Crystal growth rate in ultrathin films of poly(ethylene oxide)," *Journal of Polymer Science Part B: Polymer Physics,* vol. 39, no. 21, pp. 2615-2621, 2001.

[47] F. Zhang, M. Ceder, and O. Inganäs, "Enhancing the photovoltage of polymer solar cells by using a modified cathode," *Advanced Materials,* vol. 19, no. 14, pp. 1835-1838, 2007.

[48] D. J. Carrad, A. M. Burke, R. W. Lyttleton, H. J. Joyce, H. H. Tan, C. Jagadish, K. Storm, H. Linke, L. Samuelson, and A. P. Micolich, "Electron-beam patterning of polymer electrolyte films to make multiple nanoscale gates for nanowire transistors," *Nano Letters,* vol. 14, no. 1, pp. 94-100, 2014.

[49] E. W. Kinder, A. Fuller, Y.-C. Lin, J. A. Robinson, and S. K. Fullerton-Shirey, "Increasing the room-temperature electric double layer retention time in two-dimensional crystal FETs," *ACS Applied Materials & Interfaces,* vol. 9, no. 29, pp. 25006-25013, 2017.

[50] *COMSOL Multiphysics, coefficient form partial differential equation solver and AC/DC module* 5.4, COMSOL AB, Stockholm, Sweden. [Online]. Available: https://www.comsol.com.

[51] M. S. Kilic, M. Z. Bazant, and A. Ajdari, "Steric effects in the dynamics of electrolytes at large applied voltages. II. Modified Poisson-Nernst-Planck equations," *Physical Review E,* vol. 75, no. 2, p. 021503, 2007.

[52] D. Alby, C. Charnay, M. Heran, B. Prelot, and J. Zajac, "Recent developments in nanostructured inorganic materials for sorption of cesium and strontium: Synthesis and shaping, sorption capacity, mechanisms, and selectivity—A review," *Journal of Hazardous Materials,* vol. 344, pp. 511-530, 2018.

[53] R. Shannon, "Revised effective ionic radii and systematic studies of interatomic distances in halides and chalcogenides," *Acta Crystallographica Section A,* vol. 32, no. 5, pp. 751-767, 1976.

[54] T. M. W. J. Bandara, H. D. N. S. Fernando, M. Furlani, I. Albinsson, M. A. K. L. Dissanayake, J. L. Ratnasekera, and B. E. Mellander, "Effect of the alkaline cation size on the conductivity in gel polymer electrolytes and their influence on photo electrochemical solar cells," *Physical Chemistry Chemical Physics,* vol. 18, no. 16, pp. 10873-10881, 2016.

[55] A. E. Binks and A. Sharples, "Electrical conduction in olefin oxide polymers," *Journal of Polymer Science Part A-2: Polymer Physics,* vol. 6, no. 2, pp. 407-420, 1968.

[56] S. K. Fullerton-Shirey and J. K. Maranas, "Effect of $LiClO_4$ on the structure and mobility of PEO-based solid polymer electrolytes," *Macromolecules,* vol. 42, no. 6, pp. 2142-2156, 2009.

[57] K. A. Gonzalez-Serrano and A. C. Seabaugh, "Electrical Properties of Spin-Coated Polyethylene Oxide Capacitors as Thin as 8 nm," presented at the 62nd Electronic Materials Conference, virtual, June 24-26, 2020.

[58] K. A. Gonzalez-Serrano and A. C. Seabaugh, "Electrical Properties of 6 nm to 19 nm Thick Polyethylene Oxide Capacitors for Ion/Electron Functional Devices," *Journal of Electronic Materials,* 2021.

[59] H.-G. Braun and E. Meyer, "Structure Formation of Ultrathin PEO Films at Solid Interfaces—Complex Pattern Formation by Dewetting and Crystallization," (in eng), *International journal of molecular sciences,* vol. 14, no. 2, pp. 3254-3264, 2013.

[60] J.-U. Sommer and G. Reiter, "Crystallization in ultra-thin polymer films: Morphogenesis and thermodynamical aspects," *Thermochimica Acta,* vol. 432, no. 2, pp. 135-147, 2005.

[61] J. L. Hart, A. C. Lang, A. C. Leff, P. Longo, C. Trevor, R. D. Twesten, and M. L. Taheri, "Direct detection electron energy-loss spectroscopy: A method to push the limits of resolution and sensitivity," *Scientific Reports,* vol. 7, no. 1, p. 8243, 2017.

[62] Y.-F. Su, J. G. Park, A. Koo, S. Trayner, A. Hao, R. Downes, and R. Liang, "Characterization at atomic resolution of carbon nanotube/resin interface in nanocomposites by mapping sp^2-bonding states using electron energy-loss spectroscopy," *Microscopy and Microanalysis,* vol. 22, no. 3, pp. 666-672, 2016.

[63] R. Senga, H.-P. Komsa, Z. Liu, K. Hirose-Takai, A. V. Krasheninnikov, and K. Suenaga, "Atomic structure and dynamic behaviour of truly one-dimensional ionic chains inside carbon nanotubes," *Nature Materials,* Article vol. 13, p. 1050, Sep. 2014.

[64] C. Alessandri, P. Pandey, A. Abusleme, and A. Seabaugh, "Switching dynamics of ferroelectric Zr-doped HfO_2," *IEEE Electron Device Letters,* vol. 39, no. 11, pp. 1780-1783, 2018.

[65] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. Wiley, 2002.

[66] R. Islam, H. Li, P.-Y. Chen, W. Wan, H.-Y. Chen, B. Gao, H. Wu, S. Yu, K. Saraswat, and H. S. Philip Wong, "Device and materials requirements for neuromorphic computing," *Journal of Physics D: Applied Physics,* vol. 52, no. 11, p. 113001, 2019.

[67] W. Haensch, T. Gokmen, and R. Puri, "The Next Generation of Deep Learning Hardware: Analog Computing," *Proceedings of the IEEE,* vol. 107, pp. 108-122, 2019.

[68] J. Chen, C. D. Frisbie, and F. S. Bates, "Lithium Perchlorate-Doped Poly(styrene-b-ethylene oxide-b-styrene) Lamellae-Forming Triblock Copolymer as High Capacitance, Smooth, Thin Film Dielectric," *The Journal of Physical Chemistry C,* vol. 113, no. 10, pp. 3903-3908, 2009.

[69] N. H. A. Nasir, C. H. Chan, H.-W. Kammer, L. H. Sim, and M. Z. A. Yahya, "Ionic Conductivity in Solutions of Poly(ethylene oxide) and Lithium Perchlorate," *Macromolecular Symposia,* vol. 290, no. 1, pp. 46-55, 2010.

[70] A. A. Khamzin, I. I. Popov, and R. R. Nigmatullin, "Correction of the power law of ac conductivity in ion-conducting materials due to the electrode polarization effect," *Physical Review E,* vol. 89, no. 3, p. 032303, March 2014.

[71] S. K. Chaurasia, A. L. Saroj, Shalu, V. K. Singh, A. K. Tripathi, A. K. Gupta, Y. L. Verma, and R. K. Singh, "Studies on structural, thermal and AC conductivity scaling of PEO-$LiPF_6$ polymer electrolyte with added ionic liquid [$BMIMPF_6$]," *AIP Advances,* vol. 5, no. 7, p. 077178, July 1 2015.

[72] C. H. Chan, H.-W. Kammer, L. H. Sim, S. N. H. M. Yusoff, A. Hashifudin, and T. Winie, "Conductivity and dielectric relaxation of Li salt in poly(ethylene oxide) and epoxidized natural rubber polymer electrolytes," *Ionics,* vol. 20, no. 2, pp. 189-199, February 2014.

[73] W. R. Frensley. *BandProf*, UT Dallas. [Online]. Available: https://personal.utdallas.edu/~frensley/hlts/bandprof.html.

[74] V. M. Mohan, V. Raja, P. B. Bhargav, A. K. Sharma, and V. V. R. N. Rao, "Structural, electrical and optical properties of pure and $NaLaF_4$ doped PEO polymer electrolyte films," *Journal of Polymer Research,* vol. 14, no. 4, pp. 283-290, April 2007.

[75] S. K. Fullerton-Shirey, L. V. N. R. Ganapatibhotla, W. Shi, and J. K. Maranas, "Influence of thermal history and humidity on the ionic conductivity of nanoparticle-filled solid polymer electrolytes," *Journal of Polymer Science Part B: Polymer Physics,* vol. 49, no. 21, pp. 1496-1505, 2011.

[76] P. Paletti, M. A. Heidarlou, K. G. Serrano, C. Alessandri, and A. Seabaugh, "Steep Subthreshold Swing Originating from Gate Delay," in *2019 Device Research Conference (DRC)*, 2019, pp. 53-54.

[77] J. C. Dyre, P. Maass, B. Roling, and D. L. Sidebottom, "Fundamental questions relating to ion conduction in disordered solids," *Reports on Progress in Physics,* vol. 72, no. 4, p. 046501, 2009.

[78] A. Telfah, M. M. Abdul-Gader Jafar, I. Jum'h, M. J. A. Ahmad, J. Lambert, and R. Hergenröder, "Identification of relaxation processes in pure polyethylene oxide (PEO) films by the dielectric permittivity and electric modulus formalisms," *Polymers for Advanced Technologies,* vol. 29, no. 7, pp. 1974-1987, 2018.

[79] Y. Ma, Hu, and G. Reiter, "Lamellar Crystal Orientations Biased by Crystallization Kinetics in Polymer Thin Films," *Macromolecules,* vol. 39, no. 15, pp. 5159-5164, 2006.

[80] Y. Jiang, D.-D. Yan, X. Gao, C. C. Han, X.-G. Jin, L. Li, Y. Wang, and C.-M. Chan, "Lamellar Branching of Poly(bisphenol A-co-decane) Spherulites at Different Temperatures Studied by High-Temperature AFM," *Macromolecules,* vol. 36, no. 10, pp. 3652-3655, 2003.

[81] M. K. Sen, "Crystallization kinetics and crystal morphology of ultrathin polycaprolactone films directed by supercritical carbon dioxide," 2012.

[82] J. Koo, J. Yang, B. Cho, H. Jo, K. H. Lee, and M. S. Kang, "Nonvolatile Electric Double-Layer Transistor Memory Devices Embedded with Au Nanoparticles," *ACS Applied Materials & Interfaces,* vol. 10, no. 11, pp. 9563-9570, 2018.

APPENDIX A:

STEEP SUBTRESHOLD SWING ORIGINATING FROM GATE DELAY

Abstract of work presented at the 2019 Device Research Conference

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Apparent Steep Subthreshold Swing. Complex gate dielectrics are being widely explored to provide voltage amplification leading to steep subthreshold swing (SS) in transistors [1]. Here we show that hysteretic steep SS can arise simply from the introduction of a series resistance in the gate of a metal-oxide-semiconductor field-effect transistor (MOSFET), i.e. as a dynamic effect. The choice of measurement slew rate (SR) and slew direction then directly affects the measured SS as has been previously reported [2]. We use an ionic polymer gate dielectric to illustrate how the series resistance arises from the ionic conductance controlling the time response of the electric double layer (EDL) at the polymer/metal [3] or polymer/semiconductor interface [4]. While the ionic polymer in an EDL transistor is used to illustrate the effects, the principles apply generally to other complex insulating gates including ferroelectrics and piezoelectrics.

EDL Capacitor Dynamics. We first show that in a polyethylene oxide (PEO)-based metal-insulator-metal (MIM) capacitor with drop-cast PEO thickness of ~1 µm, the RC response of the dielectric is controlled by the ionic conductivity of the PEO. Two capacitors were fabricated, one with pure PEO and one containing the salt $CsClO_4$ (ether oxygen to Cs^+ molar ratio of 76:1, corresponding to an ion concentration of ~2.2×10^{20} cm^{-3}). In response to a triangular waveform of amplitude of ±1 V, with a period of 400 µs, the dynamic response of the pure PEO capacitor is well described by a simple RC equivalent circuit stemming from EDLs formed by background OH^- and H^+ ions. The dynamic response of the second PEO capacitor with $CsClO_4$ exhibits a time evolution characterized by two distinct time constants, with 16x higher current. Fitting to those measurements can be used to extract the R and C components. The slow response is a result of the low conductance of the Cs^+ and ClO_4^- ions in PEO, in series to an EDL capacitance density C_{EDL} of 2.26 µF/cm^2. More rigorously, C_{EDL} results from the series combination of the Stern layer and diffuse layer capacitance [5], analytical modeling of the bias dependence of the EDL differential capacitance show that it depends on the salt concentration and can be nonmonotonic.

Two-Dimensional (2D) EDL FET Modeling – Transient vs. Static Response. An analytic model of the ionic polymer gate on a 2D FET has been implemented to explore the dynamic behavior of the combination. The equivalent circuit of the gate dielectric is

readily captured by a series resistance represented by a series RC circuit shunted by the geometrical capacitance of the polymer dielectric, C_{INS}, on a generic 2D FET [6]. The FET electrostatics is described by a quantum capacitance, C_Q, and an interface trap capacitance which accounts for deviations from ideality in the subthreshold regime. The model reveals the partitioning of voltage drops across the diffuse layer, V_D, the Stern layer, V_S, and the 2D channel, V_{CH}. The lag induced by the gate time constant opens up a Q_{EDL}-V_{GS} hysteresis loop that widens for decreasing waveform periods while decreasing the maximum charge density accumulated within the EDL. Dynamics are also revealed in the V_{CH}-V_{GS} relation, where it is interesting to note that during the backward sweep, due to a decrement in the total gate capacitance within the subthreshold region, the voltage gain ($A_V = \Delta V_{CH}/\Delta V_{GS}$) exceeds unity, an indication of a sub-unity body factor. The computed current for an *n*FET ($W/L = 1$, $\mu_n = 100$ cm^2/Vs) reveals that SS becomes less than 60 mV/dec in the backward sweep becoming steeper as sweep rate is increased, while the extent of the sub-60 region expands.

WSe_2 EDL FET with Steep SS. Multilayer WSe_2 EDL FETs were fabricated following the process described in [7] and the same PEO:$CsClO_4$ ionic gate was utilized. In this transistor a side gate (SG) electrode was employed to record the I_D-V_{GS} transfer characteristics. First the SG was swept from −5 to 5 V with a SR of 5 mV/s to show a Schottky barrier FET characteristic exhibiting ambipolar transport and strong electron conduction (I_D ~4.8 µA/µm for $V_{SG} = 5$ V, and $V_{DS} = -0.05$ V). After a hold time of 40 minutes, the backward sweep was recorded displaying a clear counterclockwise hysteresis. The SS is more than 3x steeper in the reverse direction with a SS_{MIN} ~48 mV/dec at low currents ($V_{DS} = -0.05$ V). Similarly, for the hole branch the delayed discharge of the hole/ ClO_4^- EDL results in a SS < 50 mV/dec. In summary, we show that apparent SS less than 60 mV/dec can result simply from gate delay. In measurement of SS, care must be taken to ensure that SS does not depend on SR or slew direction.

[1] H. Agarwal *et al.*, *IEEE-EDL,* vol. 39, p. 1254, (2018).	[2] H. Wang *et al.*, *IEDM Tech. Dig.*, p. 31-1, (2018).
[3] T. Asano *et al.*, *ACS Appl. Mater. Interfaces*, vol. 9, 5056 (2017).	[4] K. Xu *et al.*, *ACS Appl. Mater. Interfaces*, 10, 43166 (2018).
[5] M. S. Kilic *et al.*, *Phys. Rev. E,* vol. 75, p. 021503, (2007).	[6] E. G. Marin *et al.*, *IEEE-TED*, vol. 65, p. 1239, (2018).
[7] M. Asghari Heidarlou *et al.*, *76th DRC*, p. 1-2, (2018).	

EDL Capacitor Dynamics

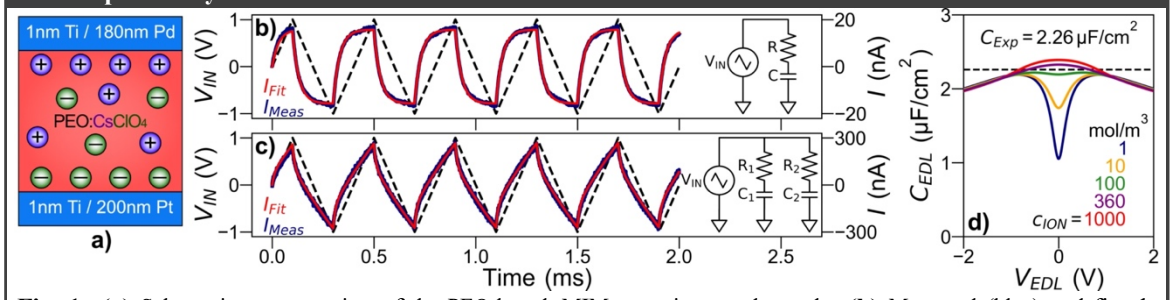

Fig. 1. **(a)** Schematic cross section of the PEO-based MIM capacitors under study. **(b)** Measured (blue) and fitted (red) *I-t* traces of an MIM device without ions (dashed line represents the input voltage waveform). Inset: equivalent circuit used for the modeling. **(c)** Same characterization for a MIM device containing the salt $CsClO_4$. **(d)** Computed C_{EDL}-V_{EDL} characteristics for different bulk salt concentrations. C_{EDL} is given by the series combination of the Stern capacitance, C_S, and the diffuse layer capacitance, C_D.

2D EDL FET Modeling – Transient vs. Static Response

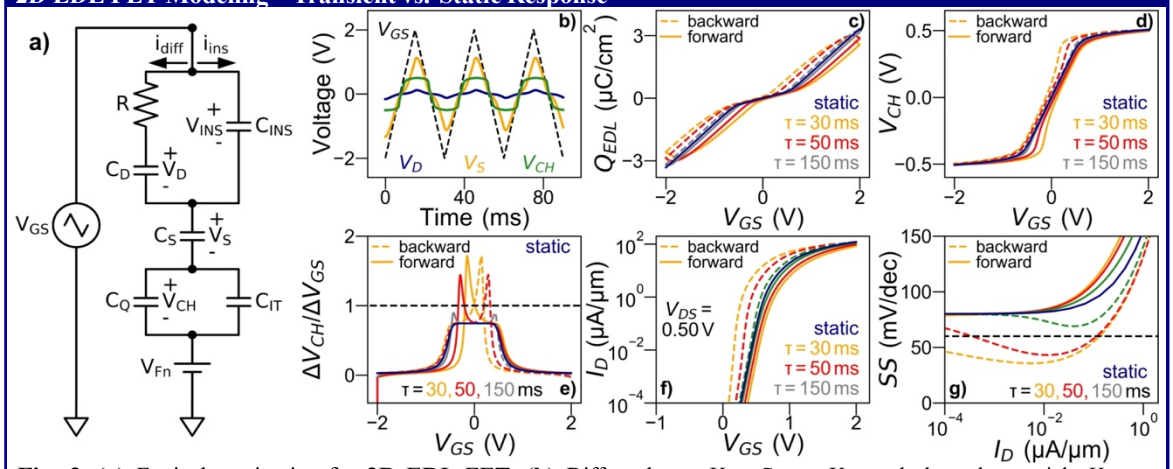

Fig. 2. **(a)** Equivalent circuit of a 2D EDL FET. **(b)** Diffuse layer, V_D, Stern, V_S, and channel potential, V_{CH}, waveforms in response to a triangular V_{GS} input. **(c)** Q_{EDL}-V_{GS} and **(d)** V_{CH}-V_{GS} loops under different waveform periods, and comparison with the static solution. © Voltage gain A_V = V_{CH} /V_{GS} as a function of V_{GS}. A_V implies sub-unity body factor. **(f)** Computed I_D-V_{GS} transfer characteristics and **(g)** extracted SS. SS < 60 mV/dec is obtained in the backward direction for fast V_{GS} sweeps.

WSe_2 EDL FET with Steep SS

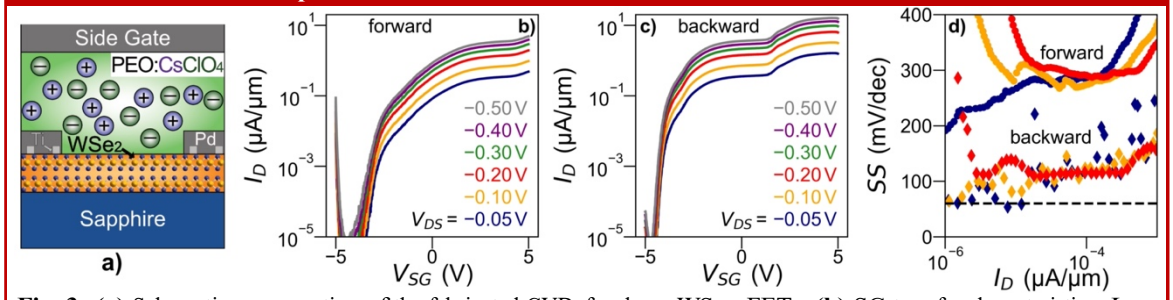

Fig. 3. **(a)** Schematic cross section of the fabricated CVD few-layer WSe_2 FETs. **(b)** SG transfer characteristics I_D-V_{SG} obtained by sweeping the SG voltage from -5 to 5 V, with SR = 5 mV/dec. **(c)** Same characterization in the reverse direction. In between the two measurements the SG voltage was kept constant at 5 V for 40 min, resulting in a strengthening of the electron branch. **(d)** Comparison of *SS* vs I_D for the forward and backward sweep directions. SS_{MIN} ~ 48mV/dec is measured for V_{DS} = -0.05 V in the backward sweep.

APPENDIX B:

ELECTRICAL PROPERTIES OF SPIN-COATED POLYETHYLENE OXIDE CAPACITORS AS THIN AS 8 NM

Abstract of work presented at the 2020 Electronic Materials Conference
Symposium: Organic Materials, Thin Films and Devices

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Polyethylene oxide (PEO) containing an alkali perchlorate has been widely used to electrolytically gate thin film and two-dimensional semiconductors [1-3]. Considering the use of this material at the limits of device scaling, we report the properties of metal/PEO/Si (MPS) capacitors at the limits of thickness scaling as obtained by spin coating in an Ar ambient. Thicknesses were measured by ellipsometry, accumulation capacitance measurements, and transmission electron microscopy (TEM) with a thickness of ~8 nm observed by TEM.

In an argon glovebox (99.999% Ar, H_2O <0.1 ppm, O_2 <0.1 ppm), PEO (Mw=110,000 g/mol, Polymer Standards Service) was dissolved in acetonitrile at room temperature to form a 1% wt. solution. $CsClO_4$ was added in an ether oxygen to Cs^+ ratio of 76:1. In the glovebox, pure–PEO or PEO:$CsClO_4$ was coated on 3.5 × 3.5 cm^2 Si wafers (n–type: Antimony, (100), 0.01–0.02 Ω–cm; p–type: Boron, 0.01–0.02 Ω–cm) that were MOS cleaned and HF dipped (50:1 DI:HF, 5 s) in a cleanroom, followed by transfer into the glovebox within ~5 min. Wafers were spun at a spin speed of either 2, 4, 6, 8, or 10 krpm for 30 s, then baked at 50 °C for 10 minutes to evaporate the solvent. Finally, capacitor top–electrodes labeled gate were formed by shadow mask evaporation (1 nm Ti / 180 nm Pd, diameters 20, 45, and 63 μm) by electron–beam evaporation. When not under test in an N_2 ambient, the capacitors were stored in an Ar glovebox to minimize water absorption. Variable angle spectroscopic ellipsometry (VASE, J. A. Woollam Co., Inc.) measurements in air and at room temperature were first used to fit the frequency ($1/\lambda$) dependence of PEO's index of refraction n using a Cauchy formula, $n(\lambda) = A + B/\lambda^2$ (fitting parameters: A, B). This was then used to determine thickness of PEO on Si vs. spins speed. Thickness was also measured from accumulation capacitance measurements and the thinnest PEO capacitor corresponding to the 8 krpm spin speed was also measured by transmission electron microscopy. The electrical and TEM measurements were in agreement, but the ellipsometric thicknesses were larger by approximately 3x.

The frequency dependence of the impedance (*Z–f*) was measured in capacitors of various thicknesses biased in accumulation (with the gate at V_G = 2 V). The impedance magnitude was well behaved, decreasing inversely with frequency while the phase remained around –90°, as expected for a simple capacitor. This ideal frequency dependence was also observed for bias conditions spanning the range of voltage used in subsequent *C-V* measurements. Pure–PEO capacitors were simulated in BandProf (W.R. Frensley, UT Dallas) to obtain band diagrams and expected *C–V* characteristics. The modeled device had an n–Si substrate (N_D = 1×10^{18} cm^{-3}), thickness t_{PEO} = 7.4 nm, dielectric constant ε_{PEO} = 1.5, band gap = 4.5 eV [4], with metal/PEO Schottky barrier of 2.2 eV, and PEO/Si ΔE_C of 1.2 eV. The predicted *C–V* was compared with measurements, showing basic agreement with accumulation capacitance and minimum capacitance, but deviating from simulation in the depletion capacitance transition. The accumulation capacitance and the inverse thickness at various spin speeds were then used to extract the dielectric constant of PEO, ε_{PEO} ~ 1.6 ± 0.1, which is consistent with a prior report for thick PEO films, ~0.25–0.40 mm [5].

PEO:$CsClO_4$ on p^+–Si was ~8 nm thicker than pure–PEO when measured by ellipsometry before gate evaporation. *Z—f* showed that capacitors with $CsClO_4$ had a lower impedance magnitude than pure PEO and a less ideal phase between –50° and –80°. However, the accumulation capacitance at –1.6 V was only ~10% lower.

[1] D. K. Efetov and P. Kim, *Phys. Rev. Lett.* 105, p. 256805 (2010). [2] K. Ueno, H. Shimotani, H. Yuan, J. Ye, M. Kawasaki, and Y. Iwasa, *J. Phys. Soc. Jpn*. 83, p. 032001 (2014). [3] C. Alessandri, S. Fathipour, H. Li, I. Kwak, A. Kummel, M. Remškar, and A. C. Seabaugh, *IEEE Trans. Electron Dev.* 64, pp. 5217–5222 (2017). [4] V. M. Mohan, V. Raja, P. B. Bhargav, A. K. Sharma, and V. V. R. N. Rao, *J. Polymer Research* 14, pp. 283-290 (2007). [5] N. H. A. Nasir, C. H. Chan, H.-W. Kammer, L. H. Sim, and M. Z. A. Yahya, *Macromolecular Symposia* 290, pp. 46-55 (2010).

Electrical Properties of Spin-Coated Polyethylene Oxide Capacitors as Thin as 8 nm

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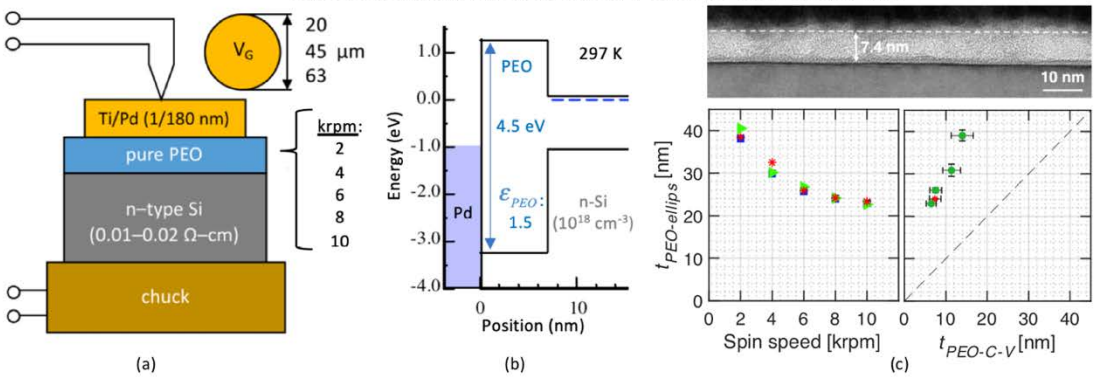

Fig. 1(a) Metal/polyethylene oxide (PEO)/Si (MPS) capacitors formed by shadow evaporation. The spin coated PEO has a molecular weight of 110 kg/mole. (b) Energy band diagram of an MPS capacitor simulated in BandProf (W.R. Frensley, UT Dallas) and biased at flatband. The modeled device: n–Si substrate: $N_D = 1\times10^{18}$ cm^{-3}, thickness $t_{PEO} = 7.4$ nm, dielectric constant $\varepsilon_{PEO} = 1.5$, band gap = 4.5 eV, with metal/PEO Schottky barrier of 2.2 eV, and ΔE_C PEO/Si of 1.2 eV. (c) TEM of an MPS capacitor with an ultrathin layer of ~7.4 nm, PEO thickness vs. spin speed measured by ellipsometry (at three positions per wafer), before depositing the gate electrodes by e-beam evaporation. Ellipsometric vs. electrical thickness extracted from TEM (red) and capacitance-voltage (*C-V*) measurements (green). Electrical thickness from accumulation capacitance and TEM agree; ellipsometric thicknesses are greater by ~3x.

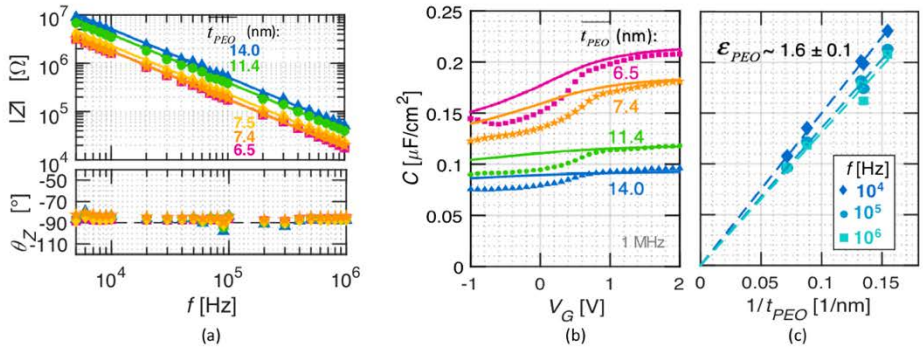

Fig. 2(a) Frequency dependence of the impedance (*Z–f*) of MPS capacitors with different PEO thicknesses, biased in accumulation at $V_G = 2$ V. Measurements (markers) are compared to an ideal capacitor's $|Z|$ (lines) of thickness t_{PEO} and dielectric constant $\varepsilon_{PEO} = 1.5$. (b) Simulated (lines) and measured (markers) *C–V* of MPS capacitors vs. PEO thicknesses. (c) Capacitance vs. inverse PEO thickness, extracted from TEM and *C–V* measurements, taken at 10k, 100k, and 1MHz. The dielectric constant of PEO, $\varepsilon_{PEO} = 1.6 \pm 0.1$, was extracted using a linear fit of the accumulation capacitance per area (at 2 V) and the inverse PEO thickness.

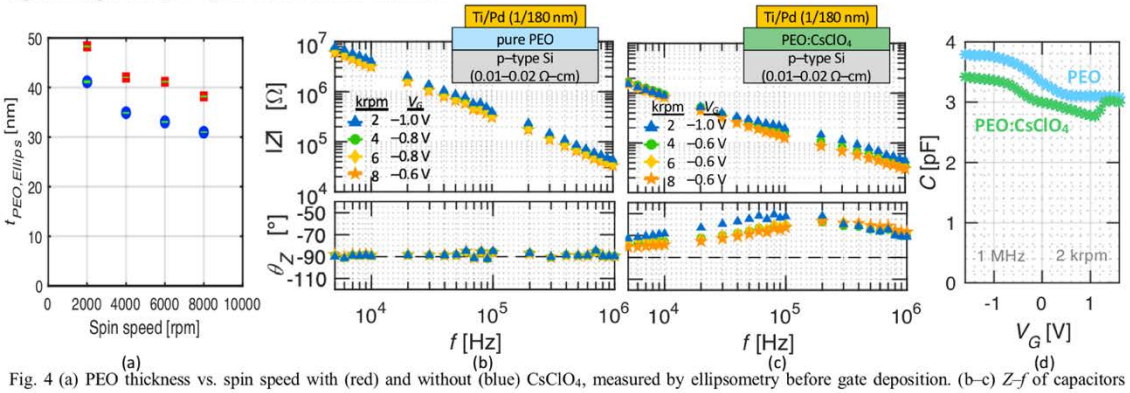

Fig. 4 (a) PEO thickness vs. spin speed with (red) and without (blue) $CsClO_4$, measured by ellipsometry before gate deposition. (b–c) *Z–f* of capacitors without (b) and with (c) $CsClO_4$ biased in the range −0.6 to −1 V. (d) *C–V* of capacitors with PEO with (green) and without (blue) $CsClO_4$ spun at 2 krpm.

APPENDIX C:

ELECTRICAL PROPERTIES OF 6 NM TO 19 NM THICK POLYETHYLENE OXIDE CAPACITORS FOR ION/ELECTRON FUNCTIONAL DEVICES

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Electrical Properties of 6 nm to 19 nm Thick Polyethylene Oxide Capacitors for Ion/Electron Functional Devices

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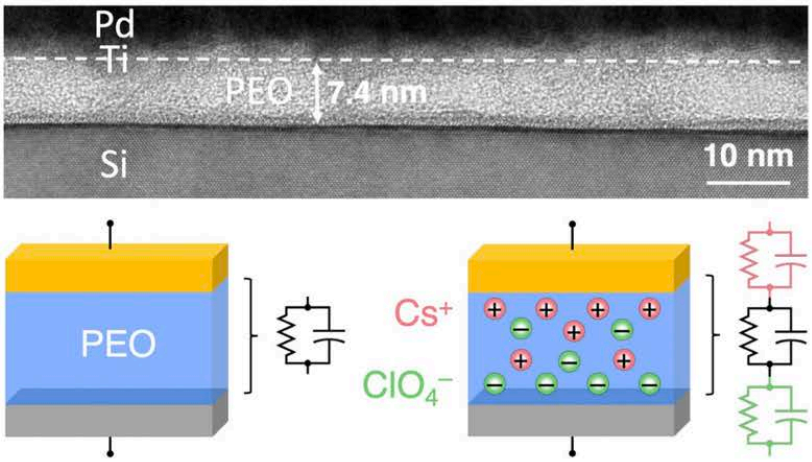
The impedance–frequency and capacitance–voltage characteristics of metal/polyethylene oxide (PEO)/Si (MOS) capacitors at thicknesses relevant to transistor technology are measured with and without $CsClO_4$. Basic understanding of the impedance frequency and voltage characteristics of this MOS system is established in spin-coated films in the thickness range from 6 nm to 19 nm, as determined from capacitance measurements and transmission electron microscopy. Estimates of the dielectric constant, energy band diagram, charge trap density, and conductivity in ultrathin PEO are obtained. Simple equivalent circuits based on resistive and capacitive elements that reflect the physical system are used to model the measured impedance frequency trends and compare films with and without $CsClO_4$ in the polymer matrix. This study reveals the electrical properties of PEO near the limits of thickness scaling, toward memory and neuromorphic device applications.

Graphic Abstract



Key words: Metal oxide semiconductor capacitor, polyethylene oxide, cesium perchlorate, electric double layer, ultrathin polymer

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INTRODUCTION

In the early days of metal oxide semiconductor field-effect transistor (MOSFET) development, ions such as Na and K were extensively characterized to understand their source and eliminate them from SiO_2 gate oxides.[1] Mobile ions in MOSFET oxides introduce hysteresis in the threshold voltage, which is an effect generally to be minimized. However, with recent interest in analog memory for weight storage in neural networks and synapse formation in neuromorphic computing, the hysteretic properties of oxides are inspiring applications.[2,3]

Polyethylene oxide (PEO) containing an alkali perchlorate has been widely used to electrolytically gate thin film and two-dimensional semiconductors.[4–8] It is common for the thicknesses in these studies to be in the range of 0.2–1 μm, well beyond the thickness scales of VLSI (very large-scale integration) electronics. In this paper, we investigate the properties of spin-coated PEO in the thickness range of 6–19 nm. We fabricate MOS capacitors and perform impedance spectroscopy to provide data in a form common to the characterization of solid-state oxides. By comparing PEO with and without the ionic salt $CsClO_4$, we are able to understand the effect of the salt on the capacitor electrical properties and show that the solid polymer PEO in ultrathin MOS capacitors has low leakage and remarkably ideal impedance–frequency behavior. This is then compared with PEO MOS capacitors containing the salt $CsClO_4$, which shows that the effects of the ionic content in these ultrathin films are remarkably consistent with prior reports on much thicker films.

EXPERIMENTAL

PEO was prepared by spin coating films with and without $CsClO_4$. Conventional Si surface preparation steps were used prior to spin coating, including an RCA-clean and buffered-HF dip. This was followed immediately by transfer into an Ar glovebox for spin coating to minimize exposure of the PEO to water vapor and O_2. An MBraun glovebox was used to maintain O_2 content below 0.1 ppm. The PEO was obtained from Polymer Standards Service (PSS-peo110k). Solutions of PEO with and without $CsClO_4$ were prepared using methods previously described.[9] $CsClO_4$ is a product of Sigma Aldrich with purity 99.995%, and the mole fraction used was 0.013. Spin coating was applied to 3.5×3.5 cm^2 Si (100) substrates with a resistivity of 0.01–0.02 Ω-cm, and for two carrier types: *n*-type, Sb, and *p*-type, B. PEO without $CsClO_4$ was spun on *n*-Si wafers at 2 krpm, 4 krpm, 6 krpm, 8 krpm, or 10 krpm. PEO either with or without $CsClO_4$ was spin coated on *p*-Si wafers at 2 krpm, 4 krpm, 6 krpm, or 8 krpm. Each wafer was spun for 30 s, followed by a hot-plate bake at 50°C for 10 min in the Ar glovebox to evaporate the solvent. Top-electrodes were formed by electron-beam evaporation through a shadow mask; the deposition consisted of a 1 nm Ti adhesion layer followed by 180 nm Pd top electrode. Capacitor diameters of 20 μm, 45 μm, and 63 μm were used to provide normalized area steps of $1\times$, $5\times$, and $10\times$. When not under test in an N_2 ambient, the capacitors were stored in the Ar glovebox to minimize water absorption.

Electrical measurements were made in a Cascade Summit 11000 probe station at room temperature in the dark and in flowing N_2. A Keithley 4200A semiconductor characterization system was used to measure impedance Z, parallel capacitance, C_P, and conductance, G_P, versus the top gate electrode voltage, V_G and frequency, f. For Z, C_P, and G_P versus f measurements, the gate voltage was applied with a superimposed sinusoid of 30 mV rms. The time over which frequency sweeps (1 kHz to 2 MHz) were taken was 284 s; this is relevant to the electrode polarization/charging state. For C, G–V measurements, V_G was swept from most negative towards positive values in steps of 0.1 V and at 10 mV/s unless otherwise noted. A 10-s hold was applied at the first measurement voltage before the start of data acquisition.

Transmission electron microscope (TEM) measurements of a Pd/Ti/PEO/*n*-Si capacitor were made in an FEI Titan 80-300 in bright-field mode to establish the physical thickness of spin-coated PEO. Focused ion beam milling (FEI Helios G4 Ux DualBeam) was used to prepare the TEM specimens, after an in situ deposition of a protective Ir/Pt cap. The average PEO thickness of the 8-krpm-coated wafer was determined over a lateral length of 932 nm (82 points) to obtain the physical thickness of 7.4 nm. Accumulation capacitance measurements were then calibrated to this thickness using a dielectric constant of 1.5. For the remainder of the sample set, capacitance measurements were used to determine the thickness with the same dielectric constant.

RESULTS AND DISCUSSION

Shown in Fig. 1a is the TEM cross section of a PEO film spun at 8 krpm, showing a thickness of 7.4 ± 1.4 nm. The PEO/Si interface is notably sharp, with most of the thickness variation arising from the upper PEO/metal interface. The measured frequency dependence of the impedance magnitude and phase are shown in Fig. 1b and c for five different PEO thicknesses. The impedance is well described by a simple capacitance, decreasing inversely with frequency, with a phase of approximately $-90°$. This ideal capacitance behavior is observed over more than two orders of magnitude. The measurement in Fig. 1 was made for an accumulation bias of 2 V; however, this ideal capacitive behavior is maintained for all bias conditions spanning the full range of voltages used in the C–V measurements. The impedance was also found to scale linearly with capacitor area, as expected.

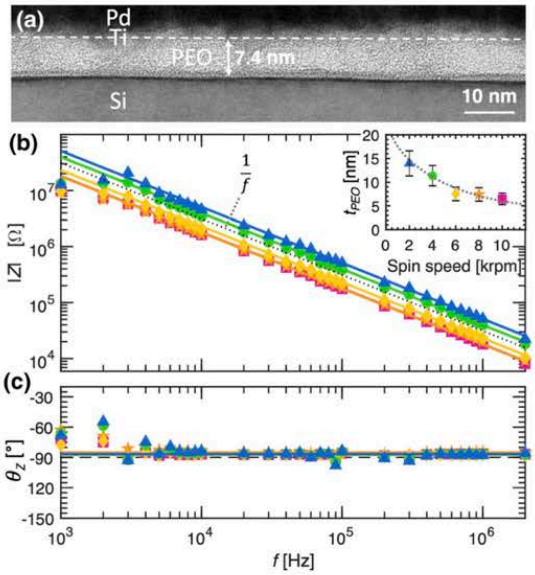

Fig. 1. (a) TEM image of a Pd/Ti/PEO/*n*-Si capacitor using PEO spun at 8 krpm, resulting in an ~ 7.4 nm film. (b) Frequency dependence of the impedance magnitude and (c) phase of 63 μm diameter MOS capacitors of different PEO thicknesses, biased in accumulation at V_G = 2 V. The dotted black line shows the excellent agreement of the measurements (markers) to an ideal capacitor's $|Z|$ with thickness t_{PEO} of 8 nm. Colored solid lines represent model fits to the measurements using a parallel-RC equivalent circuit. The inset shows PEO thickness versus spin speed extracted from the accumulation capacitances with ε_{PEO} = 1.5 (Color figure online).

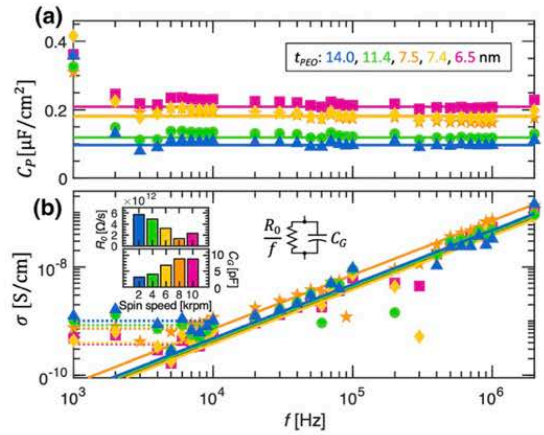

Fig. 2. Frequency dependence of the parallel (a) capacitance and (b) conductivity of 63 μm MOS capacitors with different PEO thicknesses biased in accumulation at V_G = 2 V. Dotted lines mark a region of dc conductivity. Solid lines represent model fits to the measurements (markers) from 5 k to 2 MHz, using the equivalent circuit in the inset of (b).

Using the measured physical thickness of 7.4 nm, the capacitor area, and the measured accumulation capacitance at 1 MHz, a relative dielectric constant, ε_{PEO} = 1.5, was obtained. This value is somewhat lower than reported by Nasir et al.[10], $\varepsilon_{PEO} \sim 2.3$, and measured on thick PEO films (600,000 g/mol; thickness, ~ 250–400 μm) between mm-diameter stainless steel electrodes. Using 1.5 for the dielectric constant, measured thicknesses versus spin speed were computed from accumulation capacitance measurements and plotted in the inset of Fig. 1b, with error bars given by geometrical uncertainties.

Given the ideal MOS *Z–f* dependence, we can accurately account for the frequency dependence by a parallel capacitance, C_P, and conductance, G_P. From the conductance, the conductivity, $\sigma = G_P t_{PEO}/A$, can be obtained, where A is the area. The resulting semi-logarithmic C_P–*f* and log–log σ–*f* plots are shown in Fig. 2a and b. As expected for a geometrical capacitor, the measured capacitances are substantially independent of frequency, with a slight increase observed below 3 kHz, which will be discussed later. The capacitance density with electrode areas measured by optical microscopy increases inversely with film thickness, again as expected.

The log–log σ–*f* plot in Fig. 2b shows a plateau at low frequencies, indicated by dotted lines. This frequency-independent dc conductivity, σ_{dc}, has been previously observed[11] in thicker PEO films. The plateau is followed by a region in which the conductivity increases directly in proportion to frequency spanning more than two decades. Such a frequency dependence of the conductivity is a property of many heterogeneous systems such as noncrystalline materials, including PEO.[12,13] In parallel conductance measurements when the impedance phase is close to − 90°, the measured real part of the complex impedance is much smaller than the imaginary part. The conductance of the ultrathin PEO capacitors exhibits a variability which is associated with the low signal level of the real impedance component. This is true here and in measurements to follow.

The simple capacitor behavior of $|Z|$, θ_Z, and C_P, along with the linear frequency dependence of σ for $f \geq \sim 5$ kHz can be modeled by a parallel *RC*, where C is a geometric MOS capacitance and R is a resistive element that has a linear frequency dependence, with the equivalent circuit shown in the inset in Fig. 2b. The solid lines in Figs. 1 and 2 show how closely this model represents the measured behavior (shown in markers) of Pd/Ti/PEO/*n*-Si MOS capacitors.

The measured *C–V* characteristics versus PEO thickness are shown in Fig. 3 and compared with simulated characteristics of an ideal MOS capacitor. The simulated *C–V* characteristic, Fig. 3a, is obtained using the heterostructure Poisson solver BandProf.[14] For the purposes of the simulation, a plausible band diagram is proposed using a PEO band gap from optical absorption measurements of

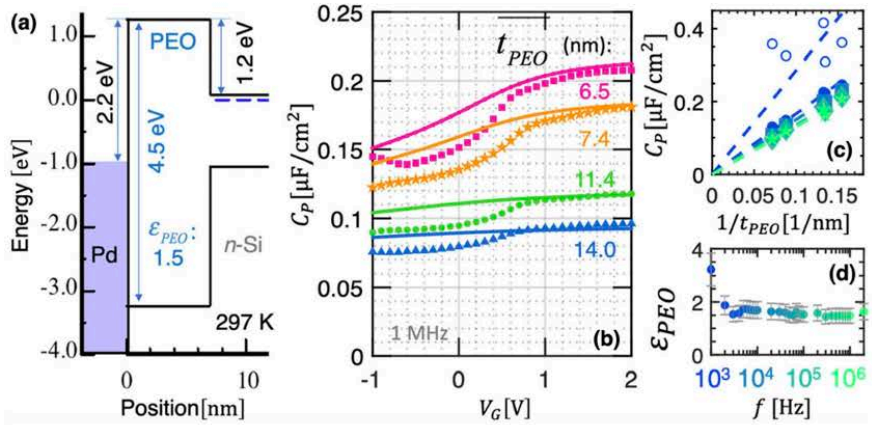

Fig. 3. (a) Energy band diagram of a Pd/PEO/*n*-Si capacitor biased at flatband and simulated using the heterojunction Poisson-solver BandProf [14]. (b) Capacitance density versus voltage in Pd/Ti/PEO/*n*-Si MOS capacitors versus thickness. Markers indicate measurements made at 1 MHz while biasing from depletion at − 1 V towards accumulation at 2 V. The solid lines are the simulations. (c) Accumulation capacitance density (at 2 V) versus inverse PEO thickness, extracted from TEM and *C–V* measurements at 1 kHz (open circles) and 2 k, 10 k, 100 k, and 1 MHz (filled colored circles). Dashed lines show the linear fit, $C = (\varepsilon_0\varepsilon_{PEO})/t_{PEO}$, used to extract ε_{PEO}. (d) Dielectric constant of PEO versus frequency (Color figure online).

4.5 eV.[15] The *n*-Si substrate has a doping of $N_D = 1 \times 10^{18}$ cm^{-3} and our measured value of $\varepsilon_{PEO} = 1.5$ is used. The metal/PEO barrier is placed near midgap, 2.2 eV, and a PEO/Si conduction band offset, ΔE_C, of 1.2 eV leads to a flatband voltage of approximately 1 V. This band diagram is consistent with the *C–V* measurements, Fig. 3b.

The simulated characteristics generally agree with the accumulation capacitance and minimum capacitance, but the transition to the minimum capacitance happens over a lower voltage span than the simulation predicts. This may arise from residual background ion conductivity in the films. PEO is known to absorb moisture, which raises its ionic conductivity.[16] Ionic polarization of the PEO surfaces can be expected to alter the capacitance transitions.

The accumulation capacitance density is plotted versus inverse PEO thickness in Fig. 3c. The linear relation and low frequency dispersion suggests a nearly ideal capacitive behavior across the various PEO thicknesses. The linear fit (dashed lines) of the measurements (markers) was used to extract the dielectric constant of PEO, which as Fig. 3d shows, has a weak dependence on frequency across most of the frequency range, with ε_{PEO} of 1.9 at 2 kHz and 1.5 at 1 MHz.

The detailed dependence of the capacitance and conductance characteristics versus slew rate of the gate voltage (using double sweeps) is shown in Fig. 4 for MOS capacitors spun at 4 krpm ($t_{PEO} \sim 11.4$ nm). The white noise reduction factor in the Keithley 4200A, i.e. filter factor, was varied from 1 to 100, and used to increment the measurement slew rate between 580 mV/s and 10 mV/s. For the PEO MOS capacitor on *n*-Si, the flatband voltage is approximately 1 V, and as bias increases

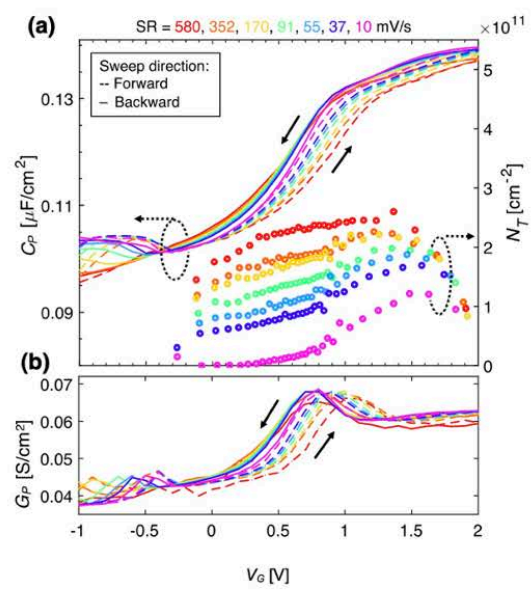

Fig. 4. Measured double-sweep slew-rate dependence of a Pd/Ti/PEO/*n*-Si MOS capacitor spun at 4 krpm ($t_{PEO} \sim 11.4$ nm) with a diameter of 63 μm. (a) Parallel capacitance, C_P, and density of trapped charge, N_T, versus voltage, and (b) parallel conductance, G_P, versus voltage. Forward and backward sweeps are indicated in dashed and solid lines, respectively.

electrons accumulate on the Si surface. The hysteresis observed in the capacitance as the voltage is ramped from − 1 V to 2 V and back corresponds to a bias which ranges from depletion to accumulation, Fig. 4a. Hysteresis in the characteristics in the voltage range above zero can be associated with charge trapping at or near the PEO/*n*-Si interface

and reaching a maxima near the flatband voltage, 1 V.

From the voltage shift in the double sweep measurement at fixed capacitance, the density of charge trapped at the PEO/n-Si interface can be estimated. In this portion of the C–V characteristic, the bias ranges from just below flatband to accumulation, so that electron traps in this region are likely located energetically near the conduction band edge. The charge responsible for the hysteresis ΔV_G at a particular C is $\Delta Q = C\Delta V_G$, and from ΔQ the density of mobile charge can be estimated as $N_T = \Delta Q/qA$, where q is the electron charge. This charge density, N_T, is plotted versus bias and slew rate in the lower right portion of Fig. 4a. Contributions to this hysteresis likely come from electronic traps, but mobile ions in the PEO cannot be ruled out. If the main contribution is electronic, the trap states are located near the Si conduction band edge. For the lowest slew rate, 10 mV/s, the peak in the mobile charge density occurs at voltages corresponding to accumulation biases. These traps are likely at the Si surface or in the surface border region of the PEO. The slew rate dependence can be explained if the traps have a higher capture rate than emission rate. High slew rates produce the greatest magnitude of accumulated fixed charge. The slower sweep rates allow the traps to fill and empty along with the bias, so that the voltage differences in the double sweep measurement are reduced. The highest accumulated charge is found to be $2.6 \times 10^{11}/\text{cm}^2$.

Considering the G–V measurement of Fig. 4b, two conductance peaks are observed and the slower slew rates shift the conductance peaks toward smaller gate voltages. The conductance peaks measured at 10 mV/s are centered around $-$ 0.5 V and 0.8 V. The upper peak at around 0.8 eV corresponds to a bias near accumulation bias and is likely due to state filling near the conduction band edge of Si. The peak at around $-$ 0.5 V is still in the upper half of the Si band gap, as band diagram simulations indicate the valence band is not reached until a voltage of nearly $-$ 4 V. The energetic position of the conductance peak near the conduction band edge suggests the presence of shallow donor traps.

The impedance–frequency characteristics of PEO capacitors with and without $CsClO_4$ are compared in Fig. 5, here using p-Si substrates. Open and filled markers indicate the measurements of PEO and PEO:$CsClO_4$ capacitors, respectively, biased in accumulation. As was observed in the n-Si substrates, the capacitors without $CsClO_4$ exhibit an essentially ideal characteristic, with inverse frequency dependence and $-$ 90° phase shift. With the added salt, the impedance magnitude decreases due to the increase in ionic conductivity. In contrast to prior published studies[10,13] on thick PEO capacitors, the measurements here show an impedance which is more capacitive than conductive. Where the phase reaches 45º, the real and imaginary parts of the impedance become equal. This again is a consequence of the reduced impedance of the PEO:$CsClO_4$ due to the ionic conductivity of the film.

The PEO and PEO:$CsClO_4$ capacitor data is modeled using the simple equivalent circuits shown in the insets of Fig. 5a and parameters given in (c–f). The resulting model fits are shown in Fig. 5a and b in solid and dashed lines for films without and with $CsClO_4$, respectively. Here our aim is to see to what extent the simplest lumped element model can capture the responses which relate to ion transport and the electrode polarization. For PEO capacitors without $CsClO_4$ on n and p-Si, the essential physics is captured by a parallel RC circuit, where the capacitive element is the geometric capacitance and the resistive element is a frequency-dependent resistor, R_0/f.

The PEO:$CsClO_4$ capacitors can be modeled by an equivalent circuit with three RC loops in series (inset of Fig. 5a). One loop, consisting of capacitance C_B in parallel with resistance R_B, represents the charge transport in the bulk of the PEO film.[18] The second and third RC loops represent the polarization at the metal and Si electrodes with the capacitor, C_{EDL}, representing an electric double layer (EDL) capacitance. This capacitance is shunted by a conductance that represents charge transfer between the PEO film and the electrodes due to ionic and/or electronic processes. This resistance R has previously been referred to as a charge transfer resistance at the solid electrolyte's interface with partially blocking electrodes, and it produces a plateau in the modeled conductivity at low frequencies.[18] The measurements reported here are for biases sufficiently low that the measurements are reversible and repeatable.

The expected bulk resistance, R_B, and capacitance, C_B, of PEO:$CsClO_4$ capacitors are marked by circles in Fig. 5c and d, respectively. The anticipated bulk capacitance and resistance were calculated as $C_B = \varepsilon_0\varepsilon_{PEO}A/t_{Bulk}$ and $R_B = \rho t_{Bulk}/A$, considering $\varepsilon_{PEO} = 1.5$, the resistivity of ~ 1 μm thick PEO:$CsClO_4$, $\rho \sim 5.67 \times 10^6$ Ω-cm,[17] and the thickness of the bulk, $t_{Bulk} = t_{PEO} - 2t_{EDL}$. The EDL thickness t_{EDL} is estimated from the average EDL capacitance at the PEO/electrode interface, $C_{EDL} = \varepsilon_0\varepsilon_{PEO}A/t_{EDL}$, obtained from the circuit parameter $C_E = C_{EDL}/2$. The expected R_B and C_B are within the same order of magnitude as the values obtained from the circuit model fits of PEO:$CsClO_4$. For both PEO and PEO:$CsClO_4$ capacitors, R_B drops and the C_B increases with decreasing film thickness as can be expected. Capacitors with $CsClO_4$ have a higher C_B, since the added presence of the EDL capacitors at the electrode/PEO interfaces reduces the bulk thickness compared to PEO films without $CsClO_4$.

The EDL capacitance density estimated from the model fit, $2C_E/A$ is ~ 1 μF/cm^2 and may be considered small for an EDL capacitance; prior

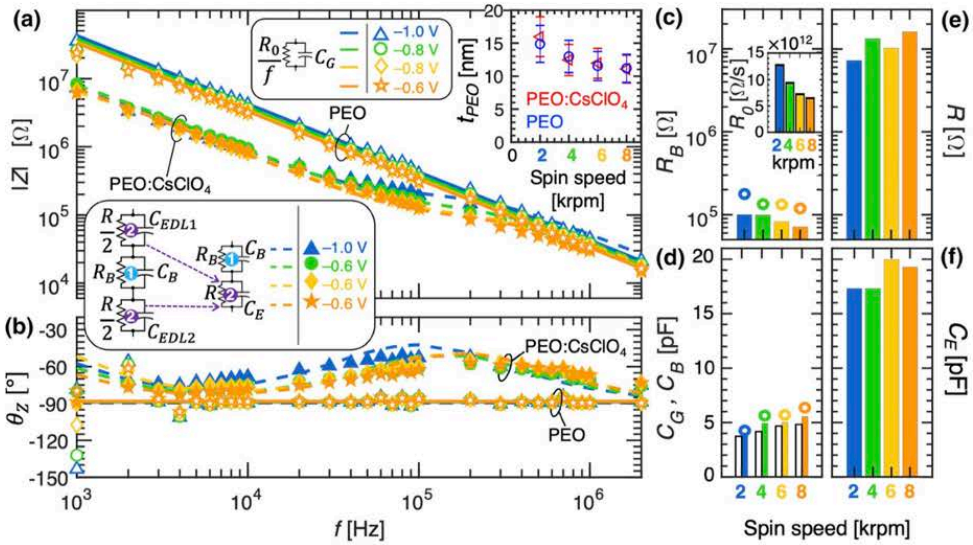

Fig. 5. Impedance–frequency dependence comparing Pd/Ti/PEO:$CsClO_4$/*p*-Si and Pd/Ti/PEO/*p*-Si MOS capacitors. (a) Impedance magnitude, $|Z|$, and (b) phase, θ_Z, versus frequency. The measurements of PEO and PEO:$CsClO_4$ capacitors are indicated with open and filled markers, respectively. The capacitors were biased in the range − 0.6 to − 1 V corresponding to accumulation biases. Solid and dashed lines represent *RC* model fits to the PEO and PEO:$CsClO_4$ capacitor data, respectively, using the equivalent circuits shown in the insets of (a) and parameters given in (c–f), with the geometrical capacitances computed from the physical geometry with $\varepsilon_{PEO} = 1.5$. The boxed inset in (a) shows the electrical thickness versus spin speed of PEO without (blue circle) and with (red left pointing triangle) $CsClO_4$. (c) Bulk resistance R_B; inset shows the R_0 parameter of the frequency-dependent resistance. (d) Geometric capacitance C_G and bulk capacitance C_B for PEO (white bars) and PEO:$CsClO_4$ (colored bars). (e) Resistance *R* and (f) capacitance $C_E = C_{EDL1}C_{EDL2}/(C_{EDL1} + C_{EDL2})$ at the electrodes. Circles in (c) mark the expected R_B extrapolated from thick PEO:$CsClO_4$ ($t_{PEO} \sim 1$ μm) discussed in prior work.[17] Circles in (d) indicate the C_B expected from the same bulk thickness used in the extrapolation of R_B. The left and right axes have the same resistance and capacitance scales (Color figure online).

measurements in this solid polymer electrolyte yielded 4 μF/cm^2.[19] The lower C_{EDL} in these ultra-thin PEO:$CsClO_4$ capacitors is likely due to the roughness of the Pd/Ti/PEO top electrode, see Fig. 1a, in contrast with the flatter PEO/Si bottom electrode. The resulting difference in the space-charge separation at the top and bottom electrodes can lead to different EDL capacitances at each electrode, C_{EDL1} and C_{EDL2}. These two capacitances in series form the capacitor C_E in the inset of Fig. 5a. If at the flatter PEO/Si electrode C_{EDL1} is the expected 4 μF/cm^2, while at the rougher Pd/Ti/PEO electrode C_{EDL2} is slightly lower, say 1.3 μF/cm^2, the total capacitance density C_E would be 1 μF/cm^2. Thus, the lower than expected C_{EDL} may arise from non-uniformities in the top-electrode.

Again, the *Z–f* data of PEO and PEO:$CsClO_4$ capacitors is used to calculate the parallel capacitance density, C_P, from which the effective dielectric constant, ε_r, can be extracted, Fig. 6. Measurements are indicated with markers, while the *RC* models are indicated with solid and dotted lines in Fig. 6a for PEO and PEO:$CsClO_4$, respectively. As with the *n*-Si devices, the capacitance and dielectric constant of PEO without $CsClO_4$ on *p*-Si are constant across more than two decades. The C_P and ε_r of devices with $CsClO_4$ are the same as in PEO devices without $CsClO_4$ at high frequencies. However, at frequencies below ~ 500 kHz, C_P and ε_r increase

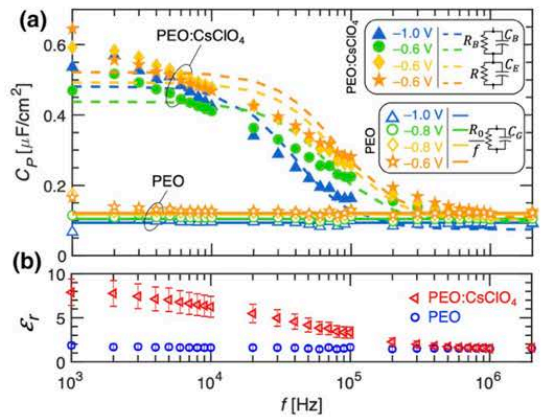

Fig. 6. Measured frequency dependence comparing Pd/Ti/PEO:$CsClO_4$/*p*-Si and Pd/Ti/PEO/*p*-Si MOS capacitors: (a) parallel capacitance, C_P, and (b) dielectric constant, ε_r, of 63 μm MOS capacitors of various PEO thicknesses biased between − 0.6 V and − 1 V. ε_r was extracted from a linear fit between the parallel capacitance density and inverse thickness. For reference, in (a) solid and dashed lines indicate the one- and two-RC loop models, for PEO and PEO:$CsClO_4$, respectively as shown in the insets, with parameters plotted in Fig. 5.

with decreasing frequency, as the two-*RC* model also shows, reaching a maximum at 1 kHz of

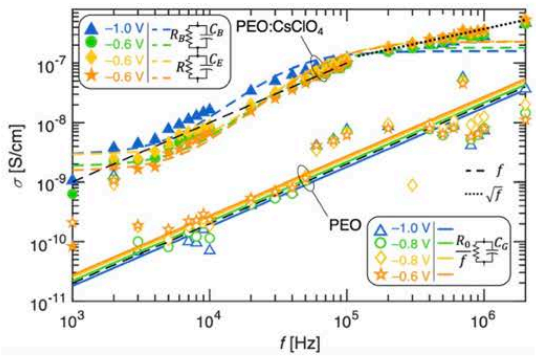

Fig. 7. Measured frequency dependence comparing Pd/Ti/PEO:$CsClO_4$/*p*-Si and Pd/Ti/PEO/*p*-Si MOS capacitors: conductivity, σ, of 63 μm MOS capacitors of various PEO thicknesses biased between − 0.6 V and − 1 V. For reference, the one- and two-*RC* loop model, shown in the insets with parameters plotted in Fig. 5, are indicated in colored solid and dashed lines for PEO and PEO:$CsClO_4$, respectively. Dashed and dotted black lines indicate a linear and square-root σ–f relation (Color figure online).

$C_P \sim 0.6$ μF/cm^2 and $\varepsilon_r \sim 8.0$ for PEO:$CsClO_4$ versus ~ 0.2 μF/cm^2 and 1.9 for PEO without $CsClO_4$.

The frequency dependence of the conductivity of PEO and PEO:$CsClO_4$ capacitors on *p*-Si wafers is shown in Fig. 7, where measurements and circuit model fits are indicated in colored markers and solid or dashed lines, respectively. PEO devices without $CsClO_4$ have a conductivity roughly increasing linearly with frequency above 10 kHz. There are some variations in σ due to the closeness of θ_Z to the ideal − 90°, as seen in Fig. 5b; that is, the measured real component of the impedance, used to calculate σ, is very small, leading to some variability in the calculation of the real part of the impedance. The linear σ–f trend measured in PEO without $CsClO_4$, shown in open markers, is reproduced by the one-*RC* equivalent circuit, indicated by solid lines, due to the presence of a frequency dependent resistor, R_0/f.

The measured conductivity of PEO:$CsClO_4$ capacitors, shown in solid markers, is between roughly 1 to 2 orders of magnitude higher than in PEO without $CsClO_4$. The frequency exponent n in the σ–f^n relation changes value at around 100 kHz, below which it is relatively linear and above which σ goes roughly as the square-root of f, as shown in black dashed and dotted lines in Fig. 7. These n values are within the limits of 0 and 1 reported in the literature for polymers, with various fractional values representing different ion conduction processes.[8]

The two-*RC* model for PEO:$CsClO_4$ captures the approximate frequency in which n changes values. Its bulk resistor, R_B, is orders of magnitude lower than the frequency-dependent resistor, R_0/f, describing the bulk of PEO without $CsClO_4$. This again shows that the addition of $CsClO_4$ increases the conductivity of the PEO bulk. In these two separate conductivity ranges for PEO and PEO:$CsClO_4$ there may be different ion conduction mechanisms involved, leading to different σ–f^n relations, as can be expected from the additional presence of Cs^+ and ClO_4^- ions, rather than only PEO's background ions, such as OH^- and H^+.

The increase in dielectric constant, Figs. 3d and 6b, and the decrease in σ, Figs. 2b and 7, at low frequencies observed in PEO and to a greater degree in PEO:$CsClO_4$ capacitors has been reported in bulk PEO and other ion-conducting materials, and it is largely attributed to incipient electrode charge polarization effects that strengthen at even lower frequencies.[11,20] At high frequencies, the conductivity is governed by ion drift in the bulk[18] of the PEO film. With increasing frequency, the conductivity increases approximately linearly and the dielectric constant tends to level off. The low-frequency σ and dielectric constant spectra are related to the accumulation of ions at the PEO/electrode interface, producing space-charge layers across which most of the electric field is dropped, while the PEO bulk experiences a much lower electric field. This causes the dielectric constant to increase and σ to drop with decreasing frequency, at least until reaching a σ plateau due to the partially, rather than fully, blocking nature of the electrodes.[18]

CONCLUSION

The impedance frequency properties of PEO and PEO:$CsClO_4$ have been characterized at thicknesses from 6 nm to 19 nm, thinner than prior reports. The properties of PEO without $CsClO_4$ are well described by an oxide that has a band gap of approximately 4.5 eV, metal-PEO barrier of 2.2 eV, and PEO/Si band offset of 1.2 eV. From the *C*–*V* hysteresis of PEO capacitors without $CsClO_4$ and assuming its main contributions are electronic, the trap density is estimated to exceed approximately 2.6×10^{11}/cm^2. The extracted static dielectric constant of PEO without $CsClO_4$ in ultrathin films is ~ 1.6. Adding $CsClO_4$ increases the parallel capacitance and dielectric constant for frequencies below 500 kHz, due to the polarization of ions at the interface of PEO with the electrodes. Adding $CsClO_4$ also increases the conductivity of the films across the full frequency range. Both PEO and PEO:$CsClO_4$ capacitors had a roughly linear frequency dependence, with the latter transitioning to a square-root conductivity–frequency dependence at $\sim$ 100 kHz.

Simple equivalent circuit models capture the overall impedance versus frequency trends. For PEO without $CsClO_4$, a single *RC* loop represents the ion transport in the bulk of the film, with the resistor having a simple inverse-frequency dependence. When $CsClO_4$ is present, the charge transfer resistance and an electrode polarization capacitance is sufficient to explain the measured response. The addition of $CsClO_4$ reduces the bulk resistance by

orders of magnitude compared to PEO without $CsClO_4$. Ultrathin PEO films at the decananometer scale are shown here to be insulating and to exhibit impedance–frequency behavior similar to thicker films even at the micron scale. No impediments are found to using PEO:$CsClO_4$ at scales commensurate with VLSI technology for deep learning and neuromorphic applications.

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CONFLICT OF INTEREST

The authors declare no conflict of interest.

REFERENCES

1. E.H. Nicollian and J.R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (New York: Wiley, 1982), p. 432.
2. W. Haensch, T. Gokmen, R. Puri, in *Proceedings of the IEEE* (2019), p. 108.
3. R. Islam, H. Li, P.-Y. Chen, W. Wan, H.-Y. Chen, B. Gao, H. Wu, S. Yu, K. Saraswat, and H.-S. Philip Wong, *J. Phys. D Appl. Phys.* 52, 1 (2019).
4. D.K. Efetov and P. Kim, *Phys. Rev. Lett.* 105, 2 (2010).
5. J. Chen, C.D. Frisbie, and F.S. Bates, *J. Phys. Chem. C* 113, 10 (2009).
6. N.S.T. Do, D.M. Schaetzl, B. Dey, A.C. Seabaugh, and S.K. Fullerton-Shirey, *J. Phys. Chem. C* 116, 40 (2012).
7. K. Ueno, H. Shimotani, H. Yuan, J. Ye, M. Kawasaki, and Y. Iwasa, *J. Phys. Soc. Jpn.* 83, 3 (2014).
8. C. Alessandri, S. Fathipour, H. Li, I. Kwak, A. Kummel, M. Remškar, and A.C. Seabaugh, *IEEE Trans. Electron Devices* 64, 12 (2017).
9. P. Paletti, R. Yue, C. Hinkle, S.K. Fullerton-Shirey, and A. Seabaugh, *npj 2D Mater. Appl.* 3, 1 (2019).
10. N.H.A. Nasir, C.H. Chan, H.-W. Kammer, L.H. Sim, and M.Z.A. Yahya, Macromol. Symp. 290, 46–55 (2010).
11. A.A. Khamzin, I.I. Popov, and R.R. Nigmatullin, *Phys. Rev. E* 89, 3 (2014).
12. S.K. Chaurasia, A.L. Saroj, S.V.K. Shalu, A.K. Tripathi, A.K. Gupta, Y.L. Verma, and R.K. Singh, *AIP Adv.* 5, 7 (2015).
13. C.H. Chan, H.-W. Kammer, L.H. Sim, S.N.H.M. Yusoff, A. Hashifudin, and T. Winie, *Ionics* 20, 2 (2014).
14. BandProf, W.R. Frensley, UT Dallas, https://personal.utdallas.edu/~frensley/hlts/bandprof.html.
15. V.M. Mohan, V. Raja, P.B. Bhargav, A.K. Sharma, and V.V.R.N. Rao, *J. Polym. Res.* 14, 4 (2007).
16. S.K. Fullerton-Shirey, L.V.N.R. Ganapatibhotla, W. Shi, and J.K. Maranas, *J. Polym. Sci. Polym. Phys.* 49, 21 (2011).
17. P. Paletti, M.A. Heidarlou, K.G. Serrano, C. Alessandri, and A. Seabaugh, in *Device Research Conference (DRC)* (2019), p. 53.
18. J.C. Dyre, P. Maass, B. Roling, and D.L. Sidebottom, *Rep. Prog. Phys.* 72, 4 (2009).
19. H. Xu, S. Fathipour, E.W. Kinder, A.C. Seabaugh, and S.K. Fullerton-Shirey, *ACS Nano* 9, 5 (2015).
20. A. Telfah, M.M. Abdul-Gader Jafar, I. Jum'h, M.J.A. Ahmad, J. Lambert, and R. Hergenröder, *Polym. Adv. Technol.* 29, 7 (2018).

APPENDIX D:

DYNAMICS OF FERROELECTRIC AND IONIC MEMORIES - PHYSICS AND APPLICATIONS

2019 IEEE 13th International Conference on ASIC (ASICON)

Dynamics of Ferroelectric and Ionic Memories: Physics and Applications

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Abstract

Ferroelectric (FE) and solid polymer electrolytes (SPEs) are being explored for memory and for a variety of purposes in transistors. While considering the dynamics of emerging memories, we note some interesting implications for transistors and transistor memories. In this paper we consider the dynamics of subthreshold swing (SS) in transistors and show that under certain conditions SS can be lowered due to the delay associated with their complex impedance. We show that even a conventional metal oxide semiconductor field-effect transistor (MOSFETs) can exhibit a dynamic SS, lowered by introducing a series resistance in the gate. We show that the when the gate dielectric has a complex response, SS can be decomposed into static and dynamic factors with the static factor given by the usual thermal SS and the dynamic factor related to dynamic gate amplification. In the measurement of SS, slew rate and slew direction can be readily utilized to reveal the SS dependence on dynamics.

1. Introduction

FEs and SPEs have interesting similarities and differences. Both exhibit charging dynamics controlled by ionic polarization. In FEs the polarization switches abruptly (but not instantaneously) between plus and minus surface charge densities at a coercive electric field, while in SPEs (electrically insulating, ion conducting polymers) the polarization is continuously dependent on electric field. Both FE and SPEs can yield high surface charge densities (10^{13}–10^{14} cm^{-2}). FE polarization is nonvolatile while SPE polarization is volatile, requiring a refresh. The partial polarization of polycrystalline FEs can be used for analog memory with the resolution set by the FE grain size. In SPEs the memory resolution does not have a domain size limitation and can reach ionic dimensions (~1 nm^2). Switching speed has been shown to be less than 10 ns in FE hafnium zirconate (HZO, 10 nm) [1, 2]. In SPEs data is lacking at comparable film thicknesses. Molecular dynamic simulations of poly-ethylene oxide:lithium perchloride (PEO:$LiClO_4$) with a film thickness of 15 nm and for an applied field of 0.1 V/nm indicate the formation time of an electric double layer (EDL) to occur in under a nanosecond [3].

In transistor structures, FEs are being inserted to increase current drive [4], lower subthreshold swing [5], to add reconfigurability [6], and to make new kinds of memory [7, 8]. In capacitor structures the partial polarization of FE HZO has been shown to be well suited for analog memory [9, 10]. These capacitors can be used with transistors to read and write [11] or can be implemented as FE tunnel junctions and read out in resistive crossbar arrays [12, 13]. The temporal response of polycrystalline HZO depends on the previous history of the switching and methods for modeling this dependence have been discussed, e.g. [14, 15].

Ionic polymers also have a wide range of applications in both two-terminal and transistor configurations: to enable reconfigurability [16, 17], to form Esaki tunnel junctions [18], and for memory [19, 20]. Understanding the dynamics is key to determining the functions and application of these technologies [21, 22].

2. Subthreshold swing

The subthreshold swing of a FET is typically defined as a static property, SS = $dV/d\log(I_D)$, where V is the input voltage applied to the gate and I_D is the drain current. If there is a time-dependence this can be written explicitly, where the instantaneous slew rate is $r = dV/dt$.

$$SS = \frac{dV/dt}{d\log(I_D)/dt} = \frac{r}{d\log(I_D)/dt}, \qquad (1)$$

Consider a circuit with a simple gate delay represented in Fig. 1, where the resistance R represents an ionic or

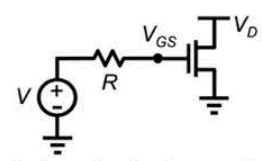

Figure 1. Equivalent circuit of a complex dielectric in which the voltage V_{GS}, controlling the intrinsic transconductance of the MOSFET, is delayed with respect to the input voltage V. The n-MOSFET is modeled using a 90 nm predictive technology model [23].

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switching dissipation in the gate of a MOSFET. From Eq. (1) and Fig. 1, it follows that

$$\frac{d\log(I_D)}{dt} = \frac{d\log(I_D)}{dV_{GS}}\frac{dV_{GS}}{dt} = \frac{dV_{GS}/dt}{\ln(10)kT/q}, \qquad (2)$$

where $d\log(I_D)/dV_{GS}$ is the usual static SS given by $\log(10)kT/q$, with k being Boltzmann's constant, T temperature and q electron charge. The dynamic SS can then be written

$$SS = \frac{r}{dV_{GS}/dt}\ln(10)\frac{kT}{q} = \frac{dV}{dV_{GS}} \times 60 \text{ mV/dec at 300 K.} \qquad (3)$$

The swing is seen to consist of the usual static swing with a dynamic factor depending on the instantaneous excitation slew rate r and the internal slew rate dV_{GS}/dt. When the internal slew rate exceeds the excitation slew rate, SS can be less than 60 mV/decade. Because the transistor gate capacitance changes from low to high as the transistor goes from depletion to inversion, dV_{GS}/dt and dV_{GS}/dV depend on slew direction. Alternatively, the dynamic factor $r/(dV_{GS}/dt)$ can be written as dV/dV_{GS} which says that SS lowering occurs when voltage amplication is obtained at the gate terminal.

3. Time response of an ionic polymer capacitor

Measurements of the current-voltage characteristics of a metal/SPE/metal structure are shown in Fig. 2, where the SPE is PEO:$CsClO_4$. In the PEO, $CsClO_4$ dissolves into Cs+ and ClO_4−. The thickness of the polymer for this case is ~1 µm and the capacitor diameter is 120 µm. Details of the fabrication and structure are given in [21, 22]. The measured current vs. time is shown in Figs. 2(b), for pure PEO, and 2(c), for PEO:$CsClO_4$, in response to a triangle input waveform. The time

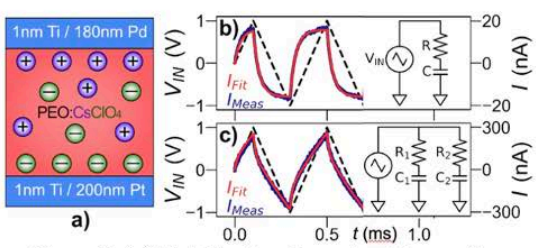
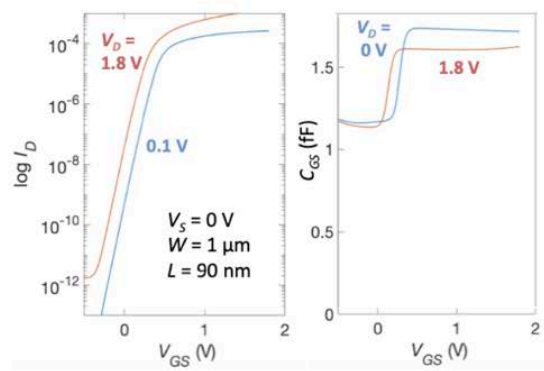


Figure 2. (a) Metal/ionic polymer/metal capacitor. Current transients in response to a triangle input waveform for (a) PEO and (b) PEO containing Cs+ and ClO_4− ions. These cases are accurately represented by the circuit insets shown.

response of both capacitors can be accounted for by a series RC circuit, where R represents the bulk ionic resistance and C represents the EDL capacitance of the metal/PEO interfaces. The pure PEO is least-squares fitted to extract the RC elements and the agreement with measurements for the fit is excellent. In the pure PEO the ionic response is attributed to H+ and OH− from absorbed water. In the PEO:$CsClO_4$ case, a second RC branch is needed to account for the ionic response of the Cs+ and ClO_4− ions. These measurements confirm that a simple gate delay can be expected with an SPE. This is what motivates our investigation of the MOSFET with a gate series resistance. We will show that when the RC time constant and the measurement slew rate are close, SS lowering results.

4. 90 nm MOSFET model

The SPICE model of a 90 nm n-MOSFET is shown in Fig. 3. This predictive technology model [23] has an SS of approximately 74 mV/decade. The capacitance density at C_{GS} = 1 fF is 1.1 µF/cm^2. Gate capacitance C_{GS} has C_{MAX}/C_{MIN} of ~1.5 between inversion and depletion.



(a) (b)

Figure 3. (a) Transfer characteristics of a 90 nm node MOSFET. (b) Capacitance-voltage characteristics of the same PTM 90 nm n-MOSFET.

A resistance R = 1 TΩ is used in the gate, so that the voltage across the MOSFET gate, V_{GS}, is delayed by RC_{GS} ~1 ms, with respect to the input voltage V. Consider the relationship shown in Fig. 4(a), between an input triangle wave applied at V and the resulting gate voltage V_{GS}. For a sufficiently slow ramp, the gate capacitance fully charges and the applied voltage V and V_{GS} are identical. This is labeled the quasistatic case QS. For the forward sweep FS, to 1.8 V, V_{GS} lags the input voltage V. When V = 2 V, V_{GS} = 1.1 V and when V starts the reverse sweep RS, the voltage across the input is still charging C_{GS} even though the input slew is negative. On the RS in Fig. 4(a) the slope gets steeper as V decreases,

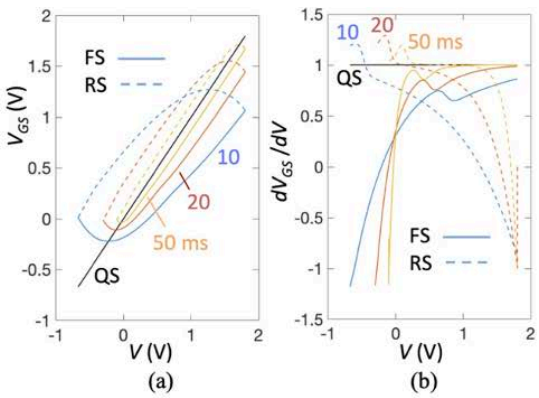


Figure 4. (a) V_{GS} vs. input voltage V for a triangle wave with a period of 10, 20, or 50 ms. This triangular wave is the second of a 2-period sequence. (b) Dynamic factor, dV_{GS}/dV vs. V_{GS}. When the dynamic factor is greater than one, SS is lowered as predicted by Eq. (1).

and the MOSFET transitions from inversion to depletion. This results in a speed-up of the discharge of C_{GS}, which acts to lower SS. This voltage loop is the second of two, chosen because after one loop the results are stable. Figure 4(b) plots the derivative dV_{GS}/dV vs. the input voltage V, which reveals the voltages over which the SS becomes greater than. This is the region where there is a dynamic lower of SS.

The transfer characteristics of the n-MOSFET with $R = 1$ TΩ, $W = 1$ μm, and $L = 90$ nm vs. triangle wave period, 10, 20, and 50 ms, are shown in Fig. 5(a). For a sufficiently slow sweep, the gate voltage follows the input voltage and there is no hysteresis in the double sweep triangle wave measurement. This is the black line labeled QS. For the forward sweep of the triangle wave (solid lines), V_{GS} lags the input waveform V and the drain current similarly lags. The reverse sweep (dashed lines) get steeper and steeper as the sweep period increases from 10 to 50 ms.

SS vs. log(I_D) is plotted in Fig. 5(b) for the forward sweep (upper) and reverse sweep (lower) directions. The QS black solid lines indicate the static SS of the transistors. For the MOSFET the series gate resistor can lead to a reduction in SS on the FS and a lowering of SS on the RS. This finding of gate delay dependent SS was reported first in [21] and shown to explain measured sub-60-mV/dec swing observed in a WSe_2 FET. These results have been extended through measurements and analysis in [22]. Here we show that even the MOSFET with a gate delay can exhibit SS depending on measurement slew rate.

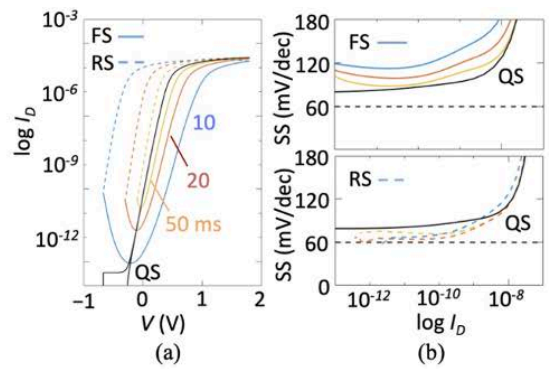


Figure 5. (a) Transfer characteristics, log(I_D) vs. input voltage V, comparing the quasistatic measurement (QS) against three triangle wave input ramps with $R = 1$ TΩ, and slew periods, 10 to 50 ms (for $RC_{GS} = 1$ ms). (b) SS vs. log(I_D) from forward sweep FS (upper) and reverse sweep RS (lower) transfer characteristics.

The choice of $R = 1$ TΩ has no special significance in this example. It just sets the time constant to for this MOSFET. Lowering R by a factor x just shortens the slew periods by the same factor to obtain the same result.

5. Discussion

The dynamics of ferroelectric switching and its effect on SS continues to be modeled and investigated [24 and references therein]. Saha et al. showed that subthermal SS can arise from delay associated with the complex impedance of a FE [25]. Recently Wang et al. presented a study of FE FETs [26], showing that polarization dynamics can be the origin of steep SS and that matching of measurement conditions to the polarization switching can be used to achieve the steepest SS. Thus FEs, SPEs, and other emerging complex dielectrics have fundamental similarities.

6. Summary

Ferroelectric and solid polymer electrolytes have complex impedances. The real parts of the impedance are represented by resistances, which account for dissipation and introduce delay. In transistor gates this delay leads to a dynamic multiplication of the gate voltage for certain input slew periods. This can be seen even in a conventional MOSFET with a series gate resistance. The dynamic multiplication factor is given by the ratio of the instantaneous excitation slew rate to the internal slew rate driving the transistor transconductance. SS can be increased or decreased as a result of this slew dependent factor. Alterations to SS are shown to arise naturally from delay.

References

[1] W. Chung, M. Si, P. R. Shrestha, J. P. Campbell et al., *2018 IEEE Symp. on VLSI Technology*, p.89.

[2] M. Si, X. Lyu, P. R. Shrestha, X. Sun, H. Wang, K. P. Cheung, and P. D. Ye, *Appl. Phys. Lett.*, (2019).

[3] K. Xu, M. M. Islam, D. Guzman, et al., *ACS Appl. Mater. Interfaces,* 10, p.43166 (2018).

[4] Z. Zhang, G. Xu, Q. Zhang, Z. Hou, J. Li, Z. Kong et al., *IEEE Electron Dev. Lett.,* 40, p.367 (2019).

[5] D. Kwon, K. Chatterjee, A. J. Tan, A. K. Yadav et al., *IEEE Electron Dev. Lett.* 39, p.300 (2018).

[6] V. Sessi, H. Mulaosmanovic, R. Hentschel, S. Pregl et al., *2018 IEEE Int. Conf. on Nanotechnology*.

[7] M. Jerry, P.-Y. Chen, J. Zhang, P. Sharma, K. Ni et al., *2017 IEEE Int. Electron Devices Mtg.,* p.6.2.1.

[8] S. Mueller, *2018 IEEE Int. Memory Workshop*.

[9] E. W. Kinder, C. Alessandri, P. Pandey, G. Karbasian et al., *2017 Device Research Conf.*

[10] C. Alessandri, P. Pandey, A. Abusleme et al., *IEEE Electron Device Lett.,* 39, p.1780 (2018).

[11] S. J. Kim, J. Mohan, C. D. Young, L. Colombo, J. Kim et al., *2018 IEEE Int. Memory Workshop.*

[12] R. Berdan, T. Marukame, S. Kabuyanagi, K. Ota et al., *2019 Symp. VLSI Technology*, p.T2-4.

[13] M. M. Frank, E. A. Cartier, K.-L. Lee et al., *2018 IEEE Semicon. Interface Specialists Conf.,* p.7.12.

[14] C. Alessandri, P. Pandey, and A. C. Seabaugh, *2018 IEEE Int. Electron Devices Mtg.,* p.16.2.1.

[15] C. Alessandri, P. Pandey, A. Abusleme et al., *IEEE Trans. Electron Dev.*, 66, p.3527 (2019).

[16] S. Fathipour, P. Paletti, S. Fullerton-Shirey, and A. Seabaugh, *2016 Device Research Conf.*

[17] C. Alessandri, S. Fathipour, H. Li, I. Kwak et al., *IEEE Trans. Electron Dev.,* 64, p.5217 (2017).

[18] P. Paletti, R. Yue, C. Hinkle et al., *Nature 2D Materials and Applications*, 3, p.603 (2019).

[19] K. Xu, H. Lu, E. W. Kinder, A. Seabaugh, and S. K. Fullerton-Shirey, *ACS Nano*, 11, p.5453 (2017).

[20] J. Tang, D. Bishop, S. Kim, M. Kopal, T. Gokmen et al., *2018 Int. Electron Devices Mtg.*, p.13.1.1.

[21] P. Paletti, M. Asghari Heidarlou, K. Gonzalez-Serrano, C. Alessandri et al., 2019 *Dev. Res. Conf.*

[22] P. Paletti, K. Gonzalez-Serrano, and A. Seabaugh, *IEEE Trans. Electron Dev.,* submitted 2019.

[23] ASU Predictive Technology Model, 90 nm NMOS, http://ptm.asu.edu/modelcard/90nm_bulk.txt.

[24] S.-C. Chang, U. E. Avci, D. E. Nikonov et al., *Phys. Rev. Applied*, 9, p.014010 (2018).

[25] A. K. Saha, S. Datta, and S. K. Gupta, *J. Appl. Phys.*, 123, p.105102, (2018).

[26] H. Wang, M. Yang, Q. Huang, K. Zhu et al., *2018 IEEE Int. Electron Devices Mtg.*, p.31.1.1.

APPENDIX E:

RESOLUTION ENHANCEMENT OF TRANSMISSION ELECTRON MICROSCOPY BY SUPER-RESOLUTION RADIAL FLUCTUATIONS

Applied Physics Letters ARTICLE scitation.org/journal/apl

Resolution enhancement of transmission electron microscopy by super-resolution radial fluctuations

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ABSTRACT

Super-resolution fluorescence microscopy techniques have enabled dramatic development in modern biology due to their capability to discern features smaller than the diffraction limit of light. Recently, super-resolution radial fluctuations (SRRF), an analytical approach that is capable of generating super-resolution images easily without the need for specialized hardware or photoswitchable fluorophores, has been presented. While SRRF has only been demonstrated on fluorescence microscopes, in principle, this method can be used to generate super-resolution images on any imaging platforms with intrinsic radial symmetric point spread functions. In this work, we show that SRRF can be utilized to enhance the resolution and quality of transmission electron microscopy (TEM) images. By including an image registration algorithm to correct for sample drift, the SRRF-TEM approach substantially enhances the resolution of TEM images of three different samples acquired with a commercial TEM system. We quantify the resolution improvement in SRRF-TEM and evaluate how SRRF parameters affect the resolution and quality of SRRF-TEM results.

Fluorescence microscopy is essential in biomedical research as it allows researchers to observe specifically labeled cellular structures in their native physiological states.[1] However, due to the diffraction of light, the resolution of fluorescence microscopy is limited to hundreds of nanometers.[2] To discern features smaller than the diffraction limit in living cells, super-resolution microscopy techniques, notably stimulated emission depletion (STED) microscopy,[3,4] photoactivated localization microscopy (PALM),[5] stochastic optical reconstruction microscopy (STORM),[6] structured illumination microscopy (SIM),[7,8] and super-resolution optical fluctuation imaging (SOFI),[9] have been demonstrated. Although these established super-resolution techniques have enabled dramatic development in modern biology, their implementations often require specialized, complicated optical setups or photoswitchable fluorophores, which are not accessible to many labs. Recently, super-resolution radial fluctuations (SRRF) has been demonstrated.[10] Unlike the established super-resolution methods, SRRF does not require specialized hardware (e.g., depletion, structured illumination lasers, and high-speed cameras) or photoswitchable fluorophores; it can be implemented using almost any conventional fluorescence microscopes, such as widefield, confocal, and total internal reflection fluorescence (TIRF) microscopes using conventional, non-photoswitchable fluorophores such as green fluorescent proteins (GFPs).[10] With SRRF, super-resolution live-cell imaging over timescales ranging from minutes to hours can be achieved.[11]

Whereas super-resolution techniques were initially developed to overcome the diffraction limit of light in fluorescence microscopy, the methodologies behind these techniques can also be used to improve the resolution of other imaging modalities, such as transmission electron microscopy (TEM). Despite having subnanometer resolutions,[12,13] many TEM images, especially those acquired from sensitive materials or captured with uncorrected aberrations, tend to have weak contrast, a low signal-to-noise ratio (SNR), and hence low resolution.[14,15] Similar to fluorescence microscopy, when the resolution of TEM images becomes a limiting factor, a super-resolution approach becomes necessary. However, it is very difficult, if not impossible, to apply the established super-resolution microscopy techniques (STED, PALM, STORM, SIM, SOFI, etc.) in TEM, as these methods require either specialized hardware that processes photons, not electrons, or photoswitchable fluorophores, not atomic structures. Unlike these methods, SRRF utilizes the intrinsic radial symmetry of the

microscope point spread function (PSF) and can be implemented easily without the requirement for additional hardware or photoswitchable emitters. Since TEM images also have intrinsic radial symmetric PSFs,[16] it is feasible to utilize the SRRF approach to improve the resolution of TEM images.

In this work, we show that SRRF, a super-resolution approach developed for fluorescence microscopy, can be used to enhance the resolution and quality of TEM images. Like SRRF in fluorescence microscopy, SRRF-TEM requires a sequence of multiple TEM images acquired from the same field of view (FOV) of the sample. However, the repetitive imaging of the same structure in TEM results in significant sample drift caused by thermally induced structural transformation and transition,[17,18] which should be compensated before SRRF processing. We demonstrate that a phase correlation-based image registration algorithm can correct for the sample drift in the TEM sequence. Three different samples were prepared and imaged using a commercial TEM system (FEI Titan 80–300). After the SRRF-TEM processing, substantial resolution enhancement can be observed on all the samples. We quantify the resolution improvement in SRRF-TEM results using Fourier ring correlation (FRC) resolutions.[19] We also evaluate how different parameters in SRRF affect the resolution and quality of resulting SRRF-TEM images. We utilize multiple open-source ImageJ (US National Institutes of Health) plug-ins for SRRF-TEM image processing,[20] such that the SRRF-TEM approach can be easily accessed by the existing TEM users.

An overview of the SRRF-TEM approach and a block diagram summarizing the steps of SRRF-TEM are shown in Fig. 1, where the image registration step corrects for thermally induced sample drift, the spatial SRRF step enhances image resolution, and the temporal SRRF step suppresses shot noise-induced artifacts. First, a sequence consisting of multiple TEM images (N frames in total) is acquired from the same FOV of the sample. Whereas the number of frames N is recommended to be as large as possible for SRRF in fluorescence microscopy,[10] in TEM, due to the thermal effects induced by electron beams, it may be impossible to acquire $N > 100$ frames of the same FOV without distorting the sample. As we demonstrate later in this work, a large number of total frames ($N > 100$) are not required to generate high-quality SRRF-TEM images. In this work, we prepared samples from three different materials, i.e., polycrystalline gallium nitride (GaN) on sapphire, polymer-coated carbon nanotubes (CNTs) on amorphized quartz, and nanoparticles (NPs). The TEM cross-sectional samples were prepared by Focus Ion Beam (FIB) using FEI Helios SEM/FIB dual beam equipment. This included depositing a protective iridium/platinum cap over the polymer-coated CNTs to help preserve the structural integrity of the cross section. The samples were then imaged with a FEI Titan 80–300 electron microscope in high-resolution TEM (HRTEM) mode.[21] To reduce thermally induced sample drift during the repetitive TEM acquisition, (a) each sample was imaged after waiting for an extended amount of time (e.g., 6 h) and (b) a short exposure time was used for image acquisition. Consequently, the intensities and contrast of the raw TEM images were lower than typical.

Even though care has been taken to reduce the sample drift and the FEI Titan 80–300 has excellent stability with a total system drift lower than 0.3 nm/min (rms),[21] notable image drift was still observed from the raw TEM sequences. Two examples of such drift can be seen in Fig. 2. Unlike image drift in fluorescence microscopy, which is mostly caused by living sample movement or stage drift,[22,23] TEM

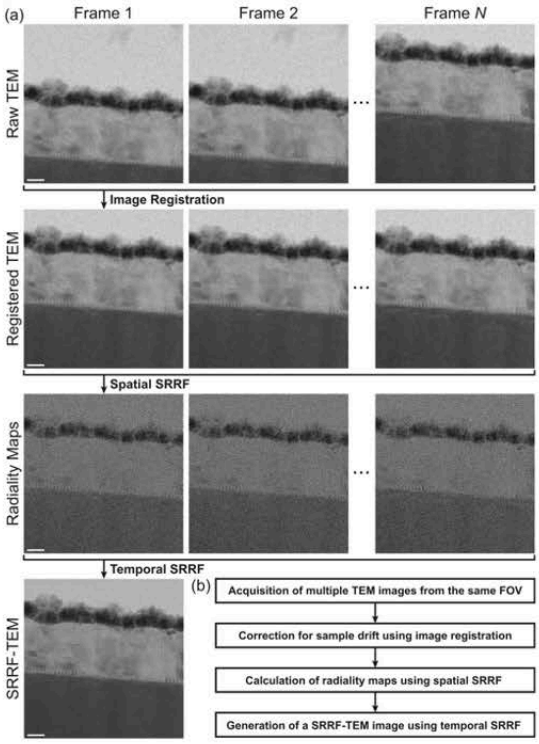

FIG. 1. Overview of the SRRF-TEM approach. (a) A sequence consisting of N raw TEM images is acquired (shown here are the experimental TEM images of polycrystalline GaN on a sapphire sample). An image registration algorithm is used to correct for sample drift. Then, spatial and temporal SRRF algorithms are sequentially utilized to generate an SRRF-TEM image for the sequence. (b) Block diagram summarizing the steps of SRRF-TEM. Scale bar, 10 nm.

image drift is caused by long-term thermal effects on samples and short-term fluctuations in the accelerating voltage and the objective lens current.[17,24] Therefore, the second step of SRRF-TEM is to correct for the drift in the raw TEM sequence using image registration algorithms. Here, we employed the "Correct 3D drift" ImageJ plug-in to register the TEM sequence, where pair-wise phase correlation analysis was used to determine the translation between each TEM frame, and the calculated offsets were then applied to the sequence.[25,26] Figure 2 shows the raw and registered sequences pseudo-color coded with each frame. Whereas the raw sequences are severely smeared, the image registration algorithm corrected for the drift such that no signs of drift can be observed in the registered sequences.

Next, the registered TEM sequence is processed using the SRRF algorithm, which consists of two distinct steps, a spatial and a temporal processing.[10,11] The spatial SRRF step magnifies each raw pixel in a TEM image into subpixels (by default, 1 raw pixel is magnified and divided into 5×5 subpixels) and assigns a value termed "radiality" to each subpixel. The radiality value at a subpixel is obtained by

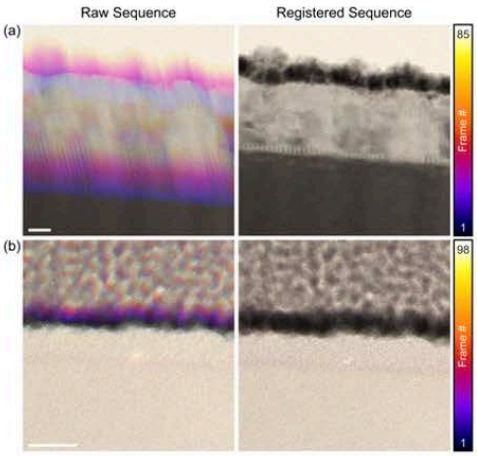

FIG. 2. Raw and registered experimental TEM sequences of (a) polycrystalline GaN on sapphire and (b) polymer-coated CNTs on amorphized quartz, pseudo-color coded to visualize the sample drift during the repeated image acquisition. The temporal scales for each frame in the sequences are shown on the right. Scale bar, 10 nm.

calculating the degree of convergence of a group of intensity gradient vectors connecting the subpixel and a ring of nearby surrounding subpixels (by default, 12 gradient vectors are considered). The ring radius of these surrounding subpixels determines the precision of the radiality distribution and consequently, the resolution, or the full width at half maximum (FWHM) of the PSF, of the resulting SRRF-TEM images. The radiality value is related to the probability of the subpixel containing an emitter: for a subpixel located at or close to the center of an emitter, there will be a high degree of convergence of surrounding gradient vectors and hence a high radiality value; for a subpixel far away from an emitter, the degree of convergence, or the radiality, will be low. The radiality value can also be seen as a measurement of local radial symmetries within the image originated from the intrinsic radial symmetry of the microscope PSF: a high radiality value means that the gradients surrounding the subpixel have high radial symmetry. This is the theoretical basis that the SRRF method is applicable to both fluorescence microscopy and TEM images, as both images have intrinsic radial symmetric PSFs.[16] The spatial SRRF processing is applied to each TEM image in the sequence, resulting in a sequence of the so-called radiality maps. Note that an intensity weighting procedure, which weights the radiality values by the raw pixel intensity, is used to conserve the quantitative information of raw images in radiality maps.

Finally, the sequence of radiality maps is subsequently processed by the temporal SRRF step to generate a single resolution-enhanced SRRF-TEM image. The temporal SRRF processing analyzes the fluctuations in radiality values within the sequence and extracts further information on the true positions of the emitters using cumulant analysis. Due to the shot noise induced by the discrete nature of electrons and the detection systems,[27] some pixels in the raw images tend to have high intensity and hence high radiality values, even though they are not close to a true emitter; these pixels result in the grainy and noisy appearance of individual radiality maps shown in Fig. 1. To prevent these shot noise-induced artifacts from appearing in the resulting SRRF-TEM image, the temporal SRRF step analyzes the temporal statistics of the whole radiality map sequence such that the radiality fluctuations caused by noise are suppressed, while the radiality values of true emitters are preserved and possibly enhanced using high-order cumulant analysis (by default, first-order cumulant analysis, i.e., averaging, is used). We employed the "NanoJ-SRRF" ImageJ plug-in to perform both the spatial and temporal SRRF processing on the registered TEM sequence.[10]

Figure 3 shows the application of SRRF-TEM processing to TEM images of Al_2O_3 simulated using the QSTEM simulation software.[28] A ground truth image of a Al_2O_3 structure (20 Å × 20 Å × 20 Å) was simulated using a high-resolution probe array (400 × 400 pixels, 0.05 Å resolution), while 64 raw TEM images of the same FOV were simulated using a low-resolution probe array (50 × 50 pixels, 0.4 Å resolution) with shot noise added (100 counts). The QSTEM simulation parameters were set as follows: 300 kV high voltage, −54.3 nm defocus, 1.0 mm spherical aberration, 1.0 mm chromatic aberration, 300 K temperature, 15 mrad convergence angle, 5×10^8 brightness ($A\,cm^{-2}sr^{-1}$), and 1 μs dwell time. The 64 raw TEM images were then used to generate the SRRF-TEM image shown in Fig. 3(a). As shown in Fig. 3(b), the SRRF-TEM image substantially enhances the resolution, contrast, and SNR of the raw TEM image. Compared to the ground truth, the SRRF-TEM image exhibits comparable image resolution and quality despite the lower contrast between the aluminum and oxygen atoms.

Figure 4 compares the raw TEM and SRRF-TEM images of crystalline and amorphous surfaces from three different samples. Four sequences consisting of 85, 146, 98, and 83 raw TEM images were used to generate the SRRF-TEM results for the GaN, CNT, and NP samples in Fig. 4(a), respectively. We attempted to take more raw TEM images of the same FOV in our experiments; however, it turned out that doing so severely distorted and deformed the morphology of the sample, so we stopped the image acquisition and included only the undistorted frames in the SRRF-TEM analysis. As shown in Fig. 4(b), even with a limited number of frames ($N < 100$), a substantial enhancement in both image resolution and quality can be seen in SRRF-TEM images compared to their raw TEM counterparts: the blurry and low-contrast atomic layers and materials interfaces in the raw TEM images become cleaner, sharper, and with stronger contrast in the SRRF-TEM ones. Notably, the cross section of a CNT (Fig. 4, 3rd row), which can hardly be separated from its polymeric embedding layer in the raw TEM image, can be clearly discerned from the background in the SRRF-TEM one.

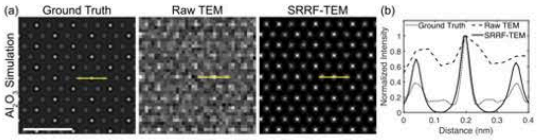

FIG. 3. Application of SRRF-TEM to simulated TEM images. (a) Ground truth (high-resolution, noise free) and raw TEM (low resolution, shot noise added) images of Al_2O_3 simulated using the QSTEM simulation software. The SRRF-TEM image was generated from 64 simulated raw TEM images. (b) Line profiles of the normalized pixel intensity values along the yellow lines in (a). Scale bar, 0.5 nm.

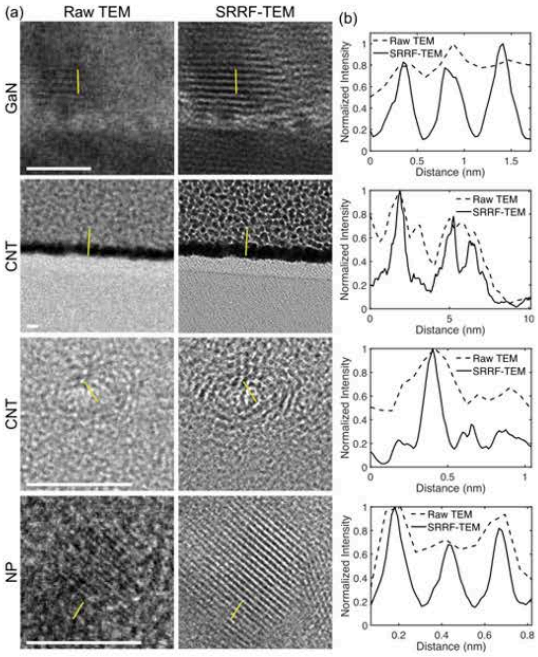

FIG. 4. Application of SRRF-TEM to experimental TEM images. (a) Comparison between raw TEM and SRRF-TEM images in four experiments acquired from three different samples: polycrystalline GaN on sapphire, polymer-coated CNTs on amorphized quartz, and nanoparticles (NPs). (b) Line profiles of the normalized pixel intensity values along the yellow lines in (a). Scale bar, 5 nm.

To quantify the resolution enhancement of SRRF-TEM and evaluate how different parameters in the SRRF algorithm affect the results, we utilized Fourier ring correlation (FRC), an image-resolution measure that is based on the spectral SNR of the images and can be computed from the two images of the same scene (FOV), which differ only in noise content.[19,29] Specifically, the raw TEM image sequences were evenly divided and processed into two SRRF-TEM images, which were used as two inputs for the "FRC" ImageJ plug-in to calculate the FRC resolution by locating the spatial frequency for which the FRC value dropped below a threshold (1/7). We first evaluated the effects of spatial SRRF parameters, i.e., the ring radius, on SRRF-FLIM results. The 98-frame raw TEM sequence of the CNT sample was divided into two independent 49-frame sequences, which were processed through the SRRF-TEM approach multiple times using different ring radii; the two SRRF-TEM images after each processing were used to calculate the FRC resolution. This whole process was repeated for 16 experiments on different FOVs of the sample, and the results are summarized in Fig. 5. A relatively consistent resolution performance can be seen for a ring radius between 0.1 and 1.0; when the ring radius is larger than 1.0, as the radius increases, the resolution becomes worse with larger means and standard deviations. This is consistent with the SRRF results acquired with fluorescence microscopes, where a smaller ring

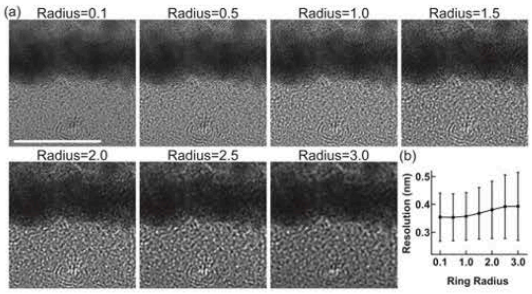

FIG. 5. Spatial SRRF parameters affect the resolution improvement in SRRF-TEM. (a) SRRF-TEM images generated from the same raw experimental TEM sequence of the CNT sample but using different ring radii. (b) FRC resolution as a function of the ring radius. Means and standard deviations are obtained from $n = 16$ experiments. Scale bar, 10 nm.

radius generally leads to a smaller FWHM of the PSF and consequently a higher resolution.[10] Therefore, a ring radius between 0.1 and 1.0 is preferred for SRRF-TEM.

We used the same analysis to evaluate the effects of temporal SRRF parameters, including the total number of frames (N) in the raw TEM sequence and the mode of cumulant analysis, on the resolution of SRRF-TEM results. To evaluate N, we chose the 146-frame raw TEM-sequence of the CNT sample as it has sufficient frames to be divided into two sub-sequences with up to 64 frames. Figures 6(a) and 6(b) show that, as the number of frames increases, the resulting SRRF-TEM image appears less noisy, and both the mean and standard deviation of the FRC resolution becomes smaller. In other words, including more frames in the raw TEM sequence improves the quality and resolution of the SRRF-TEM result. However, as we mentioned earlier, for some sensitive samples, it may be impossible to acquire a large number of (e.g., $N > 100$) raw TEM images without distorting it. Nevertheless, as Fig. 6(b) suggests, a sequence consisting of $N > 30$ raw TEM frames can already provide a decent resolution-enhancement performance in SRRF-TEM. Finally, we divided the 146-frame CNT sequence into two 72-frame sub-sequences and evaluated the SRRF-TEM performance with respect to different modes of cumulant analysis, including temporal radiality maximum (TRM), temporal radiality average (TRA), temporal radiality pairwise product mean (TRPPM), and temporal radiality autocumulant (TRAC) of second, third, and fourth orders. The results are summarized in Figs. 6(c) and 6(d), where we also included a conventional average (AVG) projection of raw TEM images for comparison. Unlike SRRF in fluorescence microscopy, where higher-order cumulants (TRAC2–4) can provide higher resolution than lower-order ones (TRA, TRM, and TRPPM),[10] SRRF-TEM performs best with lower-order cumulants, especially TRPPM and the default TRA analysis.

In conclusion, we have demonstrated that SRRF, a super-resolution approach developed for fluorescence microscopy, can be used to improve the resolution and quality of TEM images. Substantial enhancement of resolution has been demonstrated for SRRF-TEM images acquired from three different samples, where blurry and low-contrast structural layers and interfaces become sharper and with stronger contrast. By quantifying and evaluating the SRRF-TEM performance using FRC resolutions, we have found a set of optimal

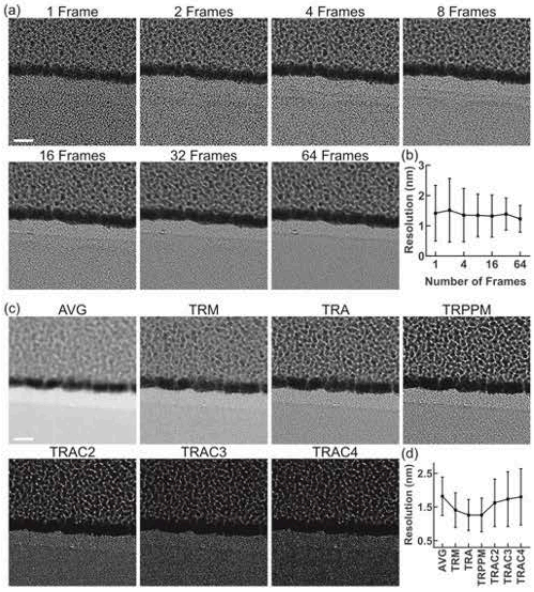

FIG. 6. Temporal SRRF parameters affect the resolution enhancement in SRRF-TEM. (a) SRRF-TEM images generated from different numbers of frames within a raw experimental TEM sequence of the CNT sample. (b) FRC resolution as a function of the number of frames included in SRRF-TEM. (c) SRRF-TEM images generated from the same raw experimental TEM sequence of the CNT sample but using different modes of cumulant analysis. (d) Relationship between the FRC resolution and the cumulant analysis mode used in SRRF-TEM. Means and standard deviations in (b) and (d) are obtained from $n = 16$ experiments. Scale bar, 10 nm.

SRRF-TEM parameters (a ring radius between 0.1 and 1.0, a sequence of more than 30 raw TEM frames, and a cumulant analysis mode of TRA or TRPPM), which could be used as guidelines for interested TEM users. We believe that SRRF-TEM has the potential to become a powerful tool in materials research, and SRRF could also be used to enhance the resolution of other imaging modalities, such as photoacoustic imaging, magnetic resonance imaging, and neutron imaging.

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REFERENCES

[1]J. W. Lichtman and J.-A. Conchello, "Fluorescence microscopy," Nat. Methods **2**, 910–919 (2005).
[2]S. W. Hell, "Far-field optical nanoscopy," Science **316**, 1153–1158 (2007).
[3]S. W. Hell and J. Wichmann, "Breaking the diffraction resolution limit by stimulated emission: Stimulated-emission-depletion fluorescence microscopy," Opt. Lett. **19**, 780–782 (1994).
[4]T. A. Klar, S. Jakobs, M. Dyba, A. Egner, and S. W. Hell, "Fluorescence microscopy with diffraction resolution barrier broken by stimulated emission," Proc. Natl. Acad. Sci. U. S. A. **97**, 8206–8210 (2000).
[5]E. Betzig, G. H. Patterson, R. Sougrat, O. W. Lindwasser, S. Olenych, J. S. Bonifacino, M. W. Davidson, J. Lippincott-Schwartz, and H. F. Hess, "Imaging intracellular fluorescent proteins at nanometer resolution," Science **313**, 1642–1645 (2006).
[6]M. J. Rust, M. Bates, and X. Zhuang, "Sub-diffraction-limit imaging by stochastic optical reconstruction microscopy (STORM)," Nat. Methods **3**, 793–796 (2006).
[7]M. G. L. Gustafsson, "Surpassing the lateral resolution limit by a factor of two using structured illumination microscopy," J. Microsc. **198**, 82–87 (2000).
[8]M. G. L. Gustafsson, "Nonlinear structured-illumination microscopy: Wide-field fluorescence imaging with theoretically unlimited resolution," Proc. Natl. Acad. Sci. U. S. A. **102**, 13081–13086 (2005).
[9]T. Dertinger, R. Colyer, G. Iyer, S. Weiss, and J. Enderlein, "Fast, background-free, 3D super-resolution optical fluctuation imaging (SOFI)," Proc. Natl. Acad. Sci. U. S. A. **106**, 22287–22292 (2009).
[10]N. Gustafsson, S. Culley, G. Ashdown, D. M. Owen, P. M. Pereira, and R. Henriques, "Fast live-cell conventional fluorophore nanoscopy with ImageJ through super-resolution radial fluctuations," Nat. Commun. **7**, 12471 (2016).
[11]S. Culley, K. L. Tosheva, P. M. Pereira, and R. Henriques, "SRRF: Universal live-cell super-resolution microscopy," Int. J. Biochem. Cell B. **101**, 74–79 (2018).
[12]D. B. Williams and C. B. Carter, *Transmission Electron Microscopy* (Springer US, 1996).
[13]J. C. H. Spence, *High-Resolution Electron Microscopy* (Oxford University Press, 2013).
[14]M. Haider, S. Uhlemann, E. Schwan, H. Rose, B. Kabius, and K. Urban, "Electron microscopy image enhanced," Nature **392**, 768–769 (1998).
[15]P. E. Batson, N. Dellby, and O. L. Krivanek, "Sub-ångstrom resolution using aberration corrected electron optics," Nature **418**, 617–620 (2002).
[16]A. R. Lupini and N. de Jonge, "The three-dimensional point spread function of aberration-corrected scanning transmission electron microscopy," Microsc. Microanal. **17**, 817–826 (2011).
[17]Z. Wang, "New developments in transmission electron microscopy for nanotechnology," Adv. Mater. **15**, 1497–1514 (2003).
[18]X. Sang and J. M. LeBeau, "Revolving scanning transmission electron microscopy: Correcting sample drift distortion without prior knowledge," Ultramicroscopy **138**, 28–35 (2014).
[19]R. P. J. Nieuwenhuizen, K. A. Lidke, M. Bates, D. L. Puig, D. Grünwald, S. Stallinga, and B. Rieger, "Measuring image resolution in optical nanoscopy," Nat. Methods **10**, 557–562 (2013).
[20]C. A. Schneider, W. S. Rasband, and K. W. Eliceiri, "NIH Image to ImageJ: 25 years of image analysis," Nat. Methods **9**, 671–675 (2012).
[21]A. Thust, J. Barthel, and K. Tillmann, "FEI Titan 80-300 TEM," J. Large-Scale Res. Facil. **2**, A41 (2016).
[22]M. J. Mlodzianoski, J. M. Schreiner, S. P. Callahan, K. Smolková, A. Dlasková, J. Šantorová, P. Ježek, and J. Bewersdorf, "Sample drift correction in 3D fluorescence photoactivation localization microscopy," Opt. Express **19**, 15009 (2011).
[23]S. H. Lee, M. Baday, M. Tjioe, P. D. Simonson, R. Zhang, E. Cai, and P. R. Selvin, "Using fixed fiduciary markers for stage drift correction," Opt. Express **20**, 12177 (2012).
[24]J. Barthel and A. Thust, "Aberration measurement in HRTEM: Implementation and diagnostic use of numerical procedures for the highly precise recognition of diffractogram patterns," Ultramicroscopy **111**, 27–46 (2010).
[25]S. Preibisch, S. Saalfeld, and P. Tomancak, "Globally optimal stitching of tiled 3D microscopic image acquisitions," Bioinformatics **25**, 1463–1465 (2009).
[26]A. Parslow, A. Cardona, and R. J. Bryson-Richardson, "Sample drift correction following 4D confocal time-lapse imaging," J. Vis. Exp. **86**, e51086 (2014).
[27]T. Seki, Y. Ikuhara, and N. Shibata, "Theoretical framework of statistical noise in scanning transmission electron microscopy," Ultramicroscopy **193**, 118–125 (2018).
[28]C. Koch, *Determination of Core Structure Periodicity and Point Defect Density Along Dislocations* (Arizona State University, 2002).
[29]M. Unser, B. L. Trus, and A. C. Steven, "A new resolution criterion based on spectral signal-to-noise ratios," Ultramicroscopy **23**, 39–51 (1987).